Cypress Semiconductor
Product Qualification Report

QTP# 091706 VERSION 2.0
May 2010

72 Meg QDR/DDR Synchronous SRAM Family 65nm (LL65P-18R) Technology, UMC Fab 12A	
CY7C11431KV18	18-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C11481/501KV18	18-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C11651KV18	18-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C11681/701KV18	18-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C13121KV18	18-Mbit QDR® II SRAM 2-Word Burst Architecture
CY7C13141KV18	18-Mbit QDR® II SRAM 2-Word Burst Architecture
CY7C13201KV18	18-Mbit DDR-II SRAM 2-Word Burst Architecture
CY7C21701KV18	18-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) With ODT
CY7C12651KV18	36-Mbit QDR® II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C12451KV18	36-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C12481KV18	36-Mbit DDR II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C12501KV18	36-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C12631KV18	36-Mbit QDR® II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C12681KV18	36-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C12701KV18	36-Mbit DDR II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C14121KV18	36-Mbit QDR® II SRAM 2-Word Burst Architecture
CY7C14141/251KV18	36-Mbit QDR™-II SRAM 2-Word Burst Architecture
CY7C14181KV18	36-Mbit DDR II SRAM 2-Word Burst Architecture
CY7C14201KV18	36-Mbit DDR-II SRAM 2-Word Burst Architecture
CY7C1512/14KV18	72-Mbit QDR™-II SRAM 2-Word Burst Architecture
CY7C1513/15KV18	72-Mbit QDR™-II SRAM 4-Word Burst Architecture
CY7C1518/20KV18	72-Mbit DDR-II SRAM 2-Word Burst Architecture
CY7C1523KV18	72-Mbit DDRII SIO SRAM 2-Word Burst Architecture
CY7C1525KV18	72-Mbit QDR™-II SRAM 2-Word Burst Architecture
CY7C1526KV18	72-Mbit QDR™-II SRAM 4-Word Burst Architecture
CY7C1543/45KV18	72-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1548/50KV18	72-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1563/631/632KV18 CY7C1565KV18	72-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1564KV18	72-Mbit QDR™-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1568/70KV18	72-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C2544KV18	72-Mbit QDR™-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency) with ODT
CY7C2563/65KV18	72-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2564KV18	72-Mbit QDR™-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2568/70KV18	72-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) with ODT

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
091706		Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die Product Family	Aug 2009
093202		Qualification of UMC 65nm Process Improvement	Nov 2009

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose:	Qualify UMC Fab 12A 65nm (LL65P-18R) Technology and 7C1553K base die product family	
Marketing Part #:	CY7C1514KV18, CY7C15631KV18	
Device Description:	1.8V Commercial and Industrial available in 165-Ball FBGA (13 x 15 x 1.4 mm)	
Cypress Division:	Cypress Semiconductor Corporation –Memory & Image Division	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. K
What ID markings on Die:	7C1553K	

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65P-18R			
Number of Metal Layers:	5+RDL	Metal Composition:	Metal 1: Cu 0.18um Metal 2: Cu 0.22um Metal 3: Cu 0.22um Metal 4: Cu 0.36um Metal 5: Cu 1.25um Metal 6 (RDL): Al 1.2um
Passivation Type and Materials:			0.4um Oxide / 0.5um Nitride
Free Phosphorus contents in top glass layer(%):			0 %
Number of Transistors in Device			~600M
Number of Logic Gates in Device			~300M
Generic Process Technology/Design Rule (µ-drawn):			CMOS, 65nm
Gate Oxide Material/Thickness (MOS):			19.5A
Name/Location of Die Fab (prime) Facility:			UMC Fab 12
Die Fab Line ID/Wafer Process ID:			L65LL

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**ASE-Taiwan, CML Autoline**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	KE-G2270 / Kyocera
Mold Compound Flammability Rating:	UL94, V-0
Oxygen Rating Index:	N/A
Substrate Material:	BT resin
Lead Finish, Composition / Thickness:	Sn63Pb37
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-42742
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	13.7
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-06518
Name/Location of Assembly (prime) facility:	ASE-Taiwan/CML-Philippine

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Chipmos

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C/150°C	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 80hrs, 500hrs & 1000hrs	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.25V, -30°C	P
High Accelerated Saturation Test (HAST)	130°C, 2.25V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Temperature Humidity Bias Test (THB)	85°C, 2.25V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow**, 260°C**+0, -5°C	P
Precondition	JESD22 Moisture Sensitivity	P
High Temperature Storage	150°C ± 5°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V, JESD22-A114E	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C Cypress Spec. 25-00020	P
Electrostatic Discharge Machine Model (ESD-MM)	200V, JESD22-A115-A Cypress Spec. 25-00020	P
Soft Error (Alpha Particle)	JESD89A, Cypress Spec. 001-47027	P
Soft Error (Neutron/Proton)	JESD89A, Cypress Spec. 001-45212	P
Current Density	Cypress Spec 22-00029	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	Cypress Spec. 25-00104	P
Dynamic Latchup	In accordance with Cypress Spec. 01-00081	P
Static Latchup	125C, ± 200mA In accordance with JESD78 and Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	9,004 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate (150°C)	89,000 DHRs	0	0.7	170	22 FIT
High Temperature Operating Life[1,2] Long Term Failure Rate (125°C)	479,920 DHRs	0	0.7	55	

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	1000	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		

Reliability Test Data

QTP #: 093202

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	COMP	8	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	1000	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	96	596	0	
CY7C15631KV18 (7C1553K)	8910015	610921676	TAIWN-G	96	711	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	96	1795	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	168	190	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	500	184	0	