ICS87339I-11

Low Skew, ÷2/4,÷4/5/6, Differential-to-3.3V LVPECL Clock Generator

General Description

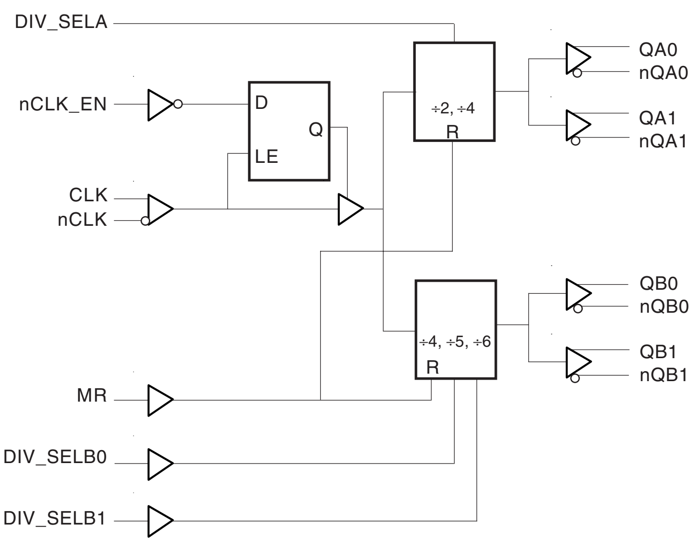
The ICS87339I-11 is a low skew, high performance Differential-to-3.3V LVPECL Clock Generator/Divider and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS87339I-11 has one differential clock input pair. The CLK, nCLK pair can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS87339I-11 ideal for clock distribution applications demanding well defined performance and repeatability.

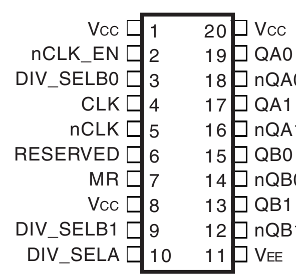
Features

- Dual ÷2, ÷4 differential 3.3V LVPECL outputs;
  Dual ÷4, ÷5, ÷6 differential 3.3V LVPECL outputs
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum clock input frequency: 1GHz
- Translates any single ended input signal (LVCMOS, LVTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Output skew: 35ps (maximum)
- Part-to-part skew: 385ps (maximum)
- Bank skew: Bank A - 20ps (maximum)
  Bank B - 20ps (maximum)
- Propagation delay: 2.1ns (maximum)
- LVPECL mode operating voltage supply range:
  V_{CC} = 3V to 3.6V, V_{EE} = 0V
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS87339I-11

20-Lead TSSOP
6.50mm x 4.40mm x 0.92 package body
G Package
Top View

20-Lead SOIC, 300MIL
7.5mm x 12.8mm x 2.25mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 8, 20	V_{CC}	Power		Positive supply pins.
2	nCLK_EN	Input	Pulldown	Clock enable. LVCMOS / LVTTL interface levels. See Table 3.
3	DIV_SELB0	Input	Pulldown	Selects divide value for Bank B outputs as described in Table 3. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	RESERVED	Reserve		Reserve pin.
7	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
9	DIV_SELB1	Input	Pulldown	Selects divide value for Bank B outputs as described in Table 3. LVCMOS / LVTTL interface levels.
10	DIV_SELA	Input	Pulldown	Selects divide value for Bank A outputs as described in Table 3. LVCMOS / LVTTL interface levels.
11	V_{EE}	Power		Negative supply pin.
12, 13	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
14, 15	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
16, 17	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
18, 19	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs					Outputs			
MR	nCLK_EN	DIV_SELA	DIV_SELB0	DIV_SELB1	QA0, QA1	nQA0, nQA1	QB0, QB1	nQB0, nQB1
1	X	X	X	X	LOW	HIGH	LOW	HIGH
0	1	X	X	X	Not Switching	Not Switching	Not Switching	Not Switching
0	0	0	0	0	÷2	÷2	÷4	÷4
0	0	0	0	1	÷2	÷2	÷5	÷5
0	0	0	1	0	÷2	÷2	÷6	÷6
0	0	0	1	1	÷2	÷2	÷5	÷5
0	0	1	0	0	÷4	÷4	÷4	÷4
0	0	1	0	1	÷4	÷4	÷5	÷5
0	0	1	1	0	÷4	÷4	÷6	÷6
0	0	1	1	1	÷4	÷4	÷5	÷5

NOTE: After nCLK_EN switches, the clock outputs stop switching following a rising and falling input clock edge.

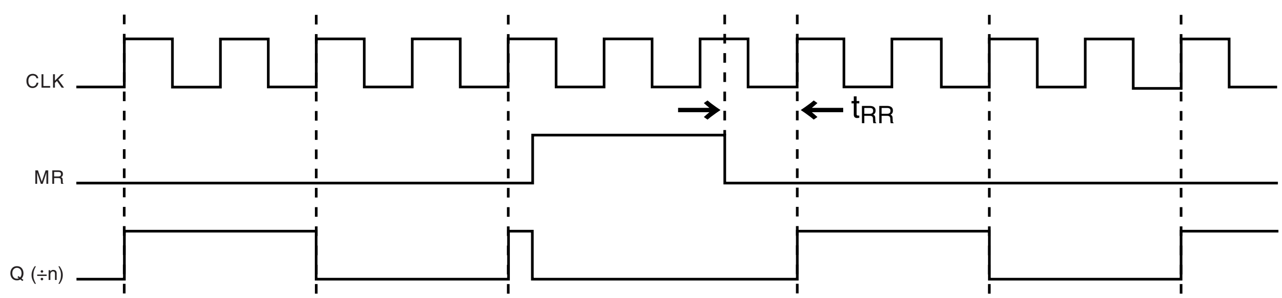


FIGURE 1A. MR TIMING DIAGRAM

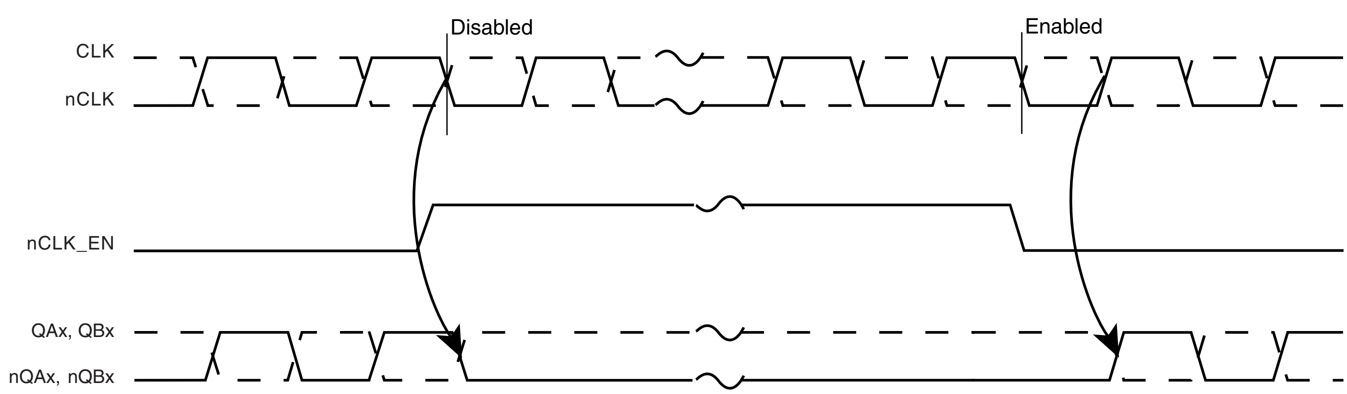


FIGURE 1B. nCLK_EN TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	
20 Lead TSSOP	73.2°C/W (0 lfpm)
20 Lead SOIC	46.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{EE}	Power Supply Current				105	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nCLK_EN, MR, DIV_SELA, DIV_SELBx	$V_{IN} = V_{CC}$ = 3.6V			150	µA
I_{IL}	Input Low Current	nCLK_EN, MR, DIV_SELA, DIV_SELBx	V_{IN} = 0V, V_{CC} = 3.6V	-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{IN} = V_{CC}$ = 3.6V			5	µA
		CLK	$V_{IN} = V_{CC}$ = 3.6V			150	µA
I_{IL}	Input Low Current	nCLK	V_{IN} = 0V, V_{CC} = 3.6V	-150			µA
		CLK	V_{IN} = 0V, V_{CC} = 3.6V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

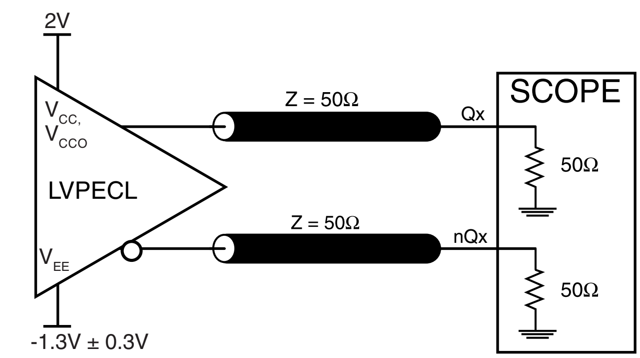
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

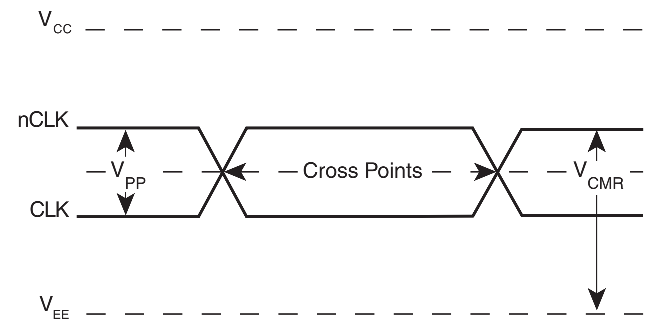
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{CLK}	Clock Input Frequency					1	GHz
t_{PD}	Propagation Delay; NOTE 1		CLK to Q (Diff)	1.6		2.1	ns
*t*sk(o)	Output Skew; NOTE 2, 5				15	35	ps
*t*sk(b)	Bank Skew; NOTE 3, 5	Bank A			10	20	ps
		Bank B			10	20	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5					385	ps
t_S	Setup Time	nCLK_EN to CLK		350			ps
t_H	Hold Time	CLK to nCLK_EN		100			ps
t_{RR}	Reset Recovery Time					400	ps
t_{PW}	Minimum Pulse Width	CLK		550			ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	100		600	ps
odc	Output Duty Cycle			48		52	%

All data taken with outputs ÷4.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points
NOTE 3: Defined as skew within a bank of outputs and with equal load conditions.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

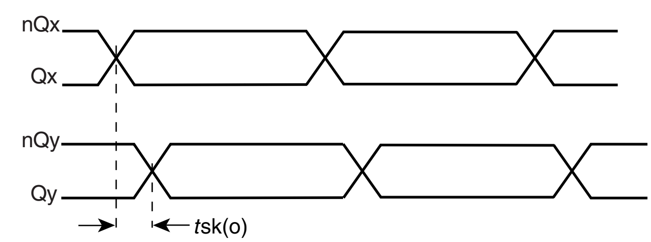
PARAMETER MEASUREMENT INFORMATION



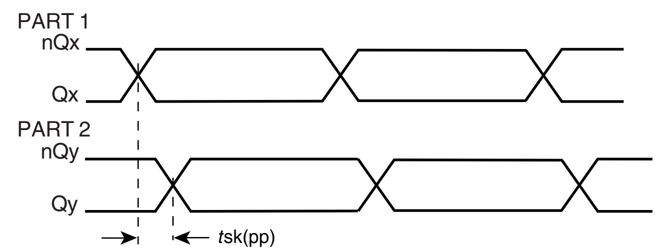
3.3V OUTPUT LOAD AC TEST CIRCUIT



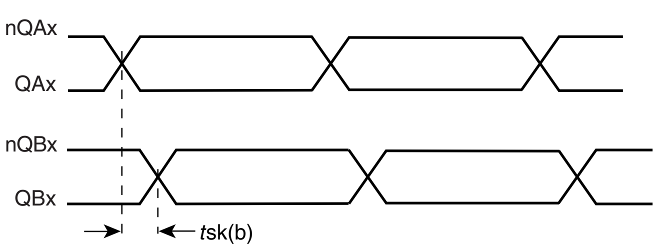
DIFFERENTIAL INPUT LEVEL



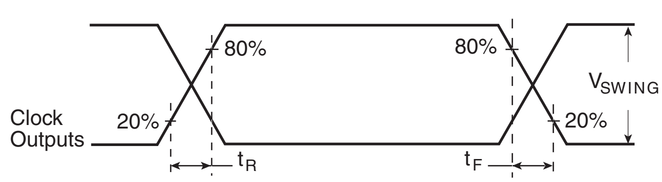
OUTPUT SKEW



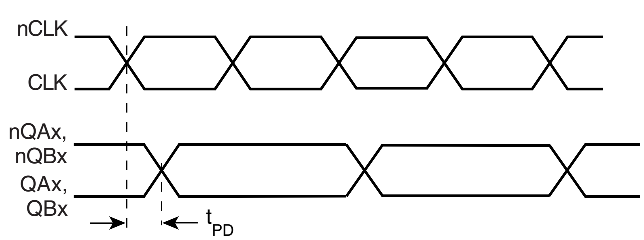
PART-TO-PART SKEW



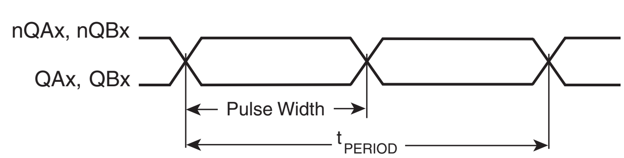
BANK SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

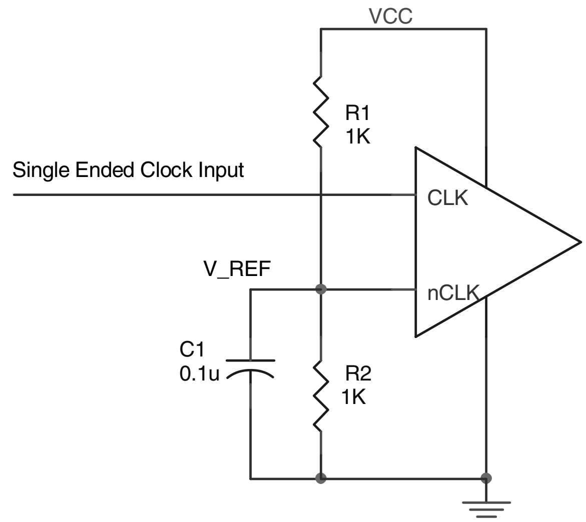
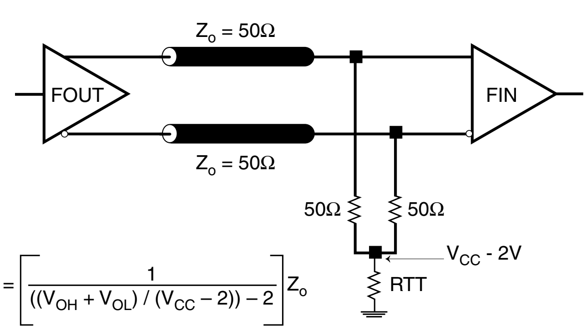


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



$$RTT = \left[\frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2}\right] Z_o$$

FIGURE 3A. LVPECL OUTPUT TERMINATION

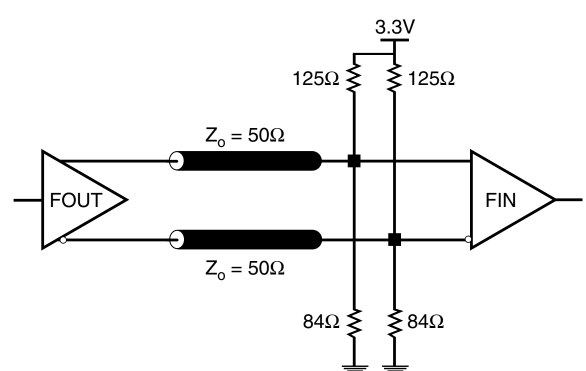


FIGURE 3B. LVPECL OUTPUT TERMINATION

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

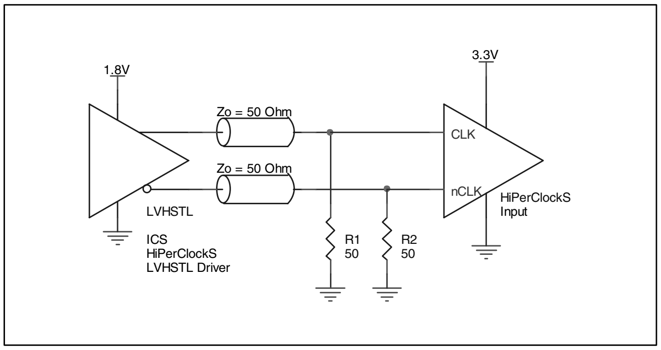


FIGURE 4A. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

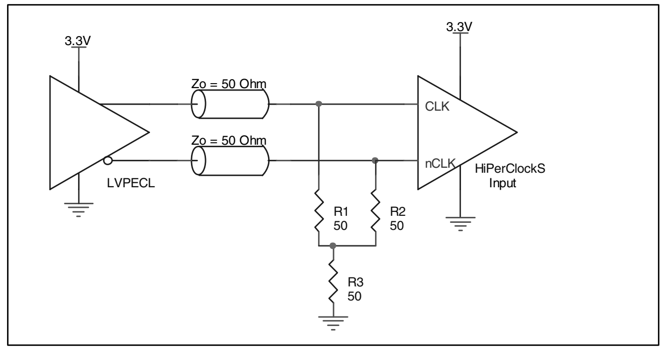


FIGURE 4B. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

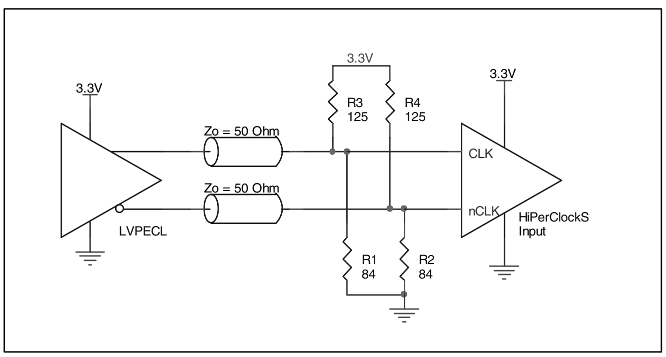


FIGURE 4C. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

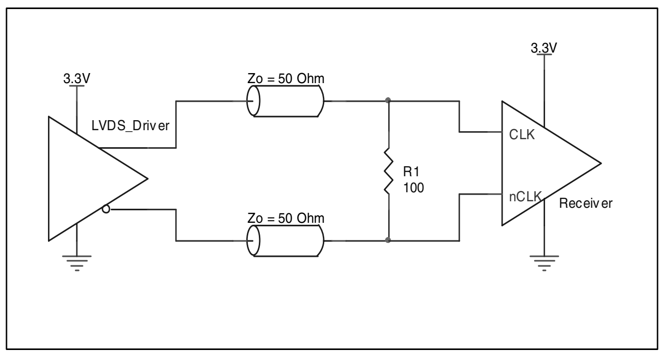


FIGURE 4D. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

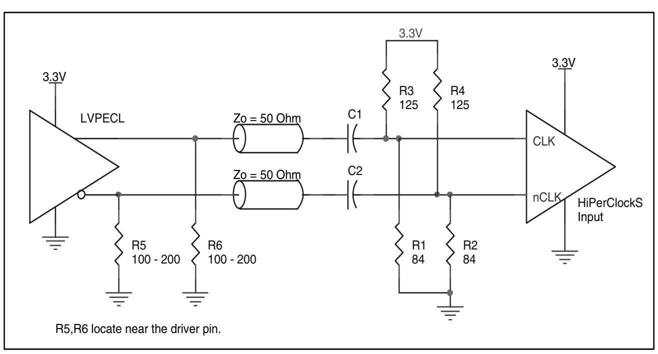


FIGURE 4E. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87339I-11.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS87339I-11 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 0.3V = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{CC_MAX} = 3.6V * 105mA = **378mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{\_MAX}$ (3.6V, with all outputs switching) = 378mW + 120mW = **498mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6A below.
Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.498W * 66.6°C/W = 118.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 6B. Thermal Resistance θ_{JA} for 20-pin SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 5.*

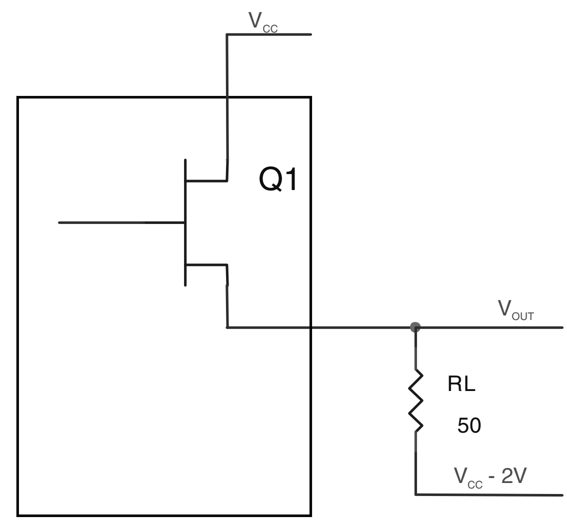


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TSSOP TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 7B. θ_{JA} VS. AIR FLOW SOIC TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

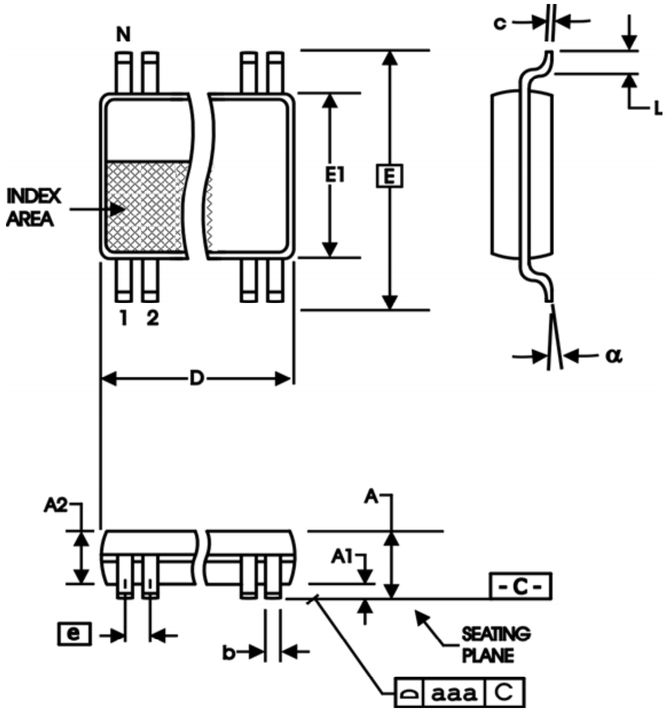
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87339I-11 is: 1745

Compatible with MC10EP139, MC100EP139

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP



PACKAGE OUTLINE - M SUFFIX FOR 20 LEAD SOIC

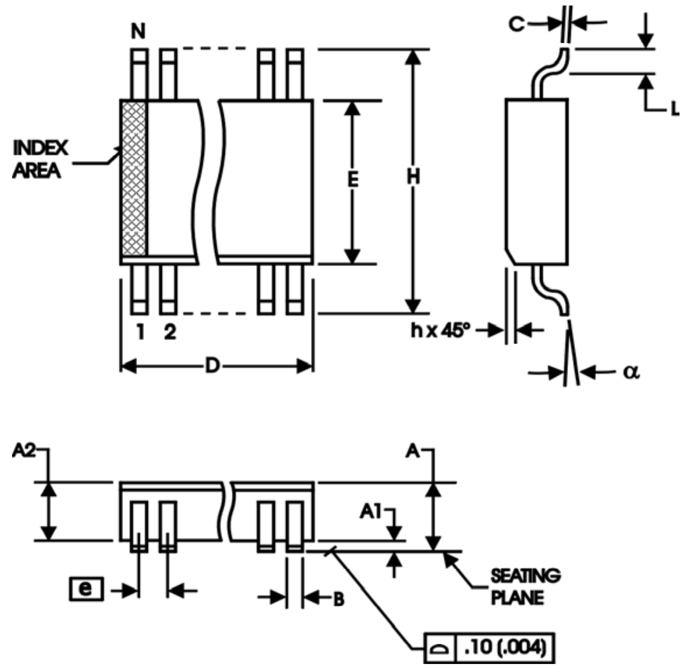


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87339AGI-11	ICS87339AI11	20 lead TSSOP	Tube	-40°C to 85°C
87339AGI-11T	ICS87339AI11	20 lead TSSOP	2500 Tape & Reel	-40°C to 85°C
87339AGI-11LF	ICS7339AI11L	20 Lead "Lead-Free" TSSOP	Tube	-40°C to 85°C
87339AGI-11LFT	ICS7339AI11L	20 Lead "Lead-Free" TSSOP	2500 Tape & Reel	-40°C to 85°C
87339AMI-11	ICS87339AMI-11	20 lead SOIC	Tube	-40°C to 85°C
87339AMI-11T	ICS87339AMI-11	20 lead SOIC	1000 Tape & Reel	-40°C to 85°C
87339AMI-11LF	ICS7339AI11L	20 Lead "Lead-Free" SOIC	Tube	-40°C to 85°C
87339AMI-11LFT	ICS7339AI11L	20 Lead "Lead-Free" SOIC	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1	1 2	Pin Assignment - changed pin 6, "nc" to "reserved". Pin Description table - corrected pin 6 to read reserved to coordinate with Pin Assignment.	3/10/05
A	 T9	1 13	Features section - corrected Output skew and Part-to-Part skew bullets. Ordering Information table - added Lead-Free note.	4/12/05
A	T9	13	Ordering Information table - added Lead-Free markings	12/19/07