TEXAS INSTRUMENTS

ADS8364EVM

User's Guide

April 2002

Data Acquisition Products

SLAU084

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It is important to operate this EVM within the input voltage range of ±12 VDC and output voltage range of 3.3 VDC and 5 VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Texas Instruments
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Dallas, Texas 75265

Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the ADS8364EVM 16-bit parallel analog-to-digital converter evaluation board. A complete circuit description as well as schematic diagram is included.

How to Use This Manual

This document contains the following chapters:

Chapter 1—EVM Overview

Chapter 2—Analog Interface

Chapter 3—Digital Interface

Chapter 4—Power Supply

Chapter 5—Initial Setup of the Board

Chapter 6—EVM Schematic

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This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

CAUTION

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

WARNING

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Data Sheets	Literature Number
ADS8364	SBAS219
OPA2132	SBOS054
OPA2350	SBOS099
TPS2104	SLVS235
SN74CBT3257	SCDS017

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Chapter 1

EVM Overview

The ADS8364 is a high-speed, low power, dual 16-bit A/D converter that operates from independent 5-V AV_{DD} and DV_{DD} supplies. The digital output is delivered through a built-in buffer circuit that can be powered from DV_{DD} or separate 2.7-V to 5.25-V (BV_{DD}) sources. This allows for flexibility when designing within mixed voltage environments.

The six fully differential sample and hold circuits are divided into three pairs (A, B, and C). Each pair of channels has a hold signal (HOLDA, HOLDB, and HOLDC) which, when strobed together, allows simultaneous sampling on all six analog inputs. The part accepts an analog input voltage in the range of $–V_{REF}$ to $+V_{REF}$, centered on the internal 2.5-V reference. The part also accepts bipolar input ranges when a level shift circuit is used in the analog front-end circuitry (see Figure 2-1).

Conversion time for the ADS8364 is 3.2 μs when a 5-MHz external clock is used. The corresponding acquisition time is 0.8 μs. To achieve the maximum output rate (250 KSPS), the read function can be performed during the start of the next conversion.

The ADS8364 EVM includes the following features:

- Full-featured evaluation board for the ADS8364 250-kHz, 16-bit, 6-channel simultaneous sampling analog-to-digital converter
- Analog inputs can be configured as single-ended or differential
- Direct connection to C5000 and C6000 DSK platforms through the 80-pin interface connectors
- Built-in reference
- High-speed parallel interface

Chapter 2

Analog Interface

The analog portion of the board is divided in two parts. The input buffer represents the front-end circuit of the A/D converter. Its function is to provide level and impedance changes to the input signal. The second part is the voltage reference circuit. In addition to being the conversion reference, the ADS8364's reference output is used for level shifting the analog input.

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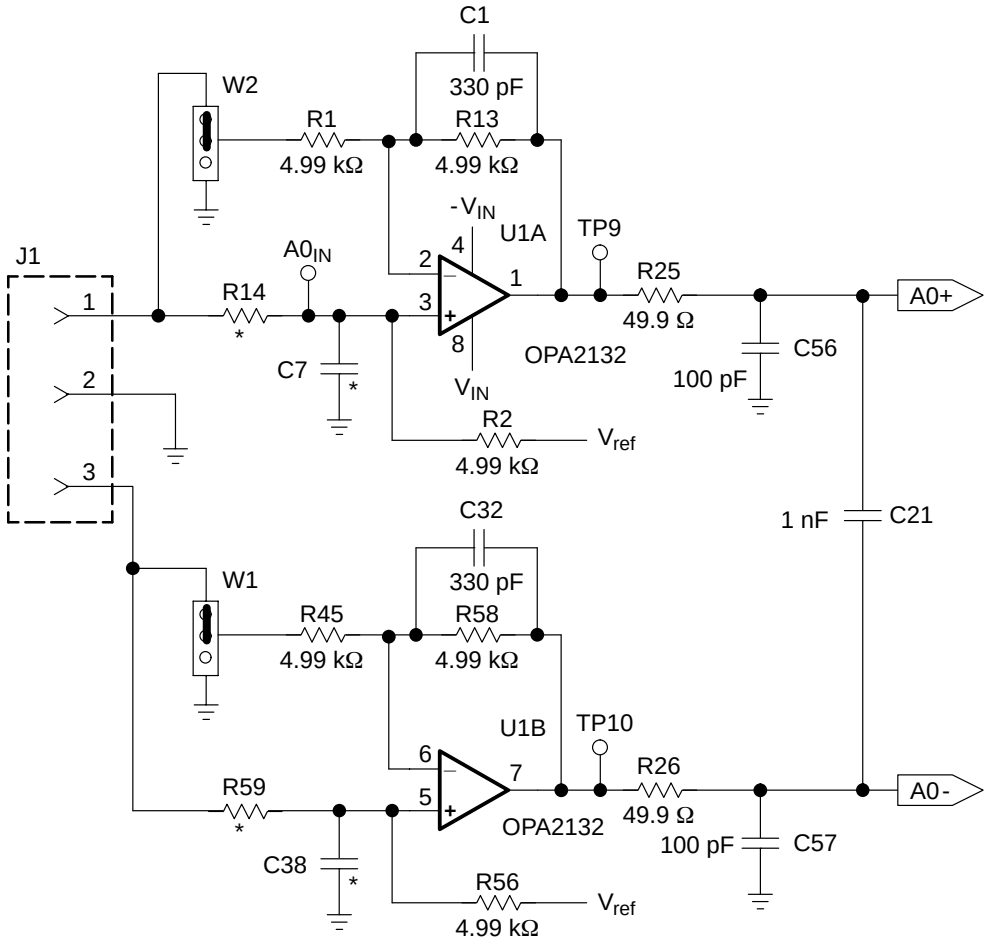
2.1 Dual Supply—Input Buffer

The analog input to the ADS8364EVM board is comprised of six independent OPA2132 operational amplifiers. The OPA2132s are powered from the ±12-V analog supply and connected as inverting amplifiers with a gain of 1. The internal 2.5-V reference voltage is applied to the noninverting input of the OPA2132s for level shifting.

Even though the ADS8364EVM board is configured at the factory for ±12-V analog operation, the EVM can tolerate maximum power supplies of ±15 VDC. However, care must be taken to ensure the ±15 VDC limit is not exceeded or potential damage to the op-amp circuits can occur.

Figure 2-1. ADS8364EVM Schematic—Analog Input Section



Note: Components marked with an asterisk (*) are NOT INSTALLED.

This configuration allows single-ended signals of ±2.5 V (5 V_{pp}) to be applied to either input of channels A, B, or C (JX pin 1 or 3 referenced to pin 2). Differential signal inputs of ±1.25 V (2.5 V_{pp}) can be applied to the channel input pairs (JX pin 1 and 3).

2.2 Bipolar Inputs

Table 2-1 lists various combinations of resistors, capacitors and jumpers. By changing components and setting the appropriate jumper, it is possible to adapt the input buffer to accept bipolar input voltages. Table 2-1 is related to the schematic presented in Table 2-1 and represents channel A0 of the ADC. Channels B0, C0, A1, B1, and C1 follow a similar placement pattern. Refer to the schematic at the end of this document for reference description details.

The capacitors C7, C38 and C1, C32 are used only in differential signal configurations. For single-ended signals, the second operational amplifier can be used to buffer the reference voltage to the input of A/D converter.

Table 2-1. Typical Analog Input Buffer Circuit Values (A0 Shown)

	Input Voltage	R14 R59	R1 R45	R2 R56	R13 R58	C7 C38	C1 C32	W2 W1
Refer to Figure 2-1	0-5	5 kΩ	open	open	short	330 pF	open	open
	0-2.5	5 kΩ	5 kΩ	open	5 kΩ	open	330 pF	1-2
	-2.5 -2.5	20 kΩ	4 kΩ	20 kΩ	4 kΩ	open	330 pF	1-2
	-5-5	20 kΩ	4 kΩ	10 kΩ	2 kΩ	open	330 pF	1-2
	-10-10	20 kΩ	4 kΩ	5 kΩ	1 kΩ	open	330 pF	1-2
	-5–0	open	5 kΩ	open	5 kΩ	short	330 pF	2-3
	0-5	open	5 kΩ	open	5 kΩ	short	330 pF	2-3

2.3 Analog and Digital 5-V Supplies

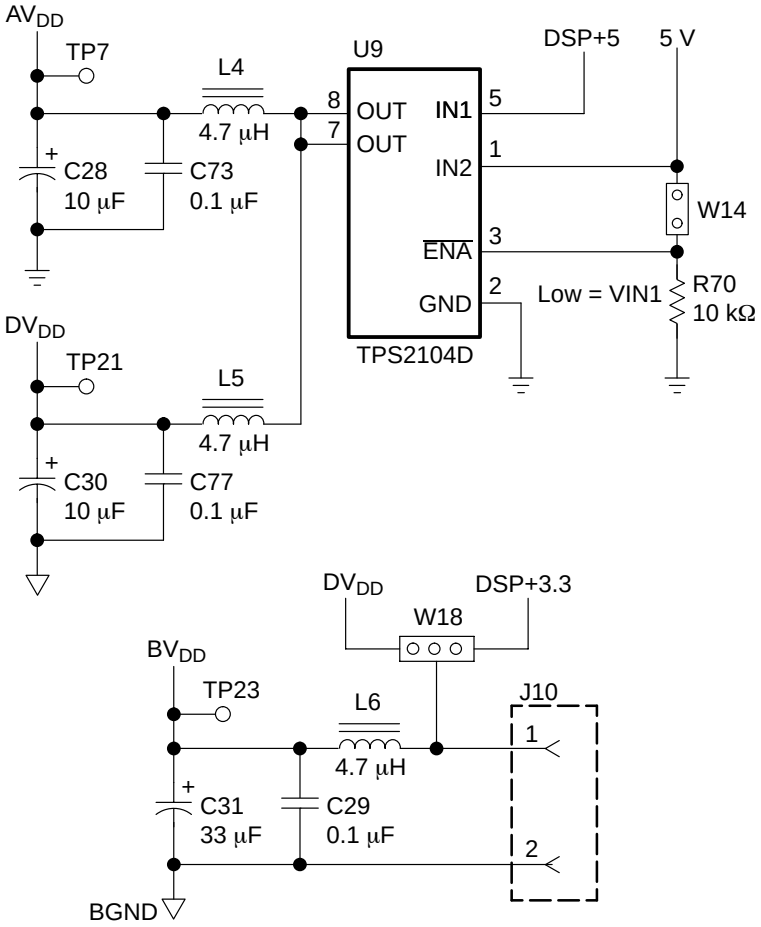
The ADS8364EVM board is configured at the factory for operation on the TMS320C6711 DSK platform. By default, W14 is open, which allows the DSP 5-V supply to be routed through U9 to the filter inductors L4 and L5. By closing W14, an external voltage source of 4.75 VDC to 5.25 VDC can be applied via J8.

2.4 Output Buffer 3.3-V Supply

As mentioned above, the ADS8364EVM board is configured at the factory for operation on the TMS320C6711 DSK platform. Since the interface to this DSP is 3.3 V, the buffer supply voltage is taken from the DSP 3.3-V source found on the interface connector at J11 (pins 41 and 42). The 3.3-V DSP supply is routed through the shunt jumper on W18 (pins 2-3). Placing the shunt on pins 1 and 2 supplys the 5-V digital source (via V9) to the buffer circuit.

The digital buffer circuit of the ADS8364 can also be powered from an external source via J10. When operated in this fashion, the shunt jumper at W18 should be completely removed in order to prevent possible damage to the EVM or DSK circuitry. The buffer voltage has a range of 2.7 VDC to 5.5 VDC maximum.

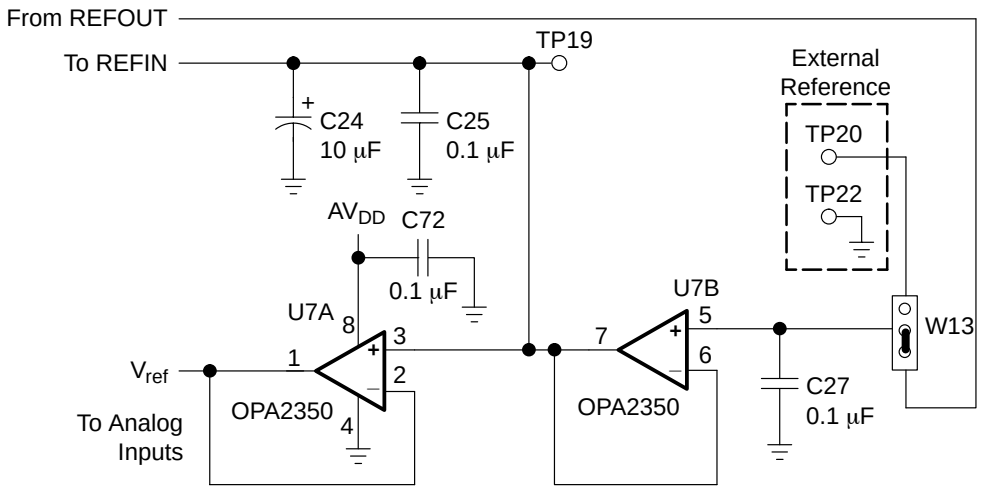
Figure 2-2. Digital Buffer Voltage Selection



2.5 Reference Voltage

The ADS8364 has an internal 2.5-V reference source, which is accessed by placing a shunt jumper on W13 pins 2 and 3 (factory default). If an external reference is desired, the shunt jumper on W13 must be moved to cover pins 1 and 2. The ADS8364EVM provides two test-points, TP20 and TP22, as a means to connect an external source. An external source should be applied to TP20, referenced to TP22. The voltage input range on this node is 1.5 VDC to 2.6 VDC. This voltage is buffered through the unity-gain noninverting buffer and fed to the REFIN pin as well as the analog input circuitry.

Figure 2-3. ADS8364EVM Reference Circuit



Chapter 3

Digital Interface

The ADS8364 EVM is designed for easy interfacing with the C5000 and C6000 series DSK platforms from Texas Instruments. Two 80-pin interface connectors located on the bottom side of the EVM allow direct plug-in to the DSK platforms.

If an alternate control system is desired, mating connector part numbers SFM-140-01-S-D or SFM-140-02-S-D can be used to wire the control and data signals. Please consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for price and availability of these connectors.

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3.2 Bus Width 3-2

3.3 External Clock 3-2

3.1 Control Signals

The ADS8364EVM was developed on the TMS320C6711 DSK platform. The HOLDx signals, ADD pin control, and reset are all derived from the GPIO function of McBSP port 1. These signals are located on J12. The address and data lines are available on J11. The EVM is factory configured to use address 0xA000 0020 as its base. Channel A0 can be accessed from this location, with channels A1 through C1 located at the base address + 0x04, as listed in Table 3-1.

An alternate address base can be selected by removing the shunt jumper on W17. This assigns A17 or 0xA002 0000 as the base address of the EVM. In this configuration, channels A1 through C1 are located at the base address + 0x4000.

Table 3-1. Address Map

	W17 CLOSED	W17 OPEN
A0	0xA000 0020	0xA002 0000
A1	0xA000 0024	0xA002 4000
B0	0xA000 0028	0xA002 8000
B1	0xA000 002C	0xA002 C000
C0	0xA000 0030	0xA003 0000
C1	0xA000 0034	0xA003 4000
Cycle	0xA000 0038	0xA003 8000
FIFO	0xA000 003C	0xA003 C000

3.2 Bus Width

The ADS8364 features a byte mode in which data can be read from the ADC in two consecutive 8-bit reads. W16 controls the byte feature, which is disabled by default. To enable byte mode, remove the jumper from W16. Please consult the data sheet for a complete description of byte mode operation.

3.3 External Clock

The BNC connector (J9) and W15 allow for the selection of an external conversion clock source. Factory default settings provide the clock source via the TOUT1 signal of the DSP by placing a shunt jumper on pins 1 and 2 of W15. By moving the shunt to pins 2 and 3, the EVM user can apply an external clock source of not more than 5 MHz to J9.

Chapter 4

Power Supply

The power supply requirements for the ADS8364EVM board can be split into three categories—analog front end, ADC power, and digital interface. While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

The power and ground planes on the inner layers of the EVM are split into digital and analog sections, with the ground planes tied together at a single point near the filter circuits.

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4.1 Analog Front-End Supply 4-2

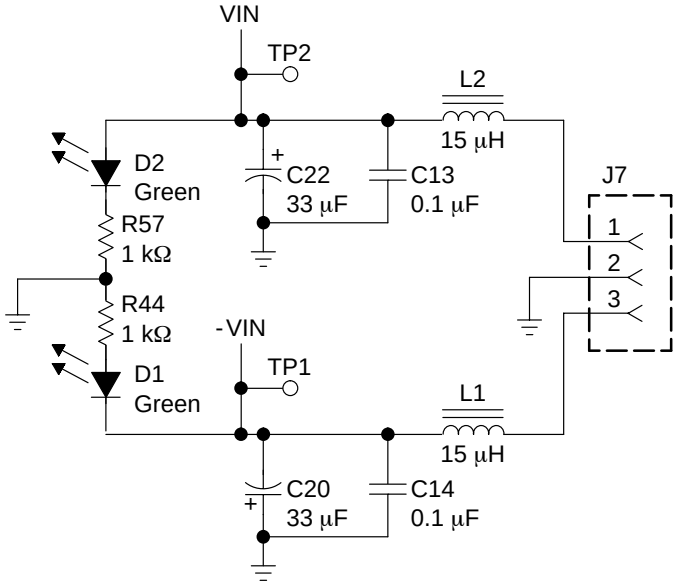
4.2 ADC Power Supply 4-3

4.3 Digital Interface Supply 4-4

4.1 Analog Front-End Supply

The analog front end of the EVM includes six OPA2132 operational amplifiers. These amplifiers are powered through J7 and are configured for bipolar operation. The circuits are designed to operate from a maximum supply voltage of ±12 VDC. Single supply operation can be achieved by applying a positive dc voltage to pin 1 of J7 (marked as +12 V on EVM) while applying a ground reference to both pins 2 and 3.

Figure 4-1. Analog Front-End Supply

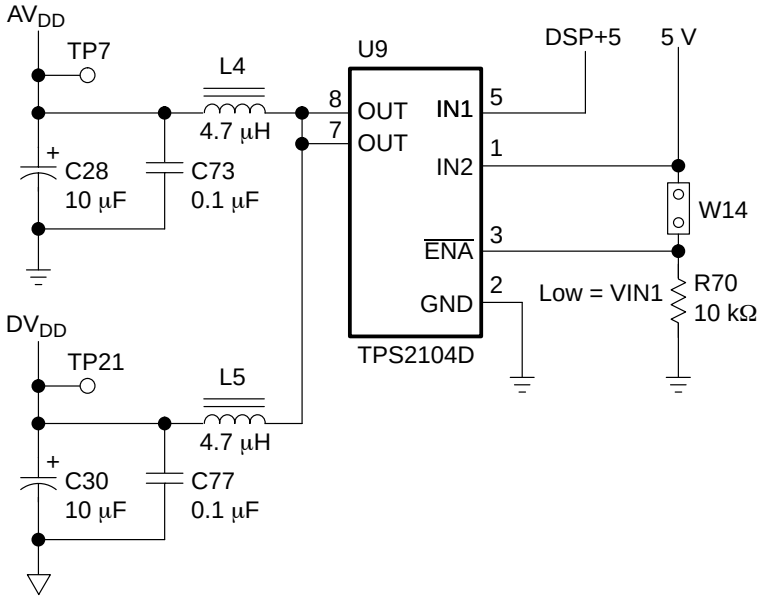


4.2 ADC Power Supply

The ADS8364 requires analog and digital supplies in the range of 4.75 VDC to 5.25 VDC. The EVM provides both analog and digital supply voltages through a single input supply source. The 5-V input supply is filtered and split into the digital and analog power planes located on the inner layer of the PCB.

W14 can be used to determine the source of the input supply. With W14 closed, the 5-V ADC power supply source is located at J8. The TPS2104 power switch at U9 directs the voltage from J8 to the analog/digital filters. With W14 open, the TPS2104 power switch directs 5-V power from the C5000/C6000 DSK board via J12, which is the factory default setting.

Figure 4-2. ADC Power-Supply Input



4.3 Digital Interface Supply

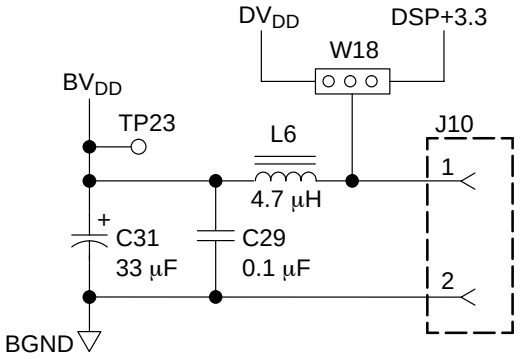
A unique feature of the ADS8364 is the built-in data buffer circuit with an independent power source. The EVM provides a jumper—W18, which allows for flexible voltage selection. When the shunt at W18 is in the factory default position (W18 pins 2 and 3 shorted), the 3.3-V DSP supply taken from J11 is applied to the BV_{DD} pins of the ADS8364. By moving the shunt jumper on W18 to pins 1 and 2, the user chooses the 5-V ADC supply as the source of the BV_{DD} voltage.

J10 provides a means of supplying an alternative independent buffer voltage. If desired, the shunt jumper at W18 can be totally removed, and a dc source of 2.7 V to 5.25 V can be applied to J10 as a means to provide BV_{DD} power.

Caution

While J10 is used, ensure that W18 remains completely open.

Figure 4-3. Digital Buffer Alternate Supply Input



Chapter 5

Initial Setup of the Board

Factory set up of the board is for a ±5-V to ±12-V analog front-end supply at J7, and 5-V ADC power provided through J8. The BV_{DD} supply is provided from the DSK platform via J11 and W18 (pins 2 and 3 shorted). The maximum analog inputs are 0-V/5-V for a differential signal. The reference circuit is connected to the internal reference of the ADC (W13 pins 2 and 3 shorted).

Table 5-1. Factory Defaults—Analog Input Buffers (A0 Shown)

Refer to Figure 2-1 and Schematic	Input Voltage	R14 R59	R1 R45	R2 R56	R13 R58	C7 C38	C1 C32	W2 W1
	0-5	open	4.99 kΩ	4.99 kΩ	4.99 kΩ	N/I	330 pF	1-2

The analog inputs to the ADS8364EVM board can be applied to any one or all of the input channels. Single-ended inputs are to be applied between analog ground (center terminal of J1–J6) and either the positive or negative terminals. Differential signals are to be applied between the positive and negative terminals.

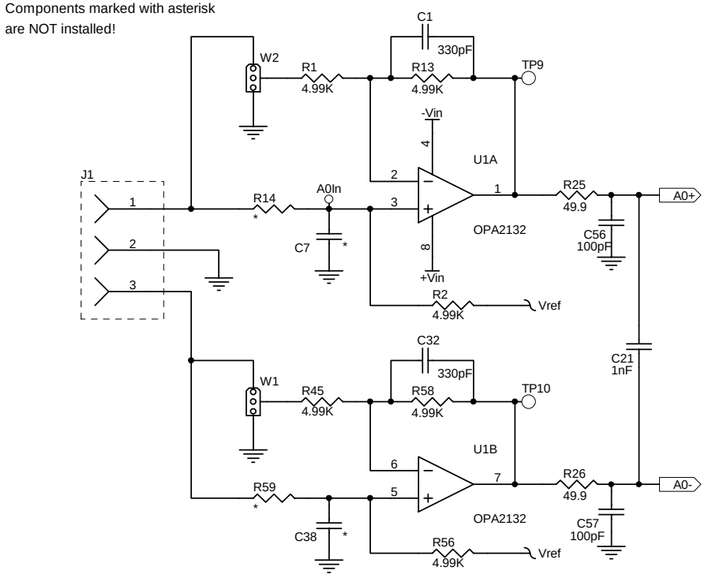
Chapter 6

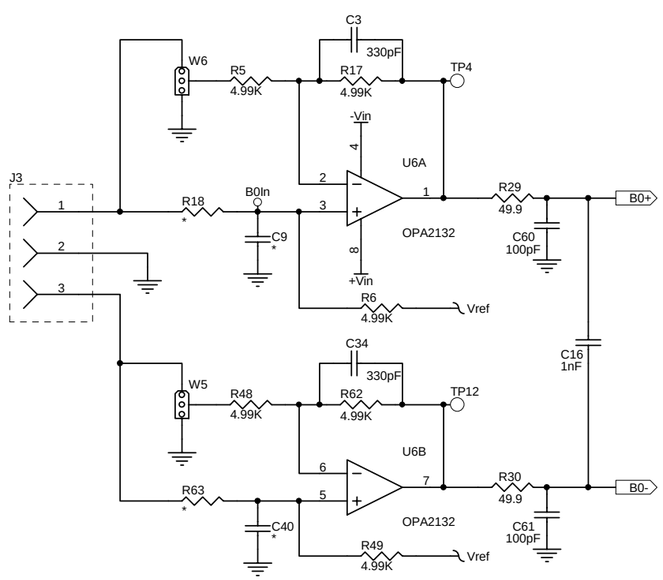
EVM Schematic

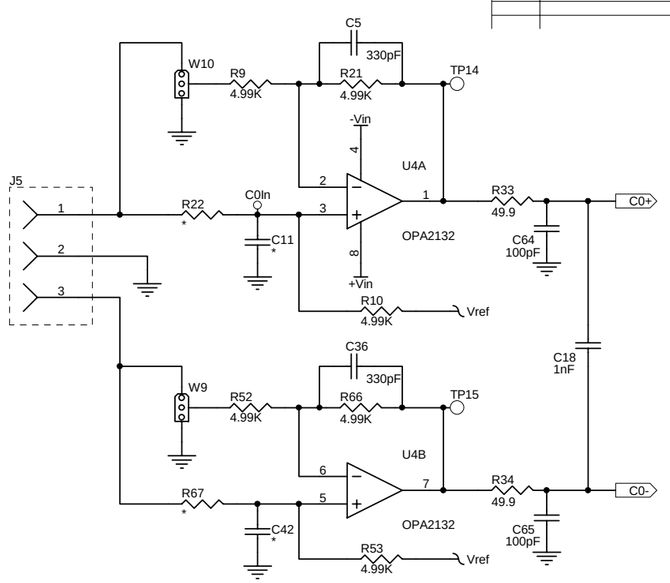
The following pages contain the ADS8364EVM circuit diagram.

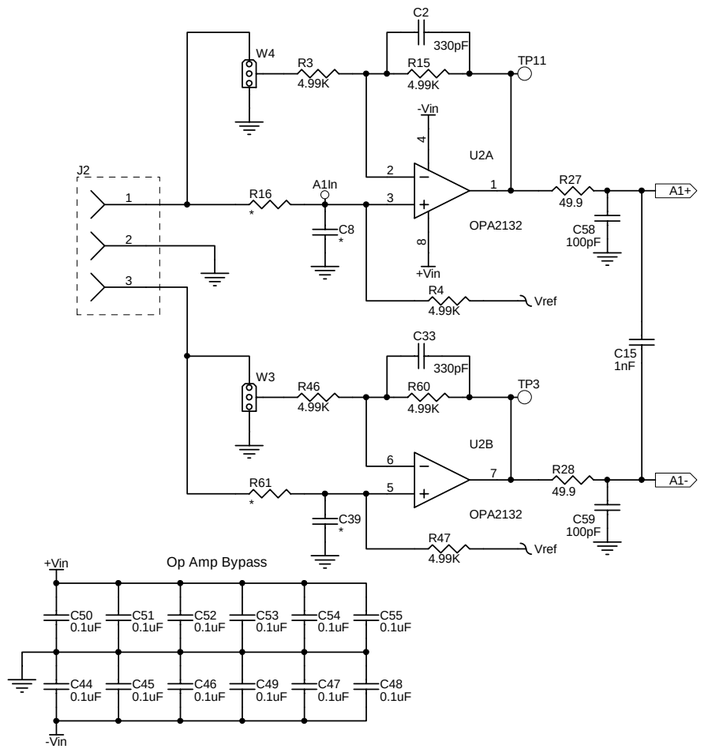
Note:
Components marked with asterisk
are NOT installed!

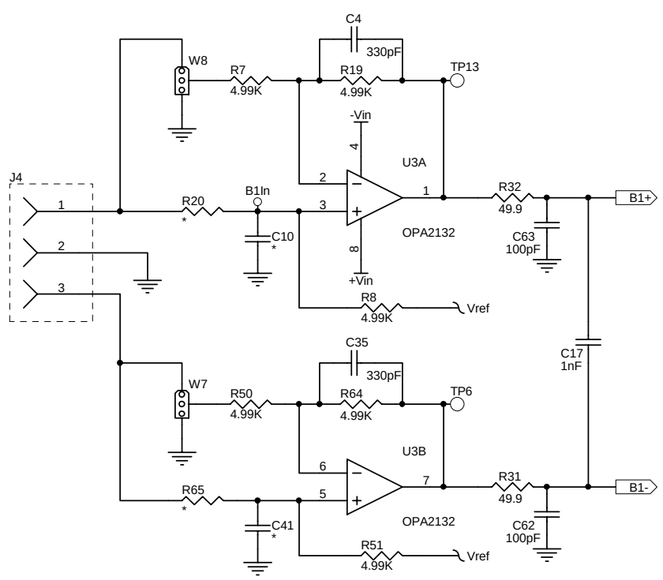
Revision History		
REV	ECN Number	Approved

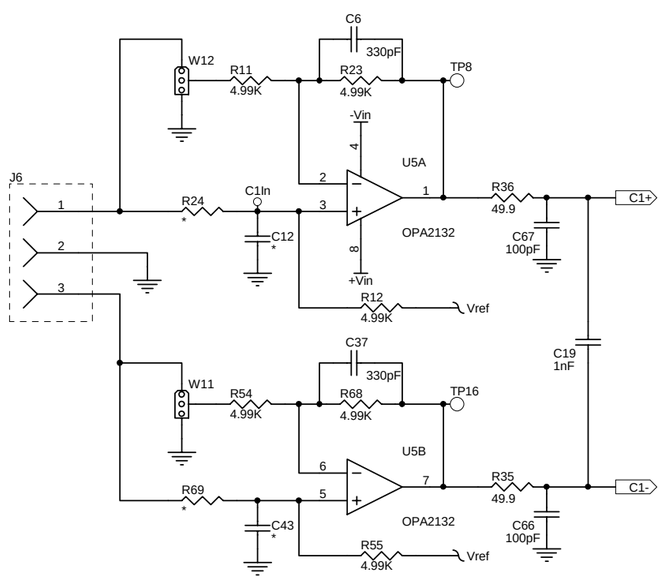












t i

12500 TI Boulevard. Dallas, Texas 75243

Title: ADS8364 Evaluation Module

Engineer: Tom Hendrick			
Drawn By: Tom Hendrick	SIZE: B	DATE: 30-Jan-2002	REV: A
FILE: ADS8364_A_SH1.Sch			SHEET: 1 OF: 3

ADC Bypass

BVdd C74 0.1uF C75 0.1uF
DVdd C76 0.1uF
AVdd C68 0.1uF C69 0.1uF C70 0.1uF C71 0.1uF

U8 ADS8364

AVdd (3, 8, 13, 59) DVdd (22) BVdd (24, 50)

A0+ (63) A0- (64)
A1- (1) A1+ (2)
A_REF (5)
B0+ (6) B0- (7)
B1- (11) B1+ (12)
B_REF (10)
C0+ (16) C0-
C1- (18) C1+ (19)
C_REF (15)
REFIN (62)
REFOUT (61)

CLK (28) — CLK — TP35
RESET# (51) — RESET# — TP28 — DC_TOUT0 — W15 — J9
ADD (52) — ADD
A2 (53) — A2
A1 (54) — A1
A0 (55) — A0
HOLD_A# (56) — HOLD_A#
HOLD_B# (57) — HOLD_B#
HOLD_C# (58) — HOLD_C#
FD (26) — FD — TP24
EOC# (27) — DC_INTa
RD# (29) — DC_ARE# — TP31 TP29
WR# (30) — DC_AWE
CS# (31) — CS# — TP32 TP34
D0 (48) — DC_D0
D1 (47) — DC_D1
D2 (46) — DC_D2
D3 (45) — DC_D3
D4 (44) — DC_D4
D5 (43) — DC_D5
D6 (42) — DC_D6
D7 (41) — DC_D7
D8 (40) — DC_D8
D9 (39) — DC_D9
D10 (38) — DC_D10
D11 (37) — DC_D11
D12 (36) — DC_D12
D13 (35) — DC_D13
D14 (34) — DC_D14
D15 (33) — DC_D15
BYTE (23) — R43 10K — BVdd — W16

AGND (4, 9, 14, 60) DGND (21) BGND (25, 49)

R71 49.9

TP19
C24 10uF C25 0.1uF
AVdd
C72 0.1uF
U7A (8) U7B (7)
Vref (1)
OPA2350 (3, 2, 4) OPA2350 (5, 6)
EXT. REF. TP20 TP22
W13
C27 0.1uF

J11

	1	2	
	3	4	
	5	6	
DC_A17	7	8	DC_A16
DC_A15	9	10	DC_A14
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
DC_A5	23	24	DC_A4
DC_A3	25	26	DC_A2
	27	28	
	29	30	
DSP+3.3	31	32	DSP+3.3
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	
	51	52	
DC_D15	53	54	DC_D14
DC_D13	55	56	DC_D12
DC_D11	57	58	DC_D10
DC_D9	59	60	DC_D8
	61	62	
DC_D7	63	64	DC_D6
DC_D5	65	66	DC_D4
DC_D3	67	68	DC_D2
DC_D1	69	70	DC_D0
	71	72	
DC_ARE#	73	74	DC_AWE
	75	76	
	77	78	DC_CSa#
	79	80	

DSP+5 DSP+12 DSP-12 DSP+5

J12

	1	2	
	3	4	
	5	6	
	7	8	
	9	10	
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
ADD	33	34	
HOLD_B#	35	36	RESET#
	37	38	
HOLD_A#	39	40	
HOLD_C#	41	42	FD
	43	44	
DC_TOUT0	45	46	
R73 49.9	47	48	
	49	50	
DC_INTa	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	
	75	76	
	77	78	
	79	80	

McBSP 1 Setup

ADD = CLKX1 (GP OUT)
HOLD A# = CLKR1 (GP OUT)
HOLD B# = FSX1 (GP OUT)
HOLD C# = FSR1 (GP OUT)
RESET# = DX1 (GP OUT)
FD = DR1 (GP IN)

BVdd U10 SN74CBT3257PWR (16)

DC_A2	2	1B1	1A	4 — TP25 — A0
DC_A14	3	1B2		
DC_A3	5	2B1	2A	7 — TP26 — A1
DC_A15	6	2B2		
DC_A4	11	3B1	3A	9 — TP27 — A2
DC_A16	10	3B2		
DC_A5	14	4B1	4A	12
DC_A17	13	4B2		
DC_CSa# — TP36	15	/OE	S	1

BVdd (8) C78 0.1uF

BVdd R42 10K R41 10K R40 10K R39 10K R38 10K

W17

BVdd U11 (5, 2, 4, 3) SN74AHC1G04 — CS#

Engineer:	Tom Hendrick
Drawn By:	Tom Hendrick
FILE:	

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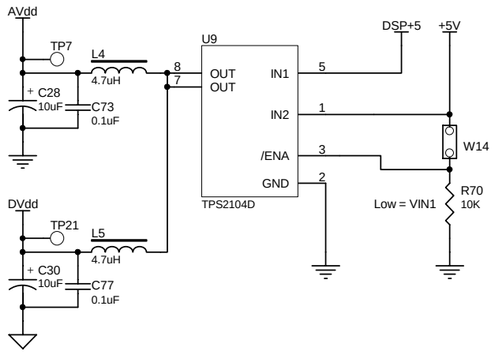
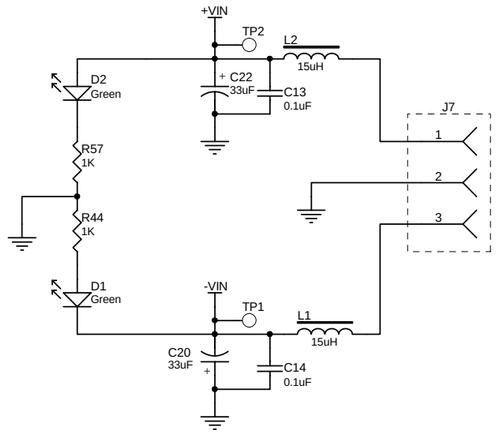
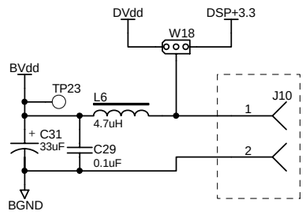
12500 TI Boulevard. Dallas, Texas 75243

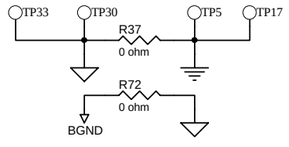
Title: ADS8364 Evaluation Module

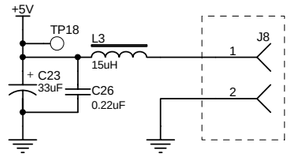
SIZE: B | DATE: 30-Jan-2002 | REV: A | SHEET: 2 OF: 3











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