

(iShynx II) 1394 Integrated PHY and Link-Layer Controller for SBP-2 Products and DPP Products

FEATURES

- IEEE 1394a-2000 Compliant
- Single 3.3-V Supply
- Internal 1.8-V Circuit to Reduce Power Consumption
- Integrated 400-Mbps Two-Port Physical Layer (PHY)
- Internal Voltage Regulator
- IEEE 1394 Related Functions:
 - Automated Read Response for ConfigROM Register Access
 - Automated Single Retry Protocol and Split Transaction Control
- SBP-2 Related Functions:
 - Supports Four Initiators by Automated Transactions and More Can Be Supported Through Firmware.
 - Automated Management ORB Fetching
 - Automated Linked Command ORB Fetching
 - Automated PageTable Fetching
 - Automated Status Block Transmit
- Ability to Support Direct Print Protocol (DPP) Mode
- Data Transfers:
 - Auto Address Increment of Direct/Indirect Addressing on Data Transfer (Packetizer)
 - Automated Header Insert/Strip for DMA Data Transfers
 - 8-/16-Bit Asynchronous and Synchronous DMA I/F With Handshake and Burst Mode
 - Supports ATAPI (Ultra-DMA) Mode and SCSI Mode
 - 8-/16-Bit Data/Address Multiplex Microcontroller and 8-/16-Bit Separated Data/Address Bus
 - Three FIFO Configurations That Support High Performance for the DMA and for Command Exchanges
 - Asynchronous Command FIFO: 1512 Bytes
 - Config ROM/LOG FIFO: 504 Bytes
 - DMA FIFO: 4728 Bytes
- Multiple Package Options:
 - PGE Dual 1394 Port Package, 144-Terminal Plastic Quad Flatpack
 - GGW Commercial Dual 1394 Port Package, 176-Terminal BGA
 - GGW Industrial Dual 1394 Port Package (TSB43AA82I), 176-Terminal BGA With Operational Range From –40°C to 85°C

DESCRIPTION

The TSB43AA82 is a high performance 1394 integrated PHY and link layer controller. It is compliant with the IEEE 1394-1995 and IEEE 1394a-2000 specifications and supports asynchronous transfers.

TSB43AA82 has a generic 16-/8-bit host bus interface. It supports parallel or multiplexed connections to the microcontroller (MCU) at rates up to 40 MHz.

The TSB43AA82 offers large data transfers with three mutually independent FIFOs: 1) the asynchronous command FIFO with 1512 Bytes, 2) the DMA FIFO with 4728 bytes and 3) the Config ROM/LOG FIFO with 504 bytes.



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The features of the TSB43AA82 support the serial bus protocol 2 (SBP-2). It handles up to four initiators with the SBP-2 transaction/timer manager. This SBP-2 transaction engine supports fully automated operation request block (ORB) fetches and fully automated memory page table fetches for both read and write transactions. Automated responses to other node requests are provided; this includes responding to another node's read request to the Config ROM and issuing ack_busy_X for a single retry. Various control registers enable the user to program IEEE 1394 asynchronous transaction settings. The user can program the number of retries and the split transaction time-out value by setting the time limit register in the CFR.

The TSB43AA82 also supports the direct print protocol (DPP). The asynchronous receive FIFO (ARF) in the TSB43AA82 is large enough to satisfy the connection register area, the DRF receiving FIFO can be used as the segment data unit (SDU) register to fulfill the large data transfer.

This document is not intended to serve as a tutorial on IEEE 1394; users are referred to IEEE Std 1394-1995 and IEEE 1394a-2000⁽¹⁾.

NOTE:

This product is for high-volume CE applications only. For a complete datasheet or more information contact support@ti.com.

- (1) IEEE Std 1394-1995, *IEEE Standard for a High Performance Serial Bus*
IEEE Std 1394a-2000, *IEEE Standard for a High Performance Serial Bus – Amendment 1*

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TSB43AA82GGW	ACTIVE	BGA MI CROSTAR	GGW	176		TBD	Call TI	Call TI
TSB43AA82GHH	OBSOLETE	BGA	GHH	179		TBD	Call TI	Call TI
TSB43AA82IGGW	ACTIVE	BGA MI CROSTAR	GGW	176		TBD	Call TI	Call TI
TSB43AA82PGE	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TSB43AA82PGE4	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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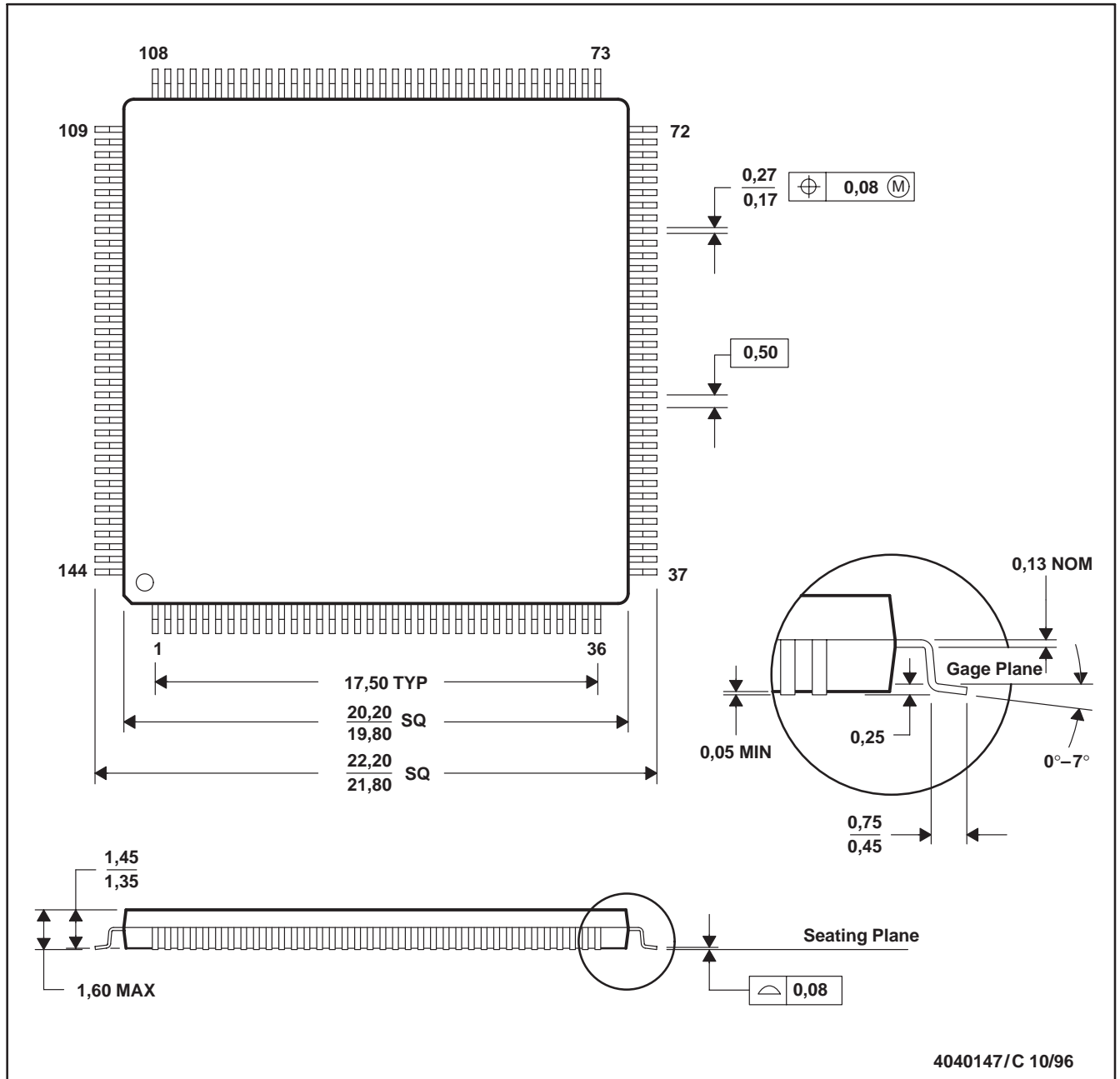
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PGE (S-PQFP-G144)

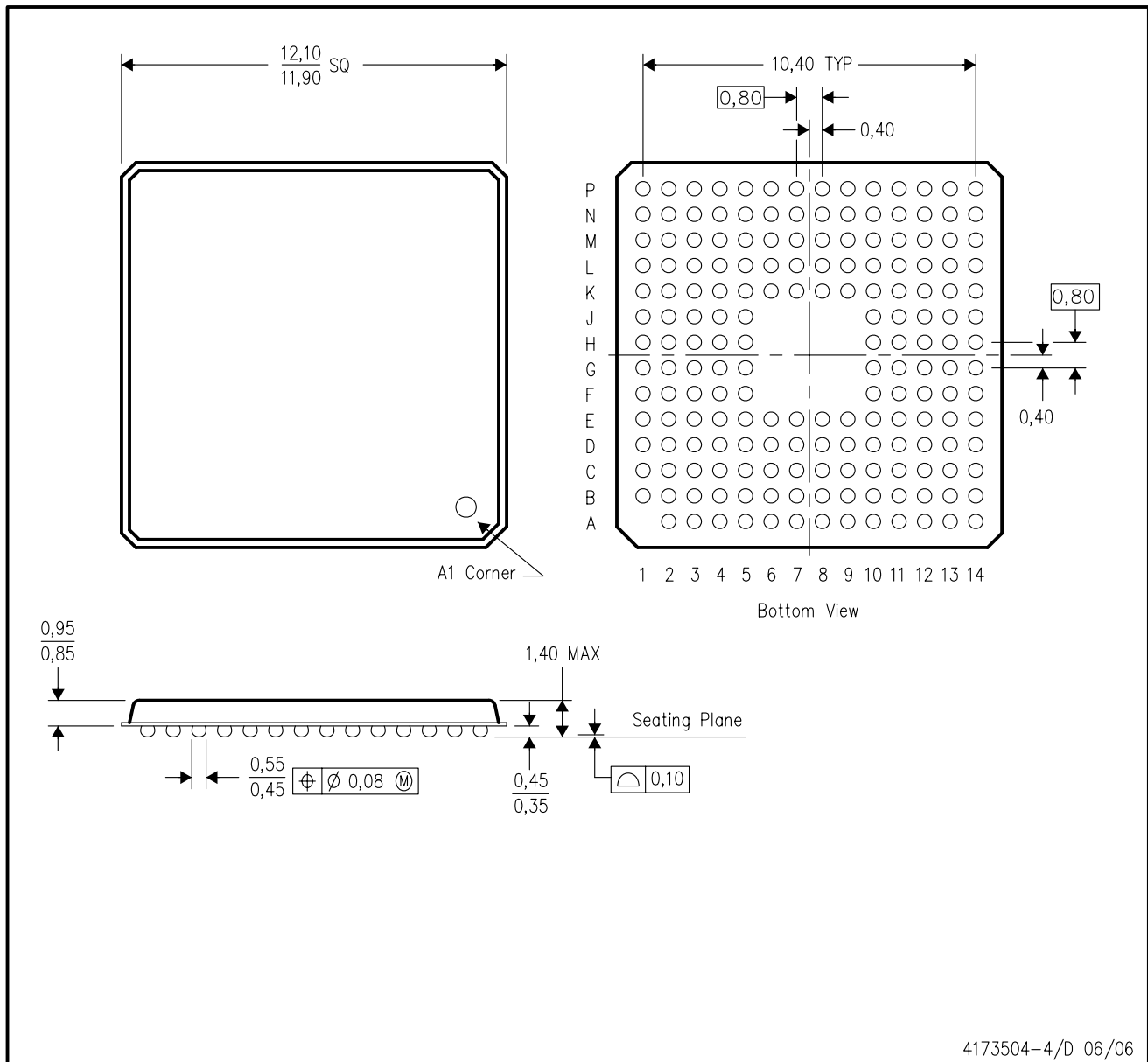
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

GHH (S-PBGA-N179)

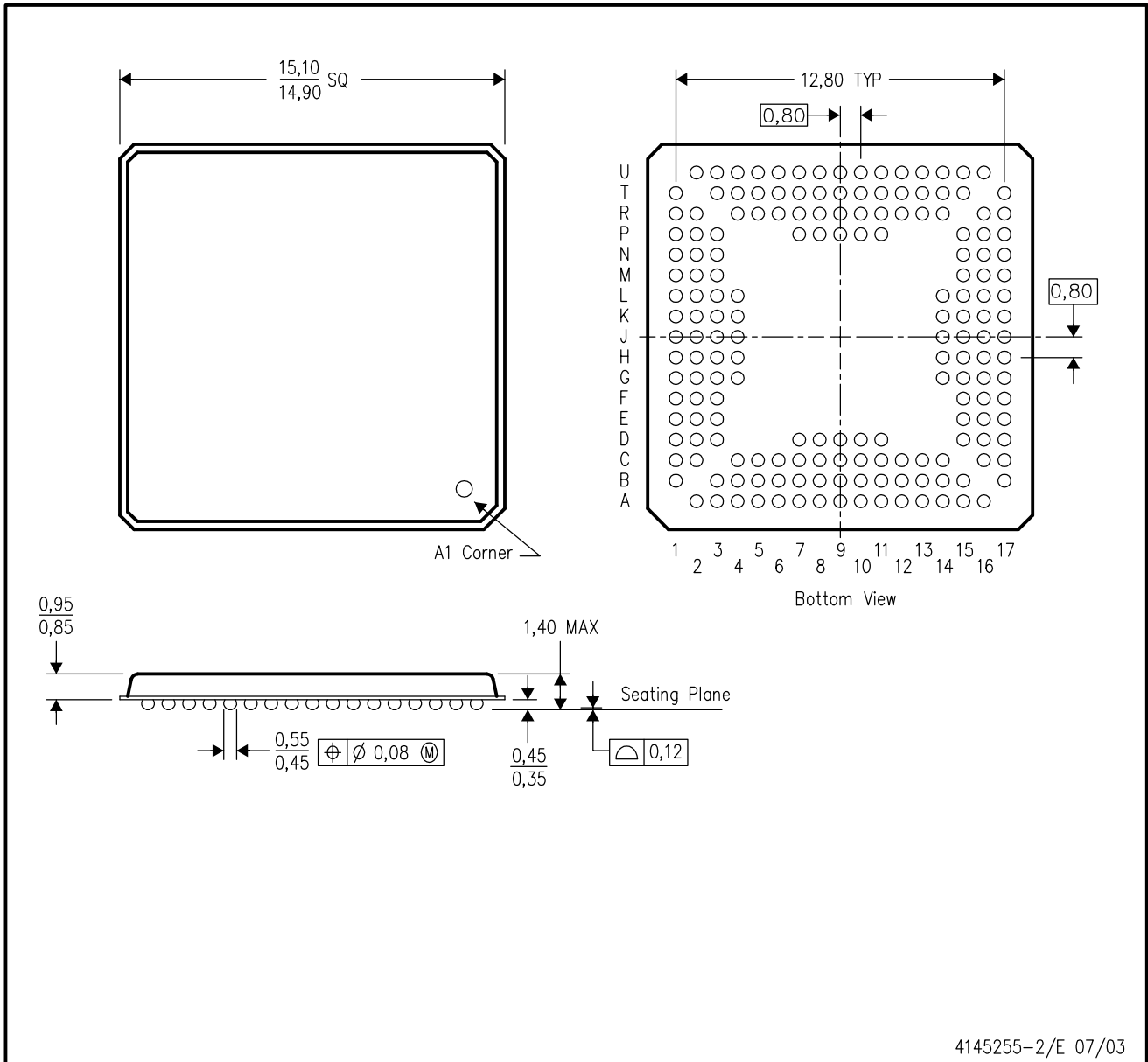
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Micro Star BGA configuration

GGW (S-PBGA-N176)

PLASTIC BALL GRID ARRAY



- NOTES:
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