

# Regulating Pulse Width Modulator

## FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600kHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation ( $V_{IN} = V_C = V_{REF} = 5.0V$ )

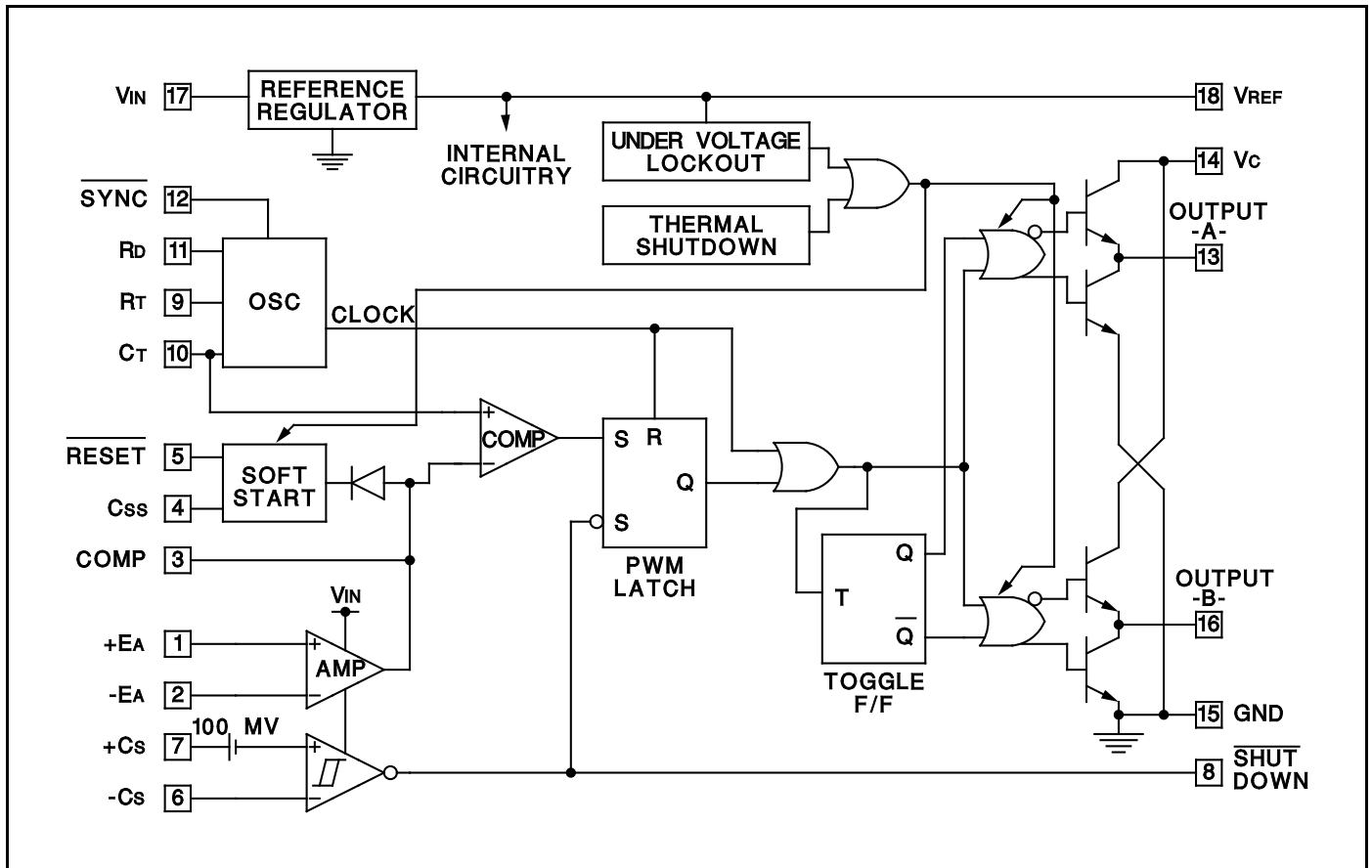
## DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non- "A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting  $V_{IN}$ ,  $V_C$  and  $V_{REF}$  to a precision 5V input supply. Consult factory for additional information.

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (Note 1, 2)

Input Voltage (+VIN) . . . . .	+40V
Collector Supply Voltage (+Vc) . . . . .	+40V
Logic Inputs . . . . .	-0.3V to +5.5V
Analog Inputs . . . . .	-0.3V to +VIN
Source/Sink Load Current (each output) . . . . .	200mA
Reference Load Current . . . . .	50mA
Logic Sink Current . . . . .	15mA
Power Dissipation at TA = +25°C (Note 2) . . . . .	1000mW
Power Dissipation at Tc = +25°C (Note 2) . . . . .	3000mW
Operating Junction Temperature . . . . .	+150°C
Storage Temperature Range . . . . .	-65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . .	+300°C

Note 1: Values beyond which damage may occur.  
 Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

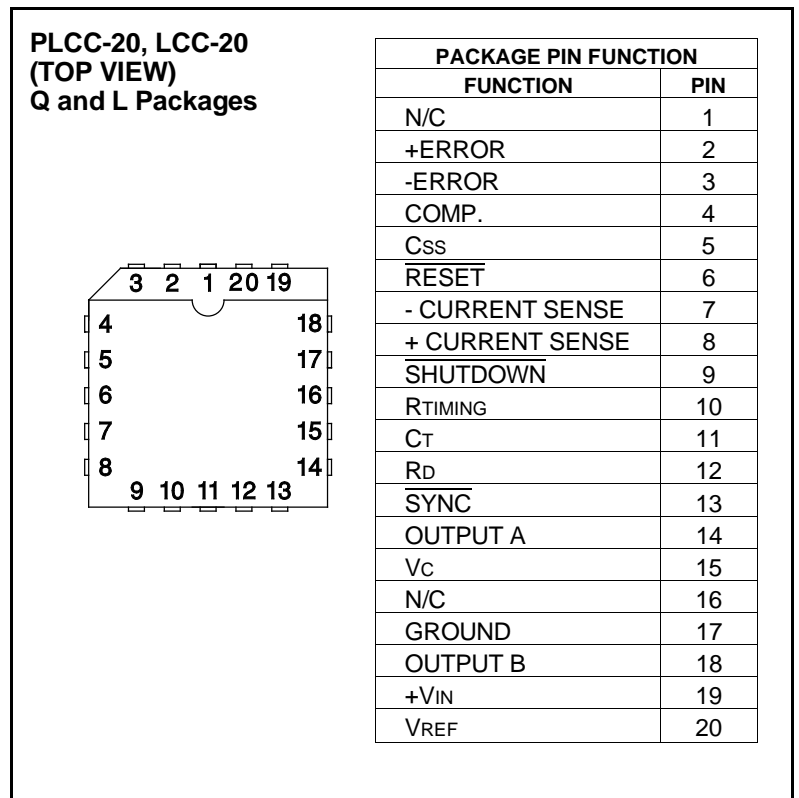
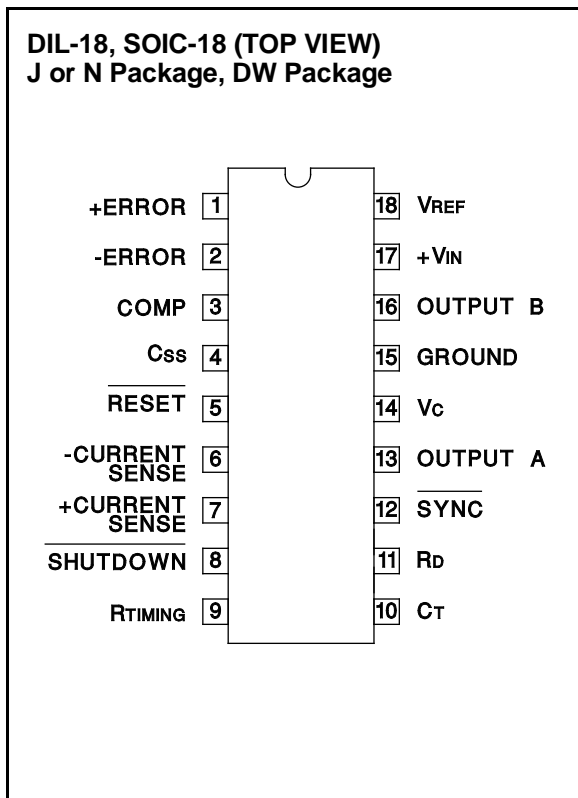
**RECOMMENDED OPERATING CONDITIONS**

(Note 3)

Input Voltage . . . . .	+7V to +35V
Collector Supply Voltage . . . . .	+4.5V to +35V
Sink/Source Load Current (each output) . . . . .	0 to 100mA
Reference Load Current . . . . .	0 to 20mA
Oscillator Frequency Range . . . . .	1Hz to 600kHz
Oscillator Timing Resistor . . . . .	2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . .	400pF to 20μF
Available Deadtime Range at 40kHz . . . . .	1% to 50%
Operating Ambient Temperature Range	
UC1526A . . . . .	-55°C to +125°C
UC2526A . . . . .	-25°C to +85°C
UC3526A . . . . .	0°C to +70°C

Note 3: Range over which the device is functional and parameter limits are guaranteed.

**CONNECTION DIAGRAMS**



**ELECTRICAL CHARACTERISTICS:** +V<sub>IN</sub> = 15V, and over operating ambient temperature, unless otherwise specified T<sub>A</sub> = T<sub>J</sub>.

PARAMETER	TEST CONDITIONS	UC1526A / UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section (Note 4)</b>								
Output Voltage	T <sub>J</sub> = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V <sub>IN</sub> = 7 to 35V		2	10		2	15	mV
Load Regulation	I <sub>L</sub> = 0 to 20mA		5	20		5	20	mV
Temperature Stability	Over Operating T <sub>J</sub> (Note 5)		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V <sub>REF</sub> = 0V	25	50	100	25	50	100	mA
<b>Under-Voltage Lockout</b>								
RESET Output Voltage	V <sub>REF</sub> = 3.8V		0.2	0.4		0.2	0.4	V
	V <sub>REF</sub> = 4.7V	2.4	4.7		2.4	4.8		V
<b>Oscillator Section (Note 6)</b>								
Initial Accuracy	T <sub>J</sub> = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V <sub>IN</sub> = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T <sub>J</sub> (Note 5)		2	6		1	3	%
Minimum Frequency	R <sub>T</sub> = 150kΩ, C <sub>T</sub> = 20μF (Note 5)			1			1	Hz
Maximum Frequency	R <sub>T</sub> = 2kΩ, C <sub>T</sub> = 470pF	550			650			kHz
Sawtooth Peak Voltage	+V <sub>IN</sub> = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V <sub>IN</sub> = 7V	0.5	1.0		0.5	1.0		V
SYNC Pulse Width	T <sub>J</sub> = 25°C, R <sub>L</sub> = 2.7kΩ to V <sub>REF</sub>		1.1			1.1		μs
<b>Error Amplifier Section (Note 7)</b>								
Input Offset Voltage	R <sub>S</sub> ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R <sub>L</sub> ≥ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	V <sub>PIN 1</sub> - V <sub>PIN 2</sub> ≥ 150mV, I <sub>SOURCE</sub> = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	V <sub>PIN 2</sub> - V <sub>PIN 1</sub> ≥ 150mV, I <sub>SINK</sub> = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R <sub>S</sub> ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V <sub>IN</sub> = 12 to 18V	66	80		66	80		dB
<b>PWM Comparator (Note 6)</b>								
Minimum Duty Cycle	V <sub>COMPENSATION</sub> = +0.4V			0			0	%
Maximum Duty Cycle	V <sub>COMPENSATION</sub> = +3.6V	45	49		45	49		%
<b>Digital Ports (SYNC, SHUTDOWN, and RESET)</b>								
HIGH Output Voltage	I <sub>SOURCE</sub> = 40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I <sub>SINK</sub> = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V <sub>IH</sub> = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V <sub>IL</sub> = +0.4V		-225	-360		-225	-360	μA
Shutdown Delay	From Pin 8, T <sub>J</sub> = 25°C		160			160		ns
<b>Current Limit Comparator (Note 8)</b>								
Sense Voltage	R <sub>S</sub> ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Shutdown Delay	From pin 7, 100mV Overdrive, T <sub>J</sub> = 25°C		260			260		ns

Note 4: I<sub>L</sub> = 0mA.

Note 5: Guaranteed by design, not 100% tested in production.

Note 6: F<sub>OSC</sub> = 40kHz, (R<sub>T</sub> = 4.12kΩ ± 1%, C<sub>T</sub> = 0.01μF ± 1%, R<sub>D</sub> = 0Ω).

Note 7: V<sub>CM</sub> = 0 to +5.2V

Note 8: V<sub>CM</sub> = 0 to +12V.

Note 9: V<sub>C</sub> = +15V.

Note 10: V<sub>IN</sub> = +35V, R<sub>T</sub> = 4.12kΩ.

**ELECTRICAL CHARACTERISTICS:** +VIN = 15V, and over operating ambient temperature, unless otherwise specified TA = TJ.

PARAMETER	TEST CONDITIONS	UC1526A UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Soft-Start Section</b>								
Error Clamp Voltage	$\overline{\text{RESET}} = +0.4\text{V}$		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{\text{RESET}} = +2.4\text{V}$	50	100	150	50	100	150	$\mu\text{A}$
<b>Output Drivers (Each Output) (Note 9)</b>								
HIGH Output Voltage	ISOURCE = 20mA	12.5	13.5		12.5	13.5		V
	ISOURCE = 100mA	12	13		12	13		V
LOW Output Voltage	ISINK = 20mA		0.2	0.3		0.2	0.3	V
	ISINK = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	VC = 40V		50	150		50	150	$\mu\text{A}$
Rise Time	CL = 1000pF (Note 5)		0.3	0.6		0.3	0.6	$\mu\text{s}$
Fall Time	CL = 1000pF (Note 5)		0.1	0.2		0.1	0.2	$\mu\text{s}$
Cross-Conduction Charge	Per cycle, TJ = 25°C		8			8		nC
<b>Power Consumption (Note 10)</b>								
Standby Current	$\overline{\text{SHUTDOWN}} = +0.4\text{V}$		14	20		14	20	mA

Note 4:  $I_L = 0\text{mA}$ .

Note 5: Guaranteed by design, not 100% tested in production.

Note 6:  $F_{\text{osc}} = 40\text{kHz}$ , ( $R_T = 4.12\text{k}\Omega \pm 1\%$ ,  $C_T = 0.01\mu\text{F} \pm 1\%$ ,  $R_D = 0\Omega$ ).

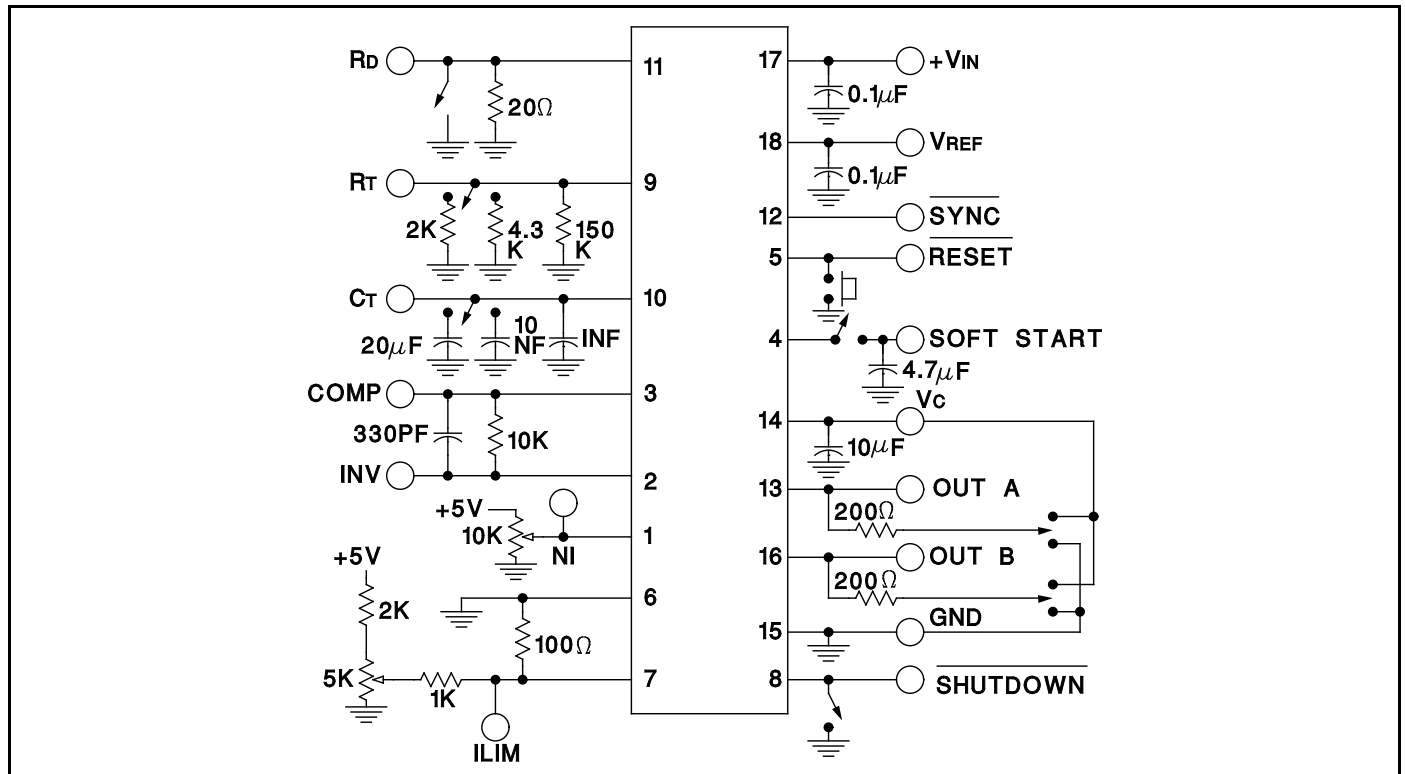
Note 7:  $V_{\text{CM}} = 0$  to  $+5.2\text{V}$

Note 8:  $V_{\text{CM}} = 0$  to  $+12\text{V}$ .

Note 9:  $V_C = +15\text{V}$ .

Note 10:  $V_{\text{IN}} = +35\text{V}$ ,  $R_T = 4.12\text{k}\Omega$ .

### Open Loop Test Circuit UC1526A



## APPLICATIONS INFORMATION

### Voltage Reference

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to  $\pm 1\%$  accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

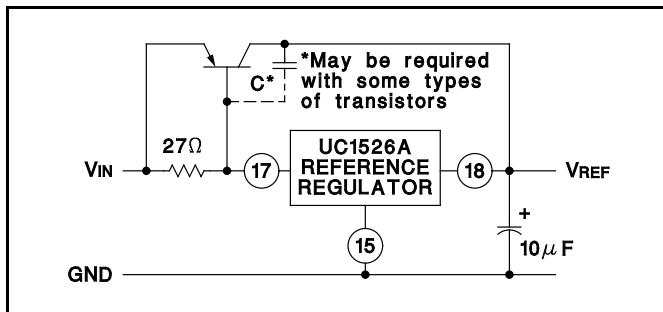


Figure 1. Extending Reference Output Current

### Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage. If +VIN is too low, the circuit disables the output drivers and holds the RESET pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to  $3V_{BE}$  or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the RESET pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls RESET LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

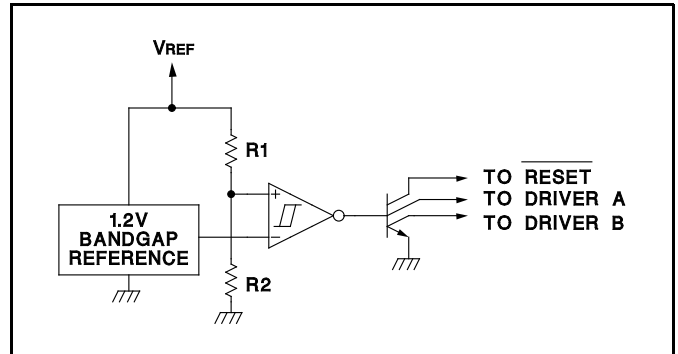


Figure 2. Under-Voltage Lockout Schematic

### Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds RESET LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, RESET will go HIGH. Q1 turns off, allowing the internal 100µA current source to charge Cs. Q2 clamps the error amplifier output to  $1V_{BE}$  above the voltage on Cs. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

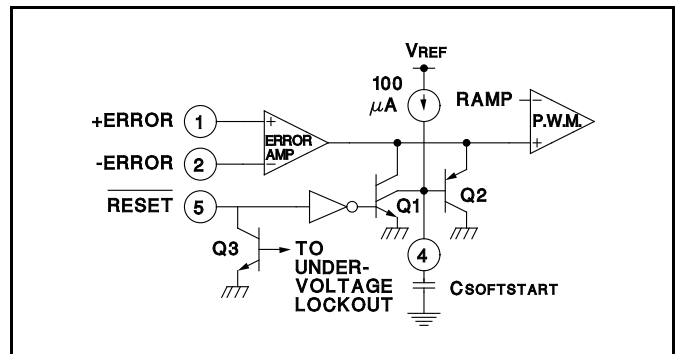


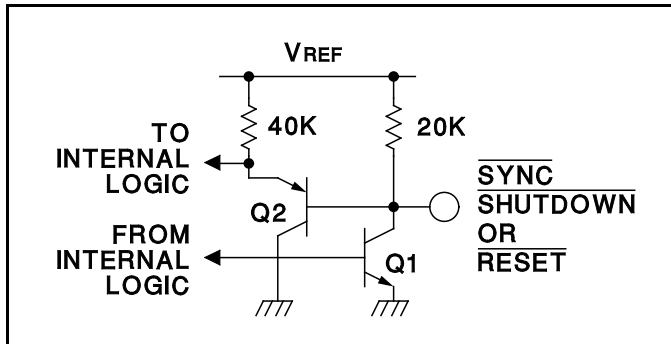
Figure 3. Soft-Start Circuit Schematic

### Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving SYNC LOW initiates a discharge cycle in the oscillator. Pulling SHUTDOWN LOW immediately inhibits all PWM output pulses. Holding RESET LOW discharges the soft-start

**APPLICATIONS INFORMATION (cont.)**

capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.



**Figure 4. Digital Control Port Schematic**

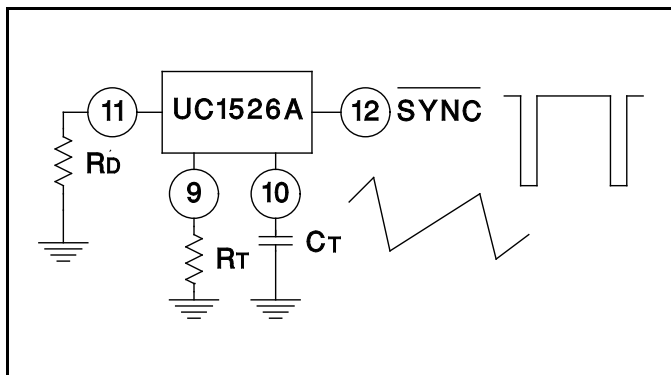
**Oscillators**

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD= 0Ω (pin 11 shorted to ground) select values for RT and CT from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +Vc terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of RD. At 40kHz dead time increases by 400ns/Ω.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the SYNC frequency.

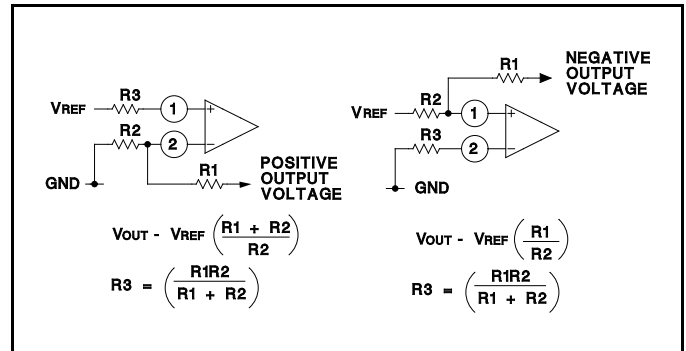
A periodic LOW logic pulse approximately 0.5μs wide at



**Figure 5. Oscillator Connections and Waveforms**

the SYNC pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master and all SYNC terminals are likewise connected to the SYNC pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminal may be either left open or grounded.

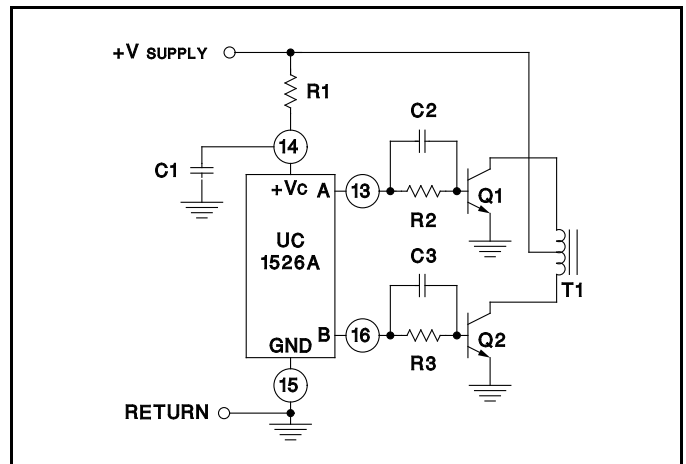


**Figure 6. Error Amplifier Connections**

**Error Amplifier**

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.



**Figure 7. Push-Pull Configuration**

**APPLICATIONS INFORMATION (cont.)**

**Output Drivers**

The totem pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the

+Vc terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at Vc is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

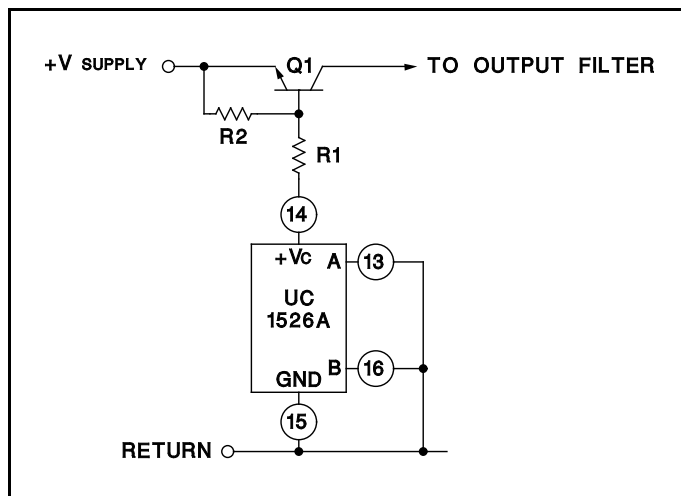


Figure 8. Single-Ended Configuration

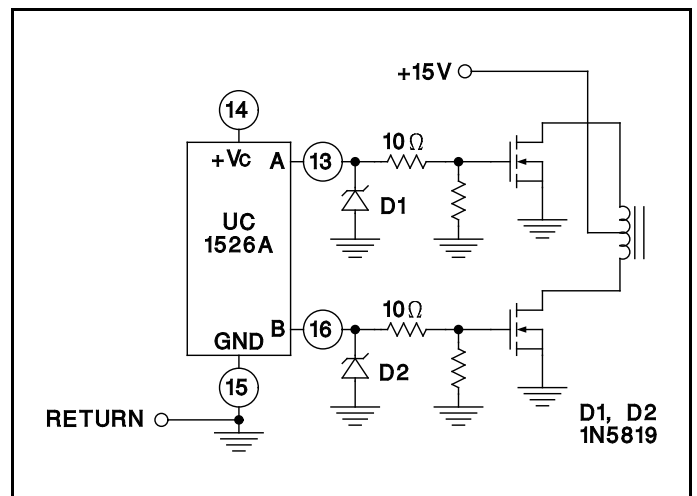
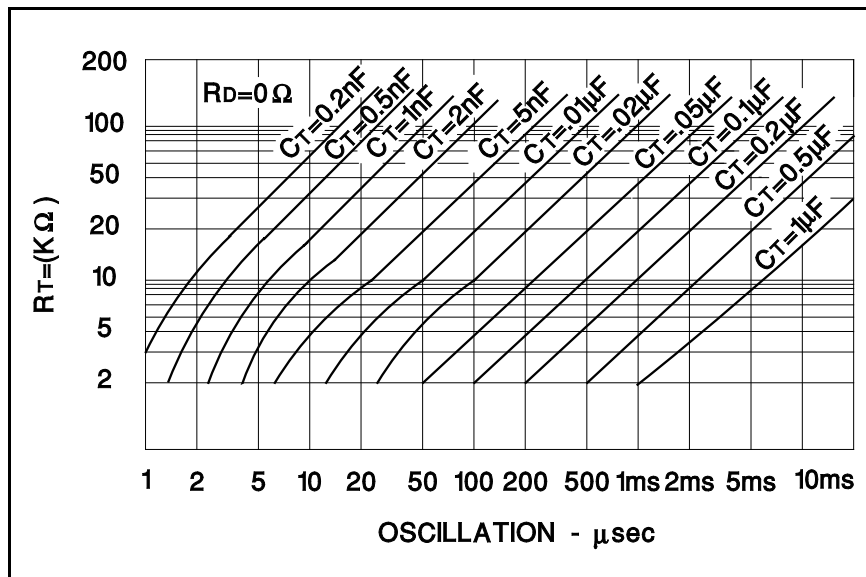


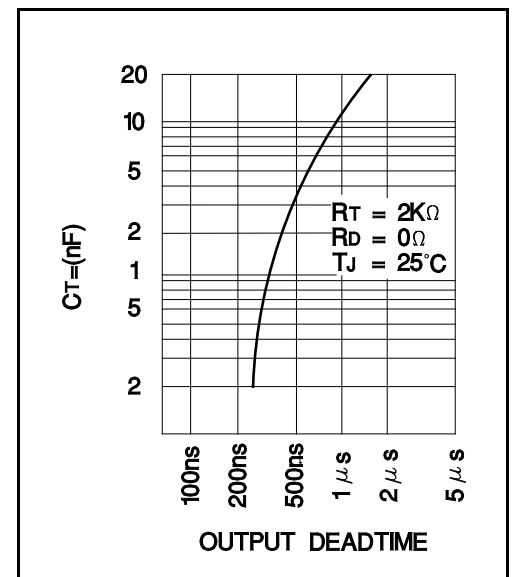
Figure 9. Driving N-Channel Power MOSFETs

**TYPICAL CHARACTERISTICS**

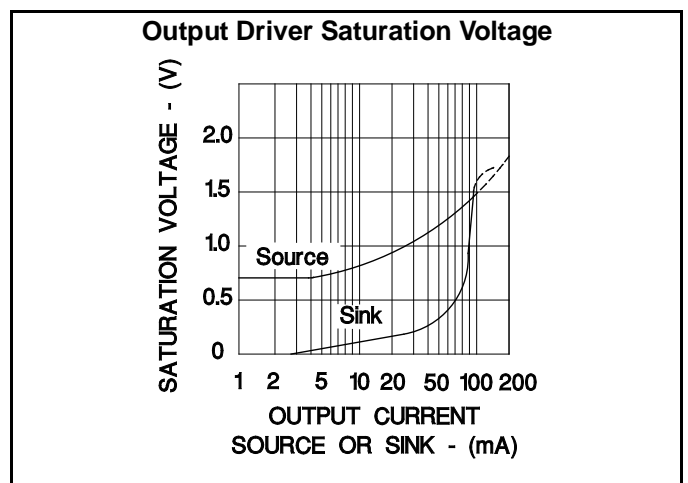
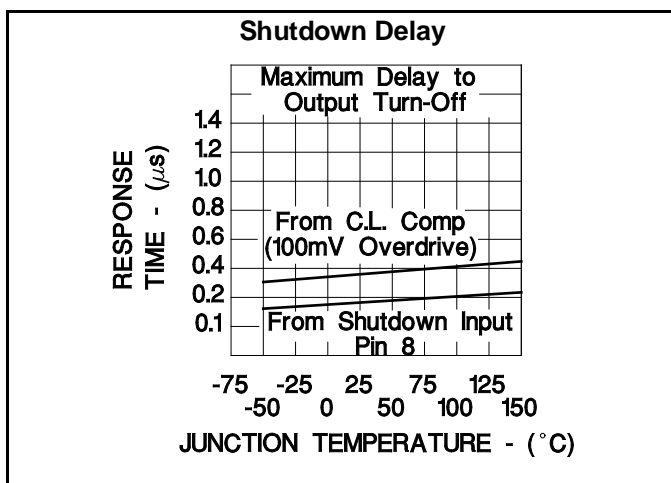
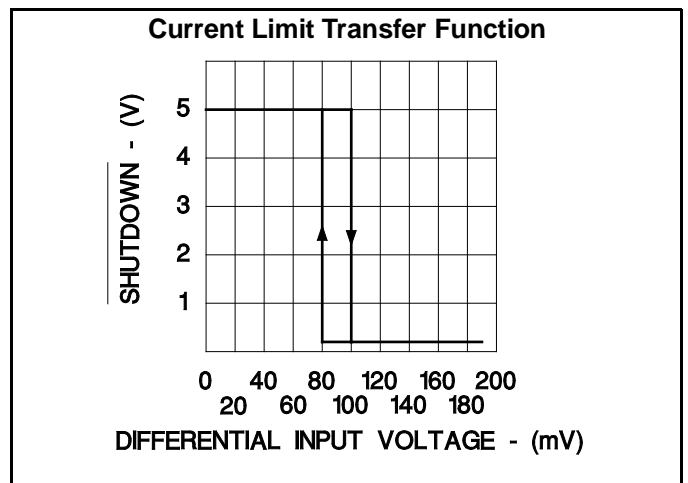
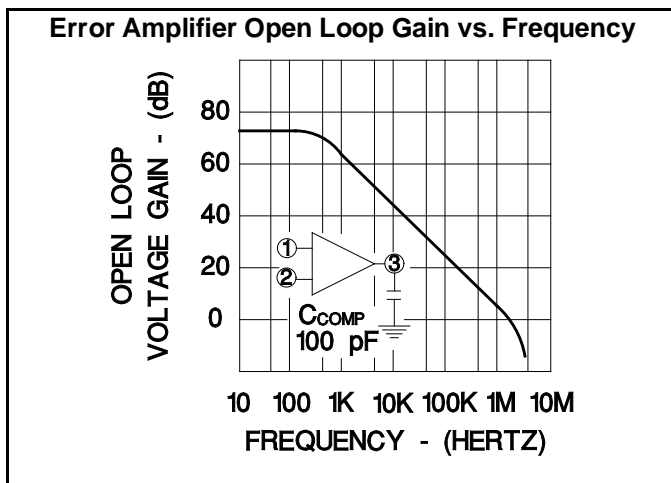
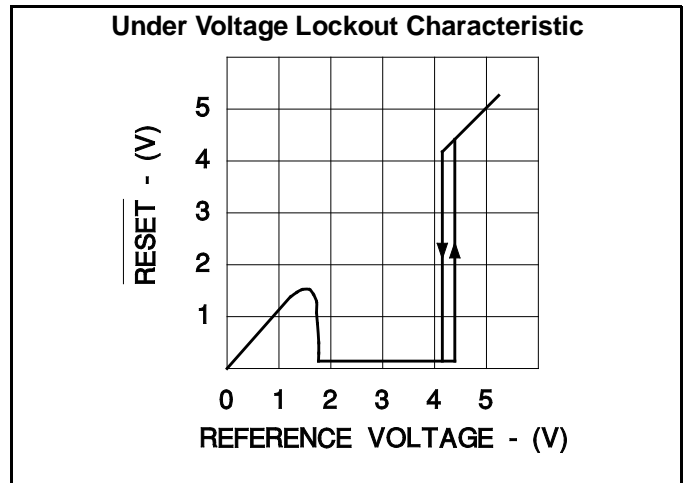
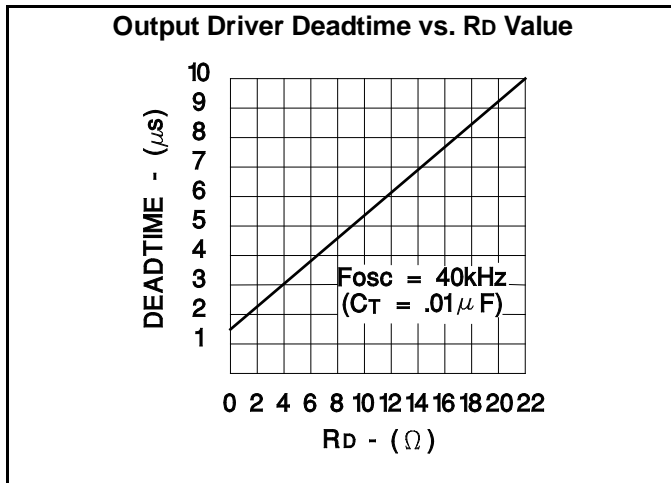
OSCILLATOR PERIOD vs RT and CT



OUTPUT BLANKING



TYPICAL CHARACTERISTICS (Cont.)





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
85515022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85515022A UC1526AL/ 883B	<a href="#">Samples</a>
8551502VA	ACTIVE	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	-55 to 125	8551502VA UC1526AJ/883B	<a href="#">Samples</a>
UC1526AJ	ACTIVE	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1526AJ	<a href="#">Samples</a>
UC1526AJ883B	ACTIVE	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	-55 to 125	8551502VA UC1526AJ/883B	<a href="#">Samples</a>
UC1526AL	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1526AL	<a href="#">Samples</a>
UC1526AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85515022A UC1526AL/ 883B	<a href="#">Samples</a>
UC2526ADW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2526ADW	<a href="#">Samples</a>
UC2526ADWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2526ADW	<a href="#">Samples</a>
UC2526ADWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2526ADW	<a href="#">Samples</a>
UC2526AN	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-25 to 85	UC2526AN	<a href="#">Samples</a>
UC2526ANG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-25 to 85	UC2526AN	<a href="#">Samples</a>
UC2526AQ	NRND	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-25 to 85	UC2526AQ	
UC2526AQQ3	NRND	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-25 to 85	UC2526AQ	
UC3526ADW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3526ADW	<a href="#">Samples</a>
UC3526ADWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3526ADW	<a href="#">Samples</a>
UC3526ADWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3526ADW	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3526ADWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3526ADW	<a href="#">Samples</a>
UC3526AN	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3526AN	<a href="#">Samples</a>
UC3526ANG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3526AN	<a href="#">Samples</a>
UC3526J	ACTIVE	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	0 to 70	UC3526J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1526A, UC2526A, UC3526A, UC3526M :**

- Catalog: [UC3526A](#), [UC3526AM](#), [UC3526](#)
- Military: [UC2526AM](#), [UC1526A](#), [UC1526](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.