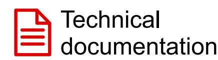


AFE11612-SEP Radiation-Tolerant, Analog Monitor and Controller With Multichannel ADC, DACs, and Temperature Sensors

1 Features

- Radiation tolerant:
  - Single-event latch-up (SEL) immune up to LET = 43 MeV-cm^2/mg at 125°C
  - Single-event functional interrupt (SEFI) characterized up to LET = 43 MeV-cm^2/mg
  - Total ionizing dose (TID) RLAT/RHA characterized up to 20 krad(Si)
- Space-enhanced plastic (space EP):
  - Meets ASTM E595 outgassing specification
  - Vendor item drawing (VID) V62/22614
  - Military temperature range: –55°C to +125°C
  - One fabrication, assembly, and test site
  - Gold bond wire, NiPdAu lead finish
  - Wafer lot traceability
  - Extended product life cycle
  - Extended product change notification
- 12 monotonic, 12-bit DACs
  - 0 V to 5 V output range
  - DAC shutdown to user-defined level
- 16 input, 12-bit SAR ADC
  - High sample rate: 500 kSPS
  - 16 single-ended inputs or 2 differential and 12 single-ended inputs
  - Programmable out-of-range alarms
- 8 GPIO pins
- Internal 2.5-V reference
- Two remote temperature sensors
- Internal temperature sensor
- Configurable SPI and I^{2}C interface
  - 2.7-V to 5.5-V operation

2 Applications

- Command and data handling (C&DH)
- Communications payload
- Radar imaging payload
- Optical imaging payload
- General analog monitoring and control

3 Description

The AFE11612-SEP is a highly integrated analog monitor and control device designed for high-density, general-purpose monitor and control systems. The device includes 12 12-bit digital-to-analog converters (DACs) and a 16-channel, 12-bit, analog-to-digital converter (ADC). The device also incorporates eight general-purpose inputs and outputs (GPIOs), two remote temperature sensor channels, and a local temperature sensor channel.

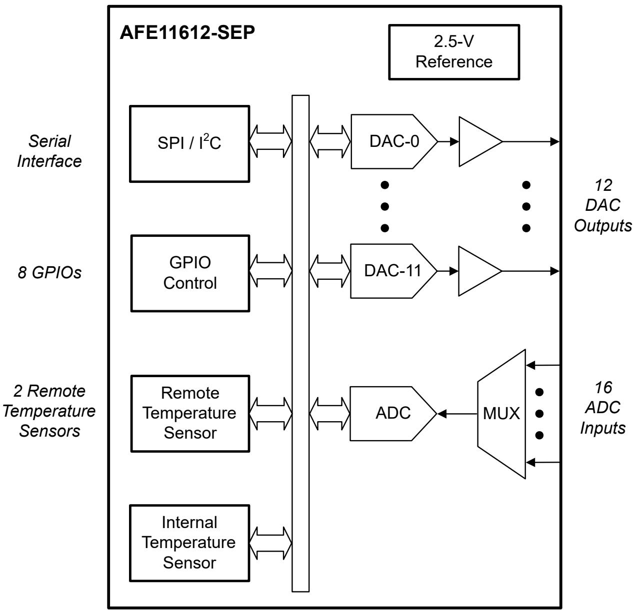
The device has an internal 2.5-V reference that sets the DAC to an output voltage range of 0 V to 5 V. The device also supports operation from an external reference. The device supports communication through both SPI-compatible and I^{2}C-compatible interfaces.

The device high level of integration significantly reduces component count and simplifies closed-loop system design, thus making the device a great choice for high-density applications where radiation-tolerance and board space are critical.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
AFE11612-SEP	HTQFP (64)	10.0 mm × 10.0 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

4 Device and Documentation Support

4.1 Trademarks

All trademarks are the property of their respective owners.

4.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.3 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2022 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE11612PAPSEP	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	AFE11612 PAPSEP	Samples
V62/22614-01XE	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR		AFE11612 PAPSEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

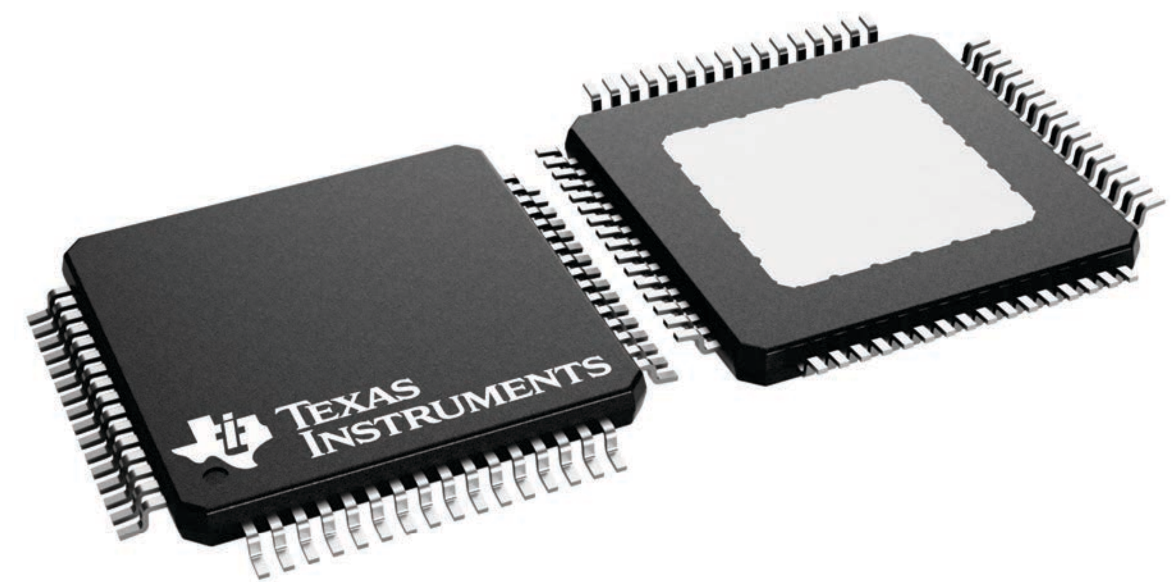
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

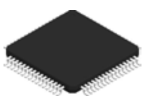
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





PACKAGE OUTLINE

PAP0064G

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

10.2
9.8
NOTE 3
B
PIN 1 ID
64
49
1
48
10.2
9.8
NOTE 3
12.2
11.8
TYP
16
33
17
32
A
60X 0.5
64X 0.27
0.17
0.08 Ⓜ C A B
4X 7.5
C
SEATING PLANE
(0.127)
TYP
SEE DETAIL A
1.2 MAX
17
32
0.25
GAGE PLANE
(1)
16
33
0° -7°
0.08 C
0.15
0.05
7.00
5.99
65
0.75
0.45
DETAIL A
TYPICAL
1
48
64
49

4218924/A 01/2022

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

(□8)
NOTE 8
(□7)
SYMM
64
49
SOLDER MASK
DEFINED PAD
64X (1.5)
1
64X (0.3)
(R0.05)
TYP
48
65
(11.4)
SYMM
(1.3 TYP)
60X (0.5)
16
33
(∅0.2) TYP
VIA
SEE DETAILS
17
32
METAL COVERED
BY SOLDER MASK
(1.3 TYP)
(11.4)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

0.05 MAX
ALL AROUND
METAL
EXPOSED METAL
SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED

0.05 MIN
ALL AROUND
SOLDER MASK
OPENING
EXPOSED METAL
METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218924/A 01/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

(□7)
BASED ON 0.125
THICK STENCIL

SYMM

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

64 49

64X (1.5)

1

64X (0.3)

(R0.05) TYP

SYMM

60X (0.5)

16

48

65

(11.4)

33

METAL COVERED
BY SOLDER MASK

17 32

(11.4)

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.83 X 7.83
0.125	7.0 X 7.0 (SHOWN)
0.15	6.39 X 6.39
0.175	5.92 X 5.92

4218924/A 01/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023, Texas Instruments Incorporated