# 12-Bit Analog Monitoring and Control Solution with Multichannel ADC, DACs, and Temperature Sensors

**Check for Samples: AMC7812B**

## FEATURES

- **12, 12-Bit DACs with Programmable Outputs:**
  - **0 V to 5 V**
  - **0 V to 12.5 V**
- **DAC Shutdown to User-Defined Level**
- **12-Bit, 500-kSPS ADC with 16 Inputs:**
  - **16 Single-Ended or Two Differential + 12 Single-Ended**
- **Two Remote Temperature Sensors:**
  - **±2°C Accuracy, –40°C to +150°C**
- **One Internal Temperature Sensor:**
  - **±2.5°C Accuracy, –40°C to +125°C**
- **Input Out-of-Range Alarms**
- **2.5-V Internal Reference**
- **Eight General-Purpose Inputs and Outputs**
- **Configurable I²C-Compatible and SPI™ Interface with 5-V and 3-V Logic**
- **Power-Down Mode**
- **Wide Operating Temperature Range: –40°C to +125°C**
- **Small Packages: 9-mm × 9-mm QFN-64, and 10-mm × 10-mm HTQFP-64**

## APPLICATIONS

- **RF Power Amplifier Control in Base Stations**
- **Test and Measurement**
- **Industrial Control**
- **General Analog Monitoring and Control**

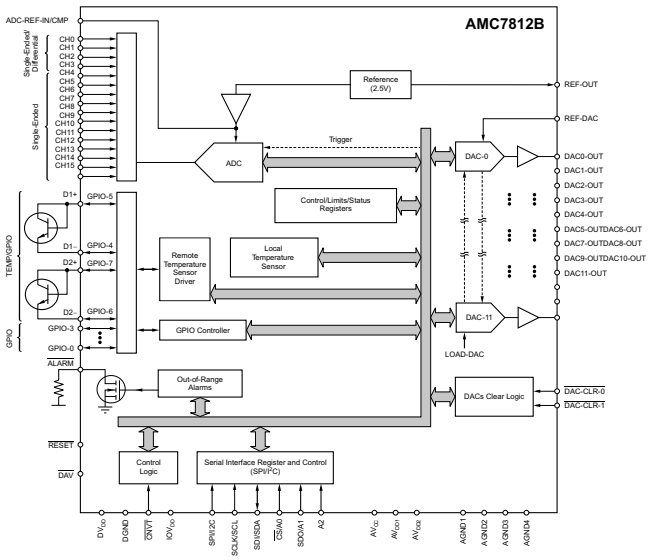
## DESCRIPTION

The AMC7812B is a complete analog monitoring and control solution that includes a 16-channel, 12-bit, analog-to-digital converter (ADC), twelve 12-bit digital-to-analog converters (DACs), eight general-purpose inputs and outputs (GPIOs), two remote temperature sensor channels, and one local temperature sensor channel.

The device has an internal +2.5-V reference that can configure the DAC output voltage to a range of either 0 V to +5 V or 0 V to +12.5 V. An external reference can be used as well. Typical power dissipation is 95 mW. The AMC7812B is ideal for multichannel applications where board space, size, and low power are critical.

The device is available in either a QFN-64 or HTQFP-64 PowerPAD™ package and is fully specified from –40°C to +105°C and operational over the full –40°C to +125°C temperature range.

For applications that require a different channel count, additional features, or converter resolutions, Texas Instruments offers a complete family of analog monitor and control (AMC) products. Refer to www.ti.com/amc for more information.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

| | | VALUE | UNIT |
|---|---|---|---|
| $AV_{DD}$ to GND | | –0.3 to +6 | V |
| $DV_{DD}$ to GND | | –0.3 to +6 | V |
| $IOV_{DD}$ to GND | | –0.3 to +6 | V |
| $AV_{CC}$ to GND | | –0.3 to +18 | V |
| $DV_{DD}$ to DGND | | –0.3 to +6 | V |
| Analog input voltage to GND | | –0.3 to $AV_{DD}$ + 0.3 | V |
| ALARM, GPIO-0, GPIO-1, GPIO-2, GPIO-3, SCLK/SCL, and SDI/SDA to GND | | –0.3 to +6 | V |
| D1+/GPIO-4, D1–/GPIO-5, D2+/GPIO-6, D2–/GPIO-7 to GND | | –0.3 to $AV_{DD}$ + 0.3 | V |
| Digital input voltage to DGND | | –0.3 to $IOV_{DD}$ + 0.3 | V |
| SDO and DAV to GND | | –0.3 to $IOV_{DD}$ + 0.3 | V |
| Operating temperature range | | –40 to +125 | °C |
| Storage temperature range | | –40 to +150 | °C |
| Junction temperature range ($T_J$ max) | | +150 | °C |
| Electrostatic discharge (ESD) ratings | Human body model (HBM) | 2.5 | kV |
| | Charged device model (CDM) | 1.0 | kV |

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | AMC7812B | | UNITS |
|---|---|---|---|---|
| | | RGC (QFN) | PAP (HTQFP) | |
| | | 64 PINS | 64 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 24.1 | 33.7 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 8.1 | 9.5 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 3.2 | 9.0 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | 0.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 3.3 | 8.9 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 0.6 | 0.2 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ELECTRICAL CHARACTERISTICS

At $T_A$ = –40°C to +105°C, $AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, $AV_{CC}$ = +15 V, AGND = DGND = 0 V, $IOV_{DD}$ = 2.7 V to 5.5 V, internal 2.5-V reference, and the DAC output span = 0 V to 5 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DAC PERFORMANCE** | | | | | | |
| **DAC DC ACCURACY** | | | | | | |
| | Resolution | | 12 | | | Bits |
| INL | Relative accuracy | $T_A$ = –40°C to +105°C, measured by line passing through codes 020h and FFFh | | | ±1 | LSB |
| | | $T_A$ = –40°C to +125°C, measured by line passing through codes 020h and FFFh | | | ±1.25 | LSBs |
| DNL | Differential nonlinearity | $T_A$ = –40°C to +125°C, measured by line passing through codes 020h and FFFh | | ±0.3 | ±1 | LSB |
| TUE | Total unadjusted error | $T_A$ = +25°C, DAC output = 5.0 V | | | ±10 | mV |
| | | $T_A$ = +25°C, DAC output = 12.5 V | | | ±30 | mV |
| | Offset error | $T_A$ = +25°C, DAC output = 0 V to +5 V, code 020h | | | ±2 | mV |
| | | $T_A$ = +25°C, DAC output = 0 V to +12.5 V, code 020h | | | ±5 | mV |
| | Offset error temperature coefficient | | | ±1 | | ppm/°C |
| | Gain error | $T_A$ = –40°C to +125°C, external reference, output = 0 V to +5 V | | ±0.025 | ±0.15 | %FSR |
| | | $T_A$ = –40°C to +125°C, external reference, output = 0 V to +12.5 V | | –0.15 | ±0.3 | %FSR |
| | Gain temperature coefficient | | | ±2 | | ppm/°C |
| **DAC OUTPUT CHARACTERISTICS** | | | | | | |
| | Output voltage range(1) | $T_A$ = –40°C to +125°C, $V_{REF}$ = 2.5 V, gain = 2 | 0 | | 5 | V |
| | | $T_A$ = –40°C to +125°C, $V_{REF}$ = 2.5 V, gain = 5 | 0 | | 12.5 | V |
| | Output voltage settling time(2) | DAC output = 0 V to +5 V, code 400h to C00h, to 1/2 LSB, from $\overline{CS}$ rising edge, $R_L$ = 2 kΩ, $C_L$ = 200 pF | | 3 | | µs |
| | Slew rate(2) | | | 1.5 | | V/µs |
| | Short-circuit current(2) | Full-scale current shorted to ground | | 30 | | mA |
| | Load current | Source within 200 mV of supply, $T_A$ = +25°C | | +10 | | mA |
| | | Sink within 300 mV of supply, $T_A$ = +25°C | | –10 | | mA |
| | | DAC output = 0 V to +5 V, code B33h. Source and sink with voltage drop < 25 mV, $T_A$ = –40°C to +95°C | ±8 | | | mA |
| | Capacitive load stability(2) | $R_L$ = infinite | 10 | | | nF |
| | DC output impedance(2) | Code 800h | | 0.3 | | Ω |
| | Power-on overshoot | $AV_{CC}$ 0 V to 5 V, 2-ms ramp | | 5 | | mV |
| | Digital-to-analog glitch energy | Code changes from 7FFh to 800h, 800h to 7FFh | | 0.15 | | nV-s |
| | Digital feedthrough | Device is not accessed | | 0.15 | | nV-s |
| | Output noise | $T_A$ = +25°C, at 1 kHz, code 800h, gain = 2, excludes reference | | 81 | | nV/$\sqrt{Hz}$ |
| | | f = 0.1 Hz to 10 Hz, excludes reference | | 8 | | $\mu V_{PP}$ |
| **DAC REFERENCE INPUT** | | | | | | |
| | Reference voltage input range | $T_A$ = –40°C to +125°C, REF-DAC pin | 1 | | 2.6 | V |
| | Input current(2) | $V_{REF}$ = 2.5 V | | 170 | | µA |

(1) The output voltage must not be greater than $AV_{CC}$. See the *DAC Output* section for further details.
(2) Sampled during initial release to ensure compliance; not subject to production testing.

## ELECTRICAL CHARACTERISTICS (continued)

At $T_A$ = –40°C to +105°C, $AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, $AV_{CC}$ = +15 V, AGND = DGND = 0 V, $IOV_{DD}$ = 2.7 V to 5.5 V, internal 2.5-V reference, and the DAC output span = 0 V to 5 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL REFERENCE** | | | | | | |
| | Output voltage | $T_A$ = +25°C, REF-OUT pin | 2.495 | 2.5 | 2.505 | V |
| | Output impedance | | | 0.4 | | Ω |
| | Reference temperature coefficient | $T_A$ = –40°C to +125°C | | 10 | 25 | ppm/°C |
| | Output current (sourcing and sinking) | | | ±5 | | mA |
| | Output voltage noise | $T_A$ = +25°C, f = 1 kHz | | 260 | | nV/√Hz |
| | | f = 0.1 Hz to 10 Hz | | 13 | | $\mu V_{PP}$ |
| **ADC PERFORMANCE** | | | | | | |
| **ADC DC ACCURACY (for $AV_{DD}$ = 5 V)** | | | | | | |
| | Resolution | | | 12 | | Bits |
| INL | Integral nonlinearity | $T_A$ = –40°C to +125°C | | ±0.5 | ±1 | LSB |
| DNL | Differential nonlinearity | $T_A$ = –40°C to +125°C | | ±0.5 | ±1 | LSB |
| **Single-Ended Mode** | | | | | | |
| | Offset error | | | ±1 | ±3 | LSB |
| | Offset error match | | | ±0.4 | | LSB |
| | Gain error | External reference | | ±1 | ±5 | LSB |
| | Gain error match | | | ±0.4 | | LSB |
| **Differential Mode** | | | | | | |
| | Gain error | External reference, 0 V to (2 × $V_{REF}$) mode, $V_{CM}$ = 2.5 V | | ±2 | ±5 | LSB |
| | | External reference, 0 V to $V_{REF}$ mode, $V_{CM}$ = 1.25 V | | ±1 | ±5 | LSB |
| | Gain error match | | | ±0.5 | | LSB |
| | Zero code error | 0 V to (2 × $V_{REF}$) mode, $V_{CM}$ = 2.5 V | | ±1 | ±3 | LSB |
| | | External reference, 0 V to $V_{REF}$ mode, $V_{CM}$ = 1.25 V | | ±1 | ±3 | LSB |
| | Zero code error match | | | ±0.5 | | LSB |
| | Common-mode rejection | At dc, 0 V to (2 × $V_{REF}$) mode | | 67 | | dB |
| **SAMPLING DYNAMICS** | | | | | | |
| | Conversion rate | External single analog channel, auto mode | | 500 | | kSPS |
| | | External single analog channel, direct mode | | 167 | | kSPS |
| | Conversion time(3) | External single analog channel | | 2 | | µs |
| | Autocycle update rate(3) | All 16 single-ended inputs enabled | | 32 | | µs |
| | Throughput rate | SPI clock, 12 MHz or greater, single channel | | | 500 | kSPS |
| **ANALOG INPUT(4)** | | | | | | |
| | Full-scale input voltage | $T_A$ = –40°C to +125°C, single-ended, 0 V to $V_{REF}$ | 0 | | $V_{REF}$ | V |
| | | $T_A$ = –40°C to +125°C, single-ended, 0 V to (2 × $V_{REF}$) | 0 | | 2 × $V_{REF}$ | V |
| | | $T_A$ = –40°C to +125°C, $V_{IN+}$ – $V_{IN–}$, fully-differential, 0 V to $V_{REF}$ | –$V_{REF}$ | | +$V_{REF}$ | V |
| | | $T_A$ = –40°C to +125°C, $V_{IN+}$ – $V_{IN–}$, fully-differential, 0 V to (2 × $V_{REF}$) | –2 × $V_{REF}$ | | 2 × $V_{REF}$ | V |
| | Absolute input voltage | $T_A$ = –40°C to +125°C | GND – 0.2 | | $AV_{DD}$ + 0.2 | V |
| | Input capacitance(3) | 0 V to $V_{REF}$ mode | | 118 | | pF |
| | | 0 V to (2 × $V_{REF}$) mode | | 73 | | pF |
| | DC input leakage current | Unselected ADC input | | | ±10 | µA |
| **ADC REFERENCE INPUT** | | | | | | |
| | Reference input voltage range | $T_A$ = –40°C to +125°C | 1.2 | | $AV_{DD}$ | V |
| | Input current | $V_{REF}$ = 2.5 V | | 145 | | µA |

(3) Sampled during initial release to ensure compliance; not subject to production testing.
(4) $V_{IN+}$ or $V_{IN–}$ must remain within GND – 0.2 V and $AV_{DD}$ + 0.2 V; see the *Analog Inputs* section.

## ELECTRICAL CHARACTERISTICS (continued)

At $T_A$ = –40°C to +105°C, $AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, $AV_{CC}$ = +15 V, AGND = DGND = 0 V, $IOV_{DD}$ = 2.7 V to 5.5 V, internal 2.5-V reference, and the DAC output span = 0 V to 5 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL ADC REFERENCE BUFFER** | | | | | | |
| | Offset | $T_A$ = +25°C | | | ±5 | mV |
| **INTERNAL TEMPERATURE SENSOR** | | | | | | |
| | Operating range | | –40 | | +125 | °C |
| | Accuracy | $AV_{DD}$ = 5 V, $T_A$ = –40°C to +125°C | | ±1.25 | ±2.5 | °C |
| | | $AV_{DD}$ = 5 V, $T_A$ = 0°C to +100°C | | | ±1.5 | °C |
| | Resolution | Per LSB | | 0.125 | | °C |
| | Conversion rate | External temperature sensors are disabled | | 15 | | ms |
| **EXTERNAL TEMPERATURE SENSOR (Using 2N3906 external transistor)** | | | | | | |
| | Operating range | Limited by external diode | –40 | | +150 | °C |
| | Accuracy[5][6] | $AV_{DD}$ = 5 V, $T_A$ = 0°C to +100°C, $T_D$ = –40°C to +150°C | | | ±1.5 | °C |
| | | $AV_{DD}$ = 5 V, $T_A$ = –40°C to +100°C, $T_D$ = –40°C to +150°C | | | ±2 | °C |
| | Resolution | Per LSB | | 0.125 | | °C |
| | Conversion rate per sensor | With resistance cancellation (RC bit = '1') | 72 | 93 | 100 | ms |
| | | Without resistance cancellation (RC bit = '0') | 33 | 44 | 47 | ms |
| **DIGITAL LOGIC: GPIO[7][8] and $\overline{ALARM}$** | | | | | | |
| $V_{IH}$ | Input high voltage | $IOV_{DD}$ = +5 V | 2.1 | | 0.3 + $IOV_{DD}$ | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V | 2.2 | | 0.3 + $IOV_{DD}$ | V |
| $V_{IL}$ | Input low voltage | $IOV_{DD}$ = +5 V | –0.3 | | 0.8 | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V | –0.3 | | 0.7 | V |
| $V_{OL}$ | Output low voltage | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +5 V, sinking 5 mA | | | 0.4 | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V, sinking 2 mA | | | 0.4 | V |
| | High-impedance leakage | | | | 5 | µA |
| | High-impedance output capacitance | | | | 10 | pF |
| **DIGITAL LOGIC: All Except SCL, SDA, $\overline{ALARM}$, and GPIO** | | | | | | |
| $V_{IH}$ | Input high voltage | $IOV_{DD}$ = +5 V | 2.1 | | 0.3 + $IOV_{DD}$ | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V | 2.2 | | 0.3 + $IOV_{DD}$ | V |
| $V_{IL}$ | Input low voltage | $IOV_{DD}$ = +5 V | –0.3 | | 0.8 | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V | –0.3 | | 0.7 | V |
| | Input current | | | | ±1 | µA |
| | Input capacitance | | | | 5 | pF |
| $V_{OH}$ | Output high voltage | $IOV_{DD}$ = +5 V, sourcing 3 mA | 4.8 | | | V |
| | | $IOV_{DD}$ = +3.3 V, sourcing 3 mA | 2.9 | | | V |
| $V_{OL}$ | Output low voltage | $IOV_{DD}$ = +5 V, sinking 3 mA | | | 0.4 | V |
| | | $IOV_{DD}$ = +3.3 V, sinking 3 mA | | | 0.4 | V |
| | High-impedance leakage | | | | ±5 | µA |
| | High-impedance output capacitance | | | | 10 | pF |

(5) $T_D$ is the external diode temperature.
(6) Auto conversion mode disabled.
(7) For pins GPIO0 to GPIO3, the external pull-up resistor must be connected to a voltage less than or equal to 5.5 V.
(8) For pins GPIO4 to GPIO7, the external pull-up resistor must be connected to a voltage less than or equal to $AV_{DD}$.

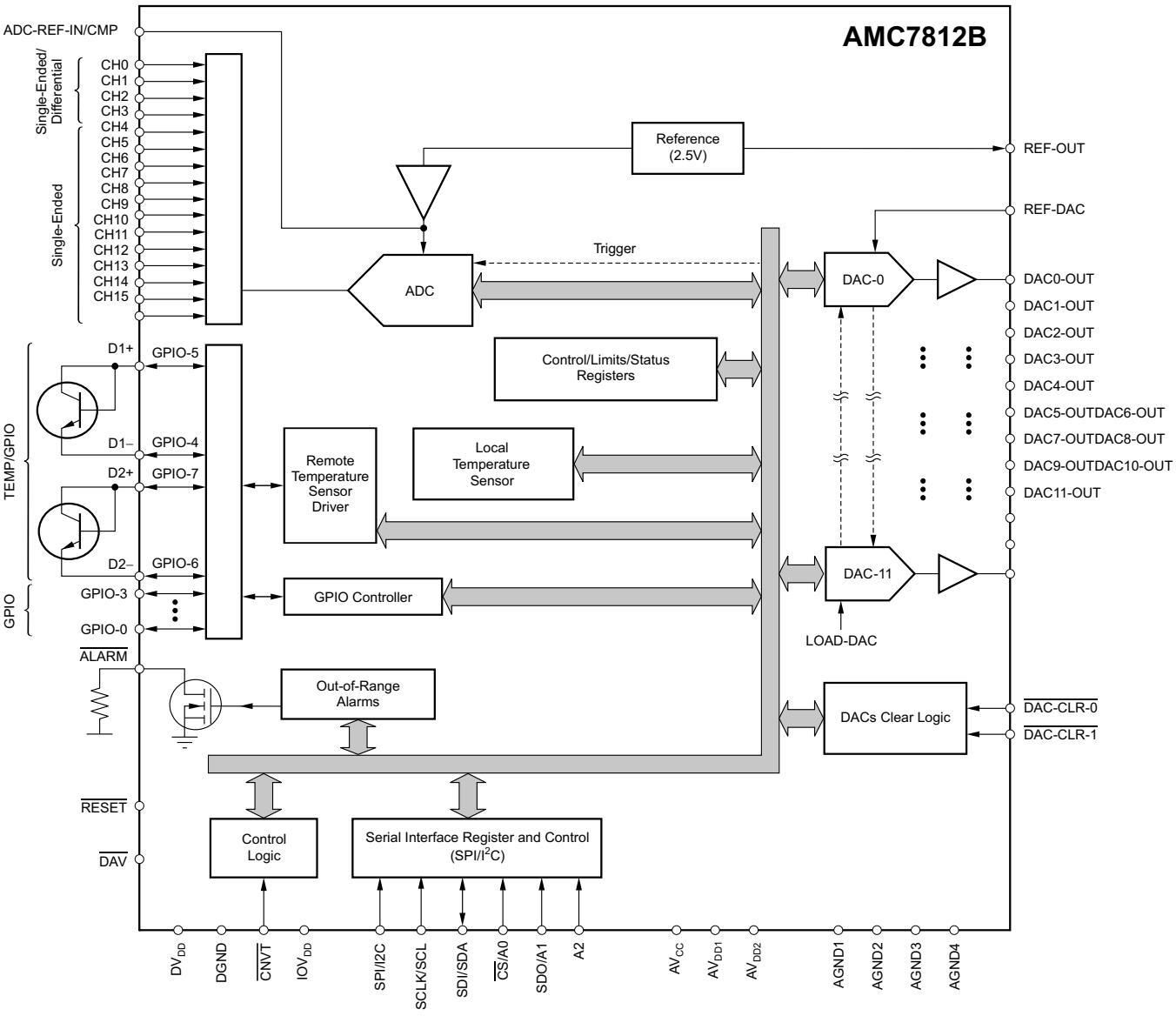
## ELECTRICAL CHARACTERISTICS (continued)

At $T_A$ = –40°C to +105°C, $AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, $AV_{CC}$ = +15 V, AGND = DGND = 0 V, $IOV_{DD}$ = 2.7 V to 5.5 V, internal 2.5-V reference, and the DAC output span = 0 V to 5 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL LOGIC: SDA, SCL ($I^2C$-Compatible Interface)** | | | | | | |
| $V_{IH}$ | Input high voltage | $IOV_{DD}$ = +5 V | 2.1 | | 0.3 + $IOV_{DD}$ | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V | 2.2 | | 0.3 + $IOV_{DD}$ | V |
| $V_{IL}$ | Input low voltage | $IOV_{DD}$ = +5 V | –0.3 | | 0.8 | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V | –0.3 | | 0.7 | V |
| | Input current | | | | ±5 | µA |
| | Input capacitance | | | | 5 | pF |
| $V_{OL}$ | Output low voltage | $IOV_{DD}$ = +5 V, sinking 3 mA | 0 | | 0.4 | V |
| | | $T_A$ = –40°C to +125°C, $IOV_{DD}$ = +3.3 V, sinking 3 mA | 0 | | 0.4 | V |
| | High-impedance leakage | | | | ±5 | µA |
| | High-impedance output capacitance | | | | 10 | pF |
| **TIMING REQUIREMENTS** | | | | | | |
| | Power-on delay | From $AV_{DD}$ , $DV_{DD}$ ≥ 2.7 V and $AV_{CC}$ ≥ 4.5 V to normal operation | | 100 | 250 | µs |
| | Power-down recovery time | From $\overline{CS}$ rising edge | | | 70 | µs |
| | Reset delay | Delay to normal operation from any reset | | 100 | 250 | µs |
| | Convert pulse width | | 20 | | | ns |
| | Reset pulse width | | 20 | | | ns |
| **POWER-SUPPLY REQUIREMENTS** | | | | | | |
| | $AV_{DD}$ | $AV_{DD}$ must be ≥ ($V_{REF}$ + 1.2 V) | +2.7 | | +5.5 | V |
| | $AI_{DD}$ | $T_A$ = –40°C to +125°C, $AV_{DD}$ and $DV_{DD}$ combined, normal operation, no DAC load | | 7.9 | 12.5 | mA |
| | | $AV_{CC}$ | | 1.6 | | mA |
| | $IV_{CC}$ | | +4.5 | | +18 | V |
| | | $AV_{CC}$, no load, DACs at code 800h | | | 6.5 | mA |
| | Power dissipation | $T_A$ = –40°C to +125°C, normal operation(9), $AV_{DD}$ = $DV_{DD}$ = 5 V, $AV_{CC}$ = 15 V | | 95 | 120 | mW |
| | $DV_{DD}$ | | +2.7 | | +5.5 | V |
| | $IOV_{DD}$ | | +2.7 | | +5.5 | V |
| **TEMPERATURE RANGE** | | | | | | |
| | Specified performance | | –40 | | +105 | °C |
| | Operating range | | –40 | | +125 | °C |

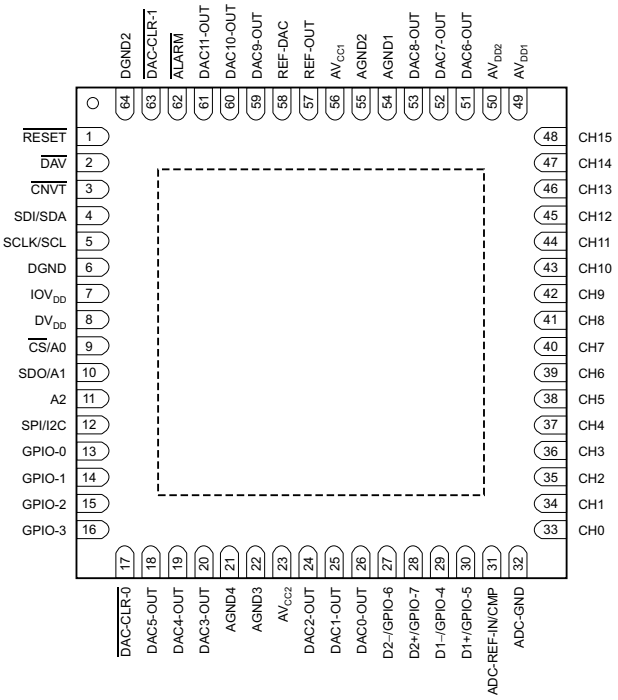
(9) No DAC load, all DACs at 800h and both ADCs at the fastest auto conversion rate.

## FUNCTIONAL BLOCK DIAGRAM

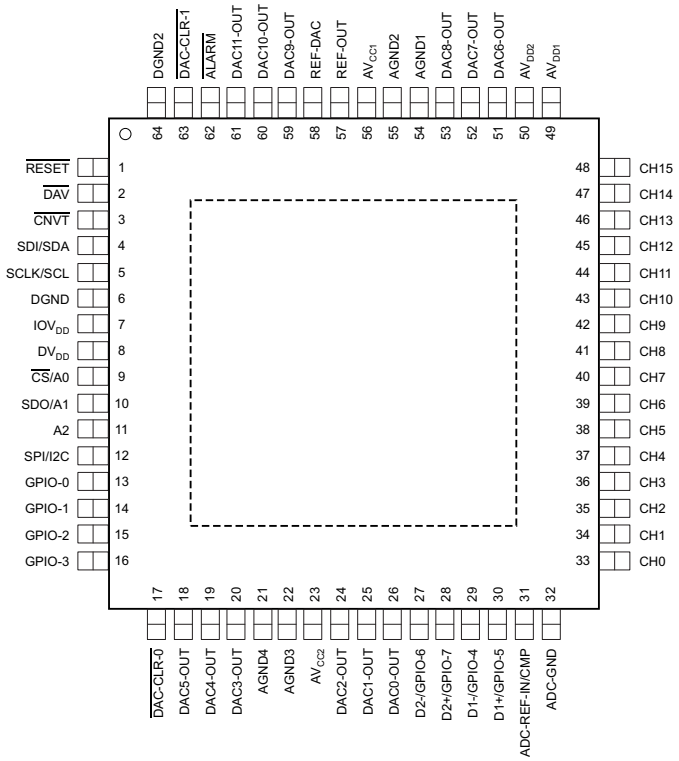


## PIN CONFIGURATIONS

**RGC PACKAGE**
**QFN-64**
**(TOP VIEW)**




**PAP PACKAGE**
**HTQFP-64**
**(TOP VIEW)**



## PIN DESCRIPTIONS

| NAME | NO. | DESCRIPTION |
|---|---|---|
| A2 | 11 | Slave address selection A2 for $I^2C$ when the SPI/I2C pin is low. |
| ADC-GND | 32 | ADC ground. Must be connected to AGND. |
| ADC-REF-IN/CMP | 31 | External ADC reference input when external $V_{REF}$ is used to drive the ADC. A compensation capacitor connection (connect a 4.7-µF capacitor between this pin and AGND) when internal $V_{REF}$ is used to drive the ADC. |
| AGND1 | 54 | Analog ground |
| AGND2 | 55 | Analog ground |
| AGND3 | 22 | Analog ground |
| AGND4 | 21 | Analog ground |
| $\overline{\text{ALARM}}$ | 62 | Global alarm. Open-drain output. An external 10-kΩ, pull-up resistor is required. This pin goes low (active) when one (or more) analog channels are out of range. |
| $AV_{CC1}$ | 56 | Positive analog power for DAC6-OUT, DAC7-OUT, DAC8-OUT, DAC9-OUT, DAC10-OUT, and DAC11-OUT, must be tied to $AV_{CC2}$ |
| $AV_{CC2}$ | 23 | Positive analog power for DAC0-OUT, DAC1-OUT, DAC2-OUT, DAC3-OUT, DAC4-OUT, and DAC5-OUT, must be tied to $AV_{CC1}$ |
| $AV_{DD1}$ | 49 | Positive analog power supply |
| $AV_{DD2}$ | 50 | Positive analog power supply |
| CH0 to CH15 | 33-48 | Analog inputs of channel 0 to 15. CH4 to CH15 are single-ended. CH0, CH1, CH2, and CH3 can be programmed as differential or single-ended. |
| $\overline{\text{CNVT}}$ | 3 | External conversion trigger, active low. The falling edge initiates the sampling and conversion of the ADC. |
| $\overline{\text{CS}}$/A0 | 9 | Chip-select signal for SPI when the SPI/I2C pin is high. Slave address selection A0 for $I^2C$ when the SPI/I2C pin is low. |
| D1–/GPIO4 | 29 | Remote sensor D1 negative input when D1 is enabled; GPIO-6 when D1 is disabled. Pull-up resistor required for output. |
| D1+/GPIO-5 | 30 | Remote sensor D1 positive input when D1 is enabled; GPIO-7 when D1 is disabled. Pull-up resistor required for output. |
| D2–/GPIO-6 | 27 | Remote sensor D2 negative input when D2 is enabled; GPIO-6 when D2 is disabled. Pull-up resistor required for output. |
| D2+/GPIO-7 | 28 | Remote sensor D2 positive input when D2 is enabled; GPIO-7 when D2 is disabled. Pull-up resistor required for output. |
| DAC0-OUT | 26 | DAC channel 0 output |
| DAC1-OUT | 25 | DAC channel 1 output |
| DAC2-OUT | 24 | DAC channel 2 output |
| DAC3-OUT | 20 | DAC channel 3 output |
| DAC4-OUT | 19 | DAC channel 4 output |
| DAC5-OUT | 18 | DAC channel 5 output |
| DAC6-OUT | 51 | DAC channel 6 output |
| DAC7-OUT | 52 | DAC channel 7 output |
| DAC8-OUT | 53 | DAC channel 8 output |
| DAC9-OUT | 59 | DAC channel 9 output |
| DAC10-OUT | 60 | DAC channel 10 output |
| DAC11-OUT | 61 | DAC channel 11 output |
| $\overline{\text{DAC-CLR-0}}$ | 17 | DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC-CLR-0 pin enter a clear state, the DAC latch is loaded with a predefined code, and the output is set to the corresponding level. However, the DAC-data register does not change. When the DAC goes back to normal operation, the DAC latch is loaded with the previous data from the DAC-data register and the output returns to the previous level, regardless of the status of the SLDAC-n bit. When this pin is high, the DACs are in normal operation. |
| $\overline{\text{DAC-CLR-1}}$ | 63 | DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC-CLR-1 pin enter a clear state, the DAC latch is loaded with a predefined code, and the output is set to the corresponding level. However, the DAC-data register does not change. When the DAC goes back to normal operation, the DAC latch is loaded with the previous data from the DAC-data register and the output returns to the previous level, regardless of the status of the SLDAC-n bit. When this pin is high, the DACs are in normal operation. |
| $\overline{\text{DAV}}$ | 2 | Data available indicator, active low output. In direct mode, the $\overline{\text{DAV}}$ pin goes low (active) when the conversion ends. In auto mode, a 1-µs pulse (active low) appears on this pin when a conversion cycle completes (see the *Primary ADC Operation* and *Registers* sections for details). $\overline{\text{DAV}}$ stays high when deactivated. |
| DGND | 6 | Digital ground |
| DGND2 | 64 | Digital ground |
| $DV_{DD}$ | 8 | Digital power supply (+3 V to +5 V). Must be the same value as $AV_{DD}$. |
| GPIO-0 | 13 | General-purpose digital inputs and outputs. These pins are bidirectional open-drain, digital input and output pins, and require an external pull-up resistor. See the *General Purpose Input/Output Pins* section for more details. |
| GPIO-1 | 14 | |
| GPIO-2 | 15 | |
| GPIO-3 | 16 | |

## PIN DESCRIPTIONS (continued)

| NAME | NO. | DESCRIPTION |
|---|---|---|
| $IOV_{DD}$ | 7 | Interface power supply |
| REF-DAC | 58 | DAC reference Input |
| REF-OUT | 57 | Internal reference output |
| $\overline{RESET}$ | 1 | Reset input, active low. A logic low on this pin causes the device to perform a hardware reset. |
| SCLK/SCL | 5 | Serial clock input of the main serial interface. This pin functions as the SPI clock when the SPI/I2C pin is high. This pin functions as the $I^2C$ clock when the SPI/I2C pin is low. |
| SDI/SDA | 4 | Serial interface data. This pin functions as SDI for the serial peripheral interface (SPI) when the SPI/I2C pin (pin 12) is high. This pin functions as SDA for the $I^2C$ interface when the SPI/I2C pin is low. |
| SDO/A1 | 10 | SDO for SPI when the SPI/I2C pin is high. Slave address selection A1 for $I^2C$ when the SPI/I2C pin is low. |
| SPI/I2C | 12 | Interface selection pin; digital input. When this pin is tied to $IOV_{DD}$, the SPI is enabled and the $I^2C$ interface is disabled. When this pin is tied to ground, the SPI is disabled and the $I^2C$ interface is enabled. |

## I²C-COMPATIBLE TIMING DIAGRAMS

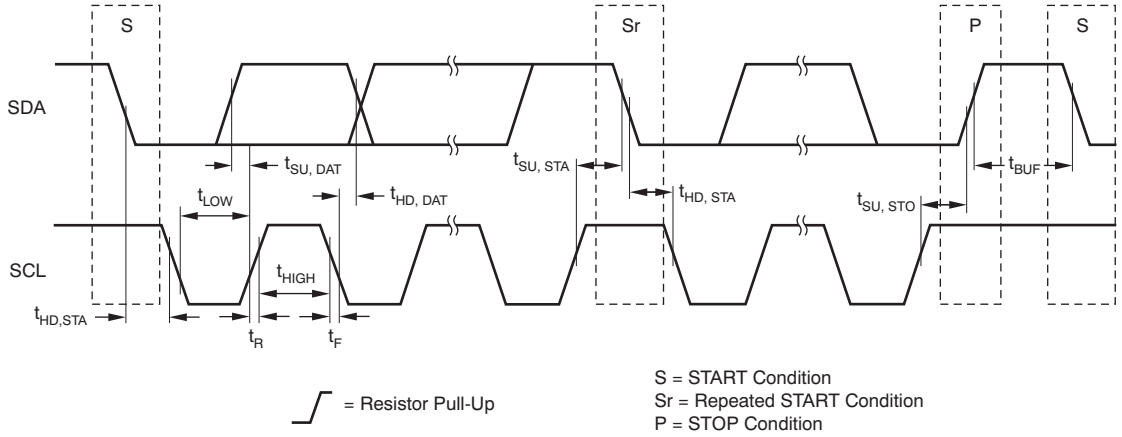


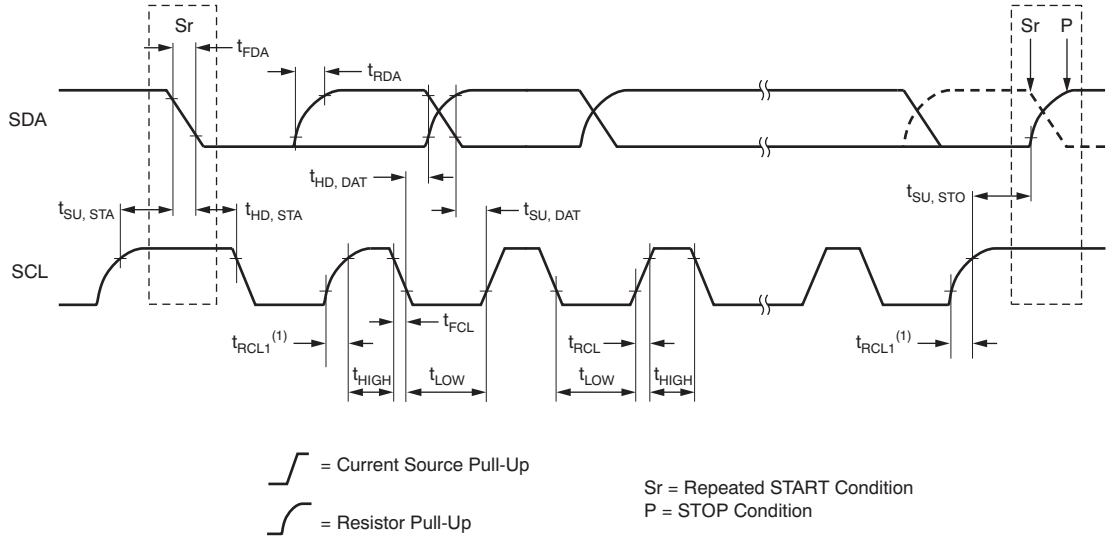

**Figure 1. Timing for Standard and Fast Mode Devices on the I²C Bus**

## TIMING CHARACTERISTICS: SDA and SCL for Standard and Fast Modes(1)

At –40°C to +105°C, $AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, AGND = DGND = 0 V, and $IOV_{DD}$ = 2.7 V to 5.5 V, unless otherwise noted.

| PARAMETER | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{SCL}$ (2) | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{LOW}$ | Low period of the SCL clock | 4.7 | — | 1.3 | — | µs |
| $t_{HIGH}$ | High period of the SCL clock | 4.0 | — | 0.6 | — | µs |
| $t_{SU, STA}$ | Set-up time for a repeated start condition | 4.7 | — | 0.6 | — | µs |
| $t_{HD, STA}$ | Hold time (repeated) start condition. After this period, the first clock pulse is generated | 4.0 | — | 0.6 | — | µs |
| $t_{SU, DAT}$ | Data set-up time | 250 | — | 100 | — | ns |
| $t_{HD, DAT}$ | Data hold time for I²C-bus devices | 0 | 3.45 | 0 | 0.9 | µs |
| $t_{SU, STO}$ | Set-up time for stop condition | 4.0 | — | 0.6 | — | µs |
| $t_R$ | Rise time of both SDA and SCL signals | — | 1000 | 20 + 0.1 $C_B$ (3) | 300 | ns |
| $t_F$ | Fall time of both SDA and SCL signals | — | 300 | 20 + 0.1 $C_B$ (3) | 300 | ns |
| $t_{BUF}$ | Bus-free time between a stop and start condition | 4.7 | — | 1.3 | — | µs |
| $C_B$ | Capacitive load for each bus line | — | 400 | — | 400 | pF |
| $t_{SP}$ | Pulse duration of spike suppressed | N/A | N/A | 0 | 50 | ns |

(1) All values refer to $V_{IHmin}$ and $V_{ILmax}$ levels.
(2) An SCL operating frequency of at least 1 kHz is recommended to avoid activating the I²C timeout function. See the *Timeout Function* section for details.
(3) $C_B$ = total capacitance of one bus line in pF.




(1) First rising edge of the SCL signal after Sr and after each acknowledge bit.

**Figure 2. Timing for High-Speed (Hs) Mode Devices on the I²C Bus**

## TIMING CHARACTERISTICS: SDA and SCL for Hs Mode(1)

At –40°C to +105°C, $AV_{DD}$ = 4.5 V to 5.5 V, $DV_{DD}$ = 2.7 V to 5.5 V, AGND = DGND = 0 V, and $IOV_{DD}$ = 2.7 V to 5.5 V, unless otherwise noted.

| PARAMETER | | $C_B$ = 10 pF to 100 pF | | $C_B$ = 400 pF | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{SCL}$ (2) | SCL clock frequency | 0 | 3.4 | 0 | 1.7 | MHz |
| $t_{SU, STA}$ | Setup time for (repeated) start condition | 160 | — | 160 | — | ns |
| $t_{HD, STA}$ | Hold time (repeated) start condition | 160 | — | 160 | — | ns |
| $t_{LOW}$ | Low period of the SCL clock | 160 | — | 320 | — | ns |
| $t_{HIGH}$ | High period of the SCL clock | 60 | — | 120 | — | ns |
| $t_{SU, DAT}$ | Data setup time | 10 | — | 10 | — | ns |
| $t_{HD, DAT}$ | Data hold time | 0 | 70 | 0 | 150 | ns |
| $t_{RCL}$ | Rise time of SCL signal | 10 | 40 | 20 | 80 | ns |
| $t_{RCL1}$ | Rise time of SCL signal after a repeated start condition and after an acknowledge bit | 10 | 80 | 20 | 160 | ns |
| $t_{FCL}$ | Fall time of SCL signal | 10 | 40 | 20 | 80 | ns |
| $t_{RDA}$ | Rise time of SDA signal | 10 | 80 | 20 | 160 | ns |
| $t_{FDA}$ | Fall time of SDA signal | 10 | 80 | 20 | 160 | ns |
| $t_{SU, STO}$ | Set-up time for stop condition | 160 | — | 160 | — | ns |
| $C_B$ (3) | Capacitive load for SDA and SCL lines | 10 | 100 | — | 400 | pF |
| $t_{SP}$ | Pulse width of spike suppressed | 0 | 10 | 0 | 10 | ns |

(1) All values refer to $V_{IHmin}$ and $V_{ILmax}$ levels.
(2) An SCL operating frequency of at least 1 kHz is recommended to avoid activating the I²C timeout function. See the *Timeout Function* section for details.
(3) For bus line loads where $C_B$ is between 100 pF and 400 pF, the timing parameters must be linearly interpolated.

## SPI TIMING DIAGRAMS

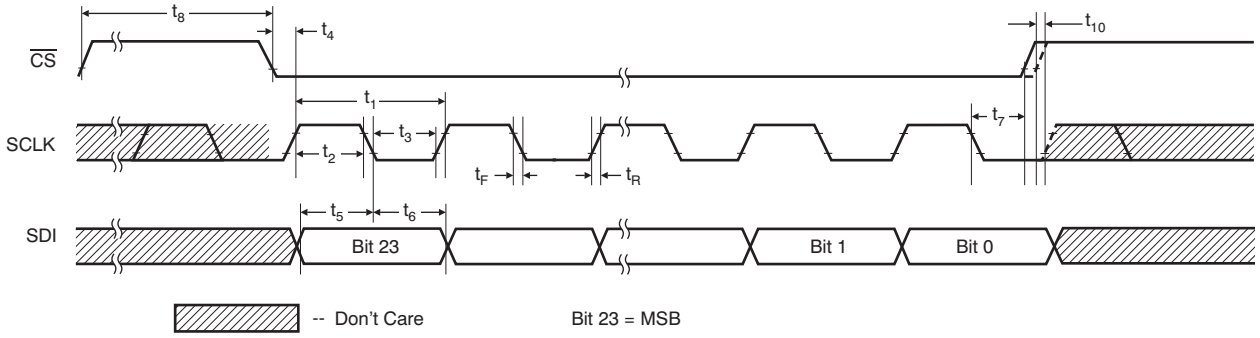



**Figure 3. SPI Single-Chip Write Operation**

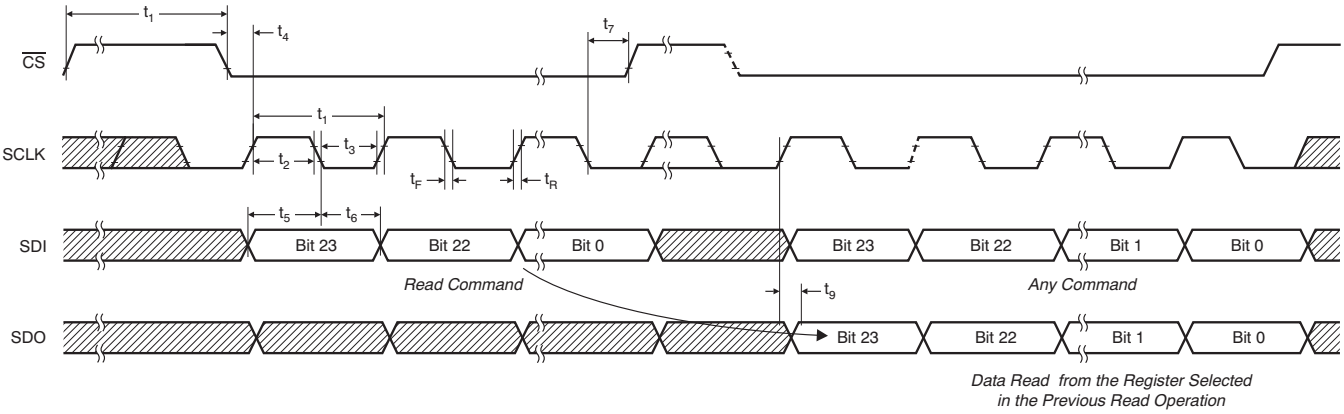



**Figure 4. SPI Single-Chip Read Operation**

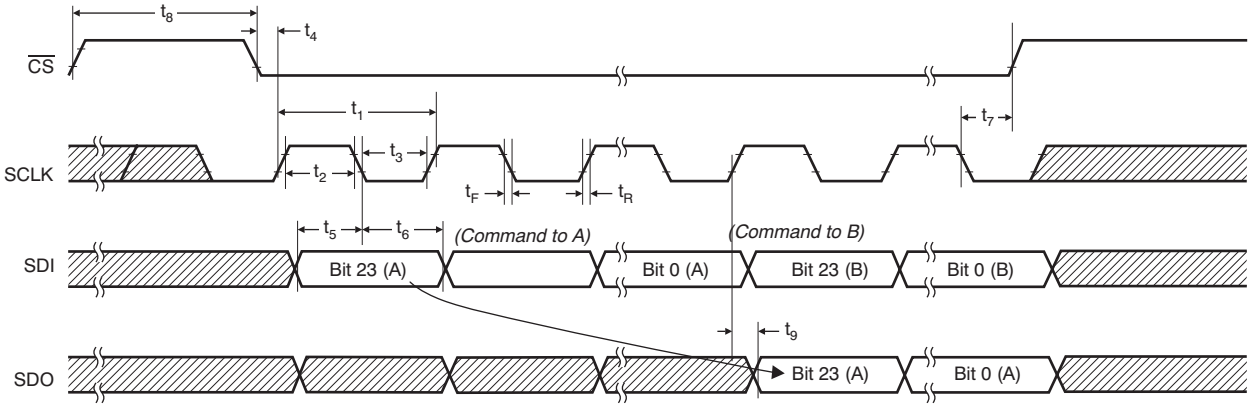



**Figure 5. Daisy-Chain Operation: Two Devices**

## TIMING CHARACTERISTICS: SPI Bus(1)(2)

At –40°C to +105°C, $AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, AGND = DGND = 0 V, and $IOV_{DD}$ = 3.0 V to 5.5 V, unless otherwise noted.

| PARAMETER | | LIMIT AT $T_{MIN}$, $T_{MAX}$ MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{SCLK}$ | Clock frequency, $T_A$ = –40°C to +105°C | | 50 | MHz |
| | Clock frequency, $T_A$ = –40°C to +125°C | | 25 | MHz |
| $t_1$ | SCLK cycle time | 20 | | ns |
| $t_2$ | SCLK high time | 8 | | ns |
| $t_3$ | SCLK low time | 8 | | ns |
| $t_4$ | $\overline{CS}$ falling edge to SCLK rising edge setup time | 5 | | ns |
| $t_5$ | Input data setup time | 5 | | ns |
| $t_6$ | Input data hold time | 4 | | ns |
| $t_7$ | SCLK falling edge to $\overline{CS}$ rising edge | 10 | | ns |
| $t_8$ | Minimum $\overline{CS}$ high time | 30 | | ns |
| $t_9$ | Output data valid time | 3 | 20 | ns |
| $t_{10}$ | $\overline{CS}$ rising to next SCLK rising edge | 3 | | ns |

(1) Specified by design; not production tested.
(2) SDO loaded with 10-pF load capacitance for SDO timing specifications, $t_R$ = $t_F$ ≤ 5 ns.

## TYPICAL CHARACTERISTICS: DAC

At +25°C, unless otherwise noted.

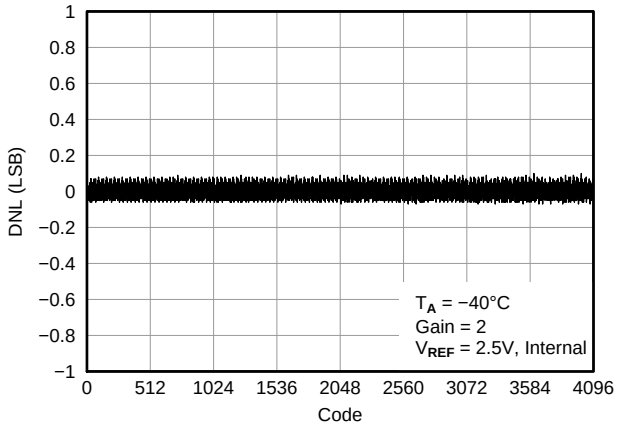



**Figure 6. DIFFERENTIAL LINEARITY ERROR vs CODE**

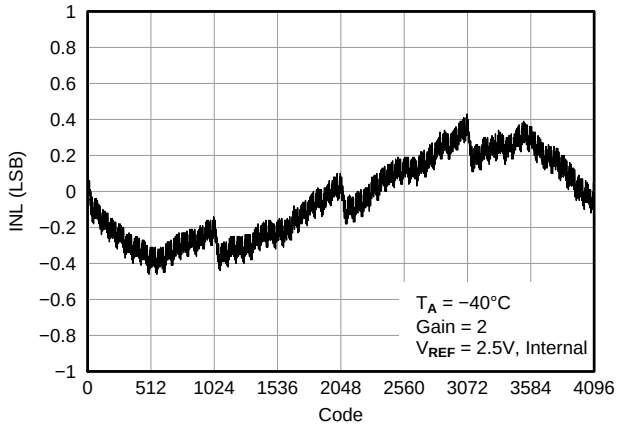



**Figure 7. LINEARITY ERROR vs CODE**

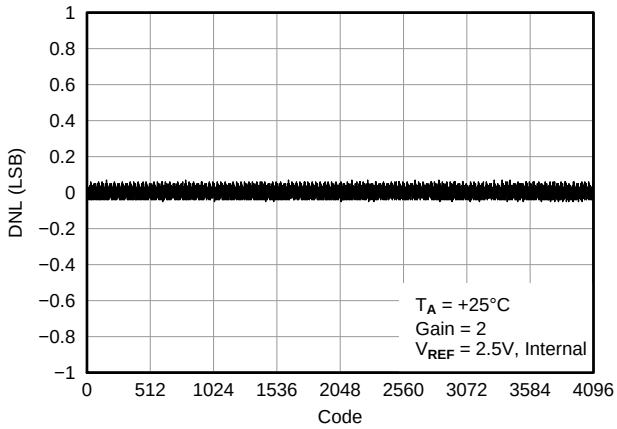



**Figure 8. DIFFERENTIAL LINEARITY ERROR vs CODE**

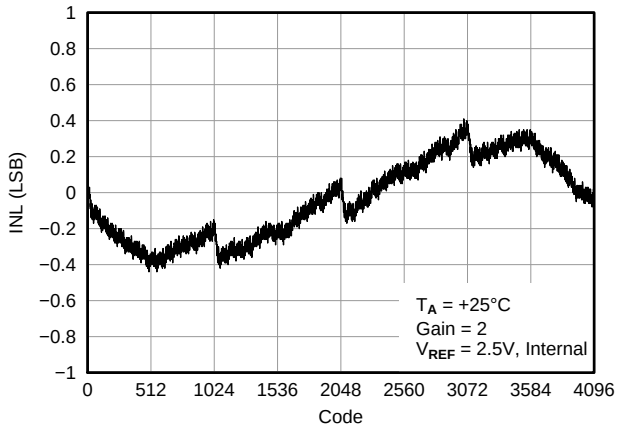



**Figure 9. LINEARITY ERROR vs CODE**

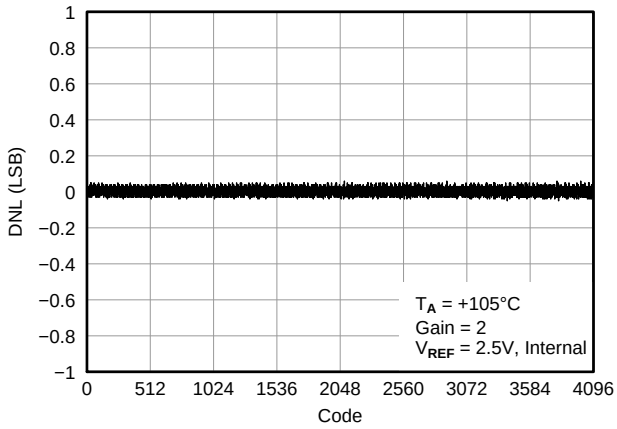



**Figure 10. DIFFERENTIAL LINEARITY ERROR vs CODE**

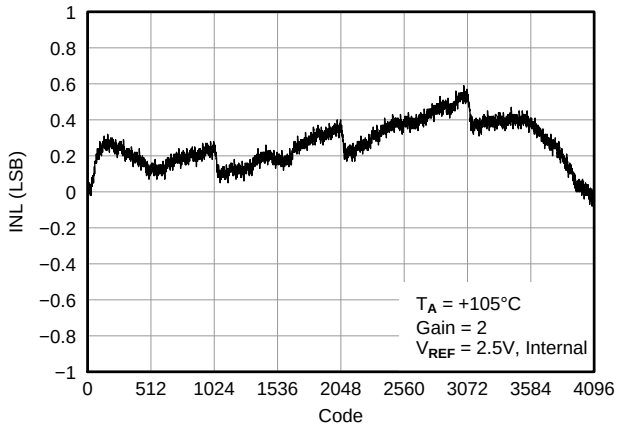



**Figure 11. LINEARITY ERROR vs CODE**

## TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

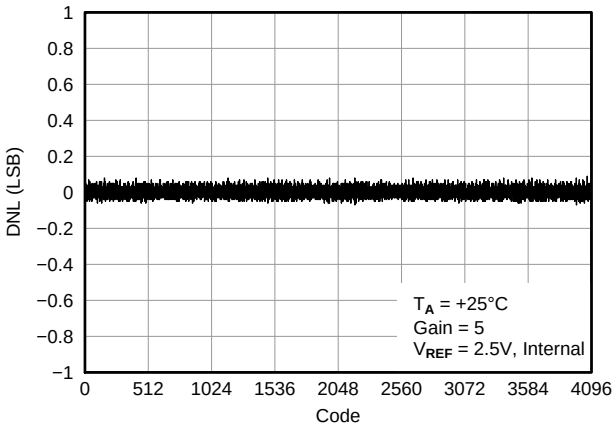



**Figure 12. DIFFERENTIAL LINEARITY ERROR vs CODE**

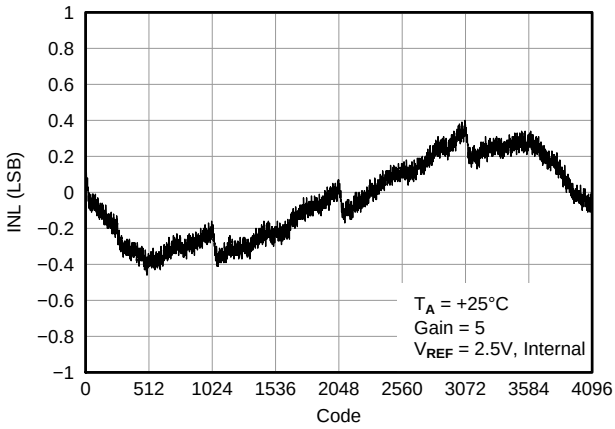



**Figure 13. LINEARITY ERROR vs CODE**

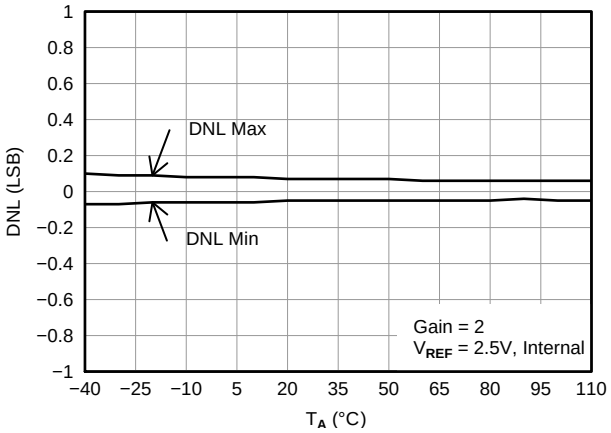



**Figure 14. DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE**

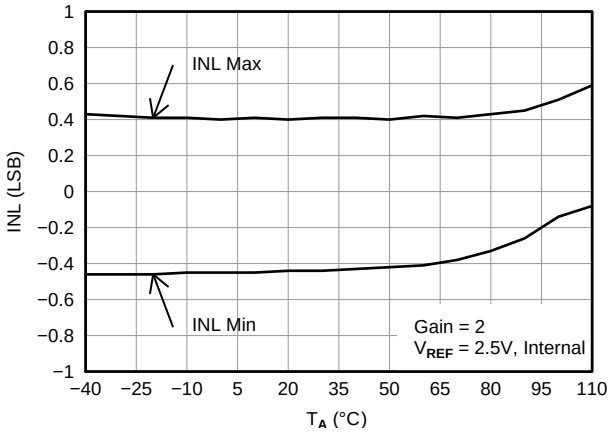



**Figure 15. LINEARITY ERROR vs TEMPERATURE**

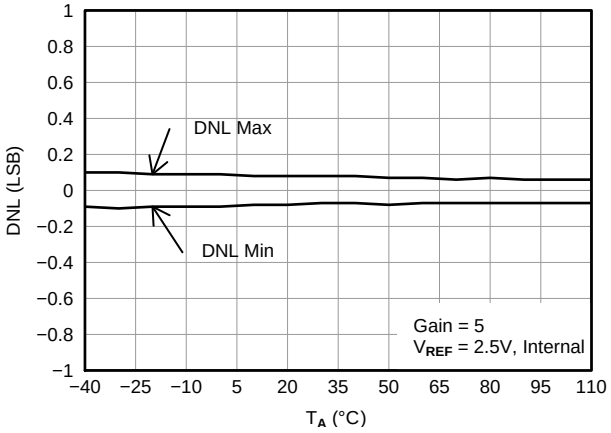



**Figure 16. DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE**

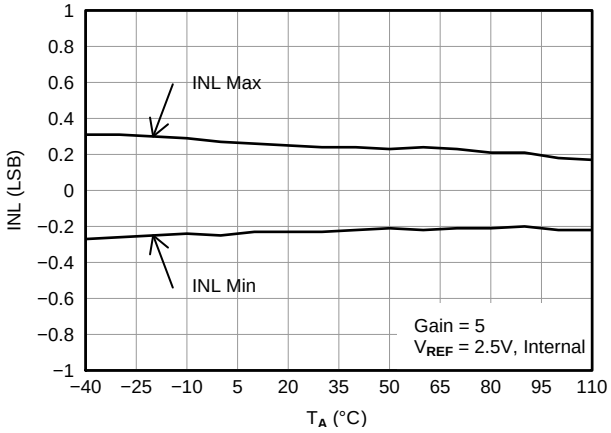



**Figure 17. LINEARITY ERROR vs TEMPERATURE**

## TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

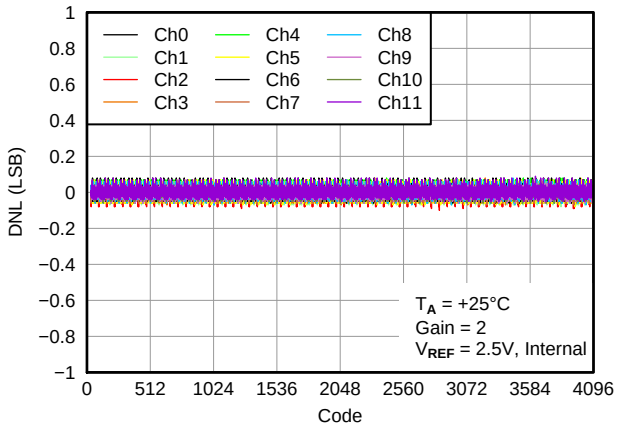



**Figure 18. DIFFERENTIAL LINEARITY ERROR vs CODE**

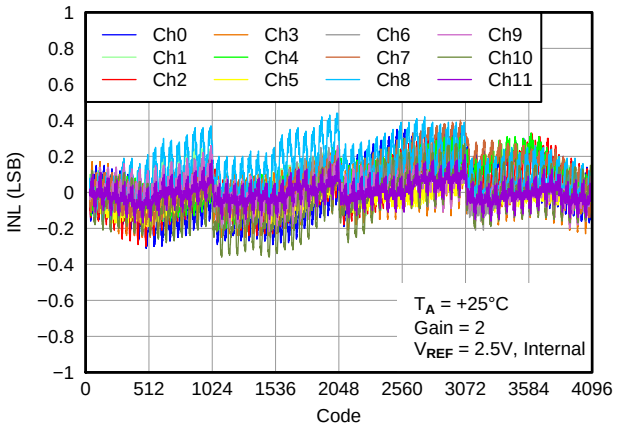



**Figure 19. LINEARITY ERROR vs CODE**

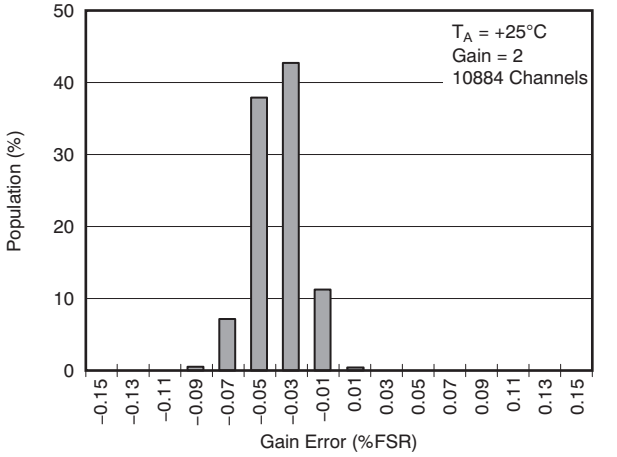



**Figure 20. GAIN ERROR**

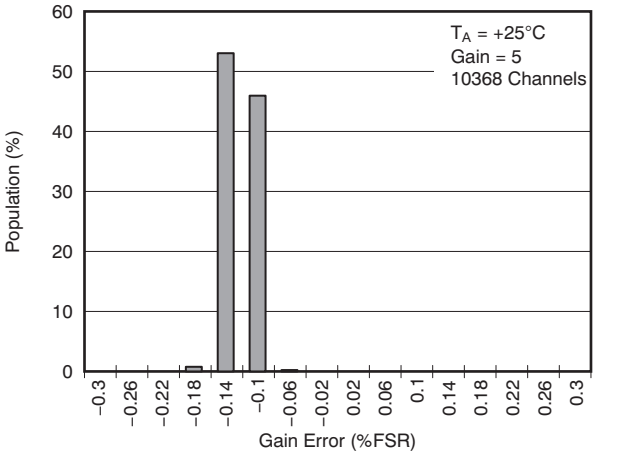



**Figure 21. GAIN ERROR**

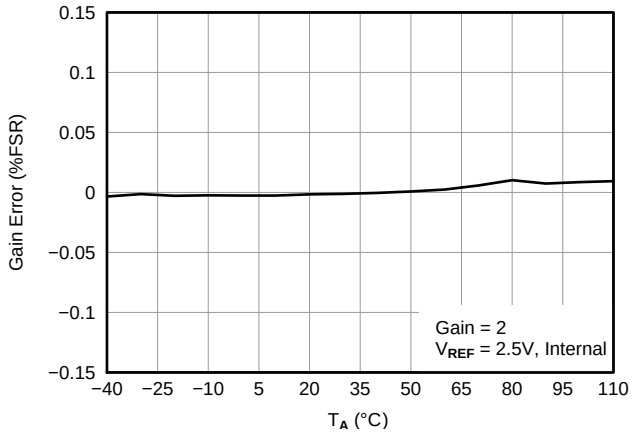



**Figure 22. GAIN ERROR vs TEMPERATURE**

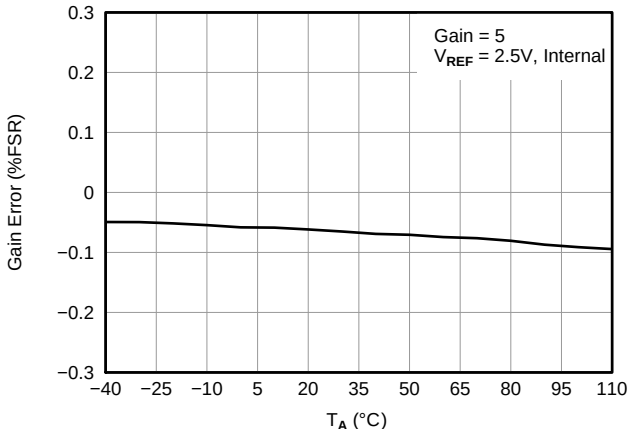



**Figure 23. GAIN ERROR vs TEMPERATURE**

## TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

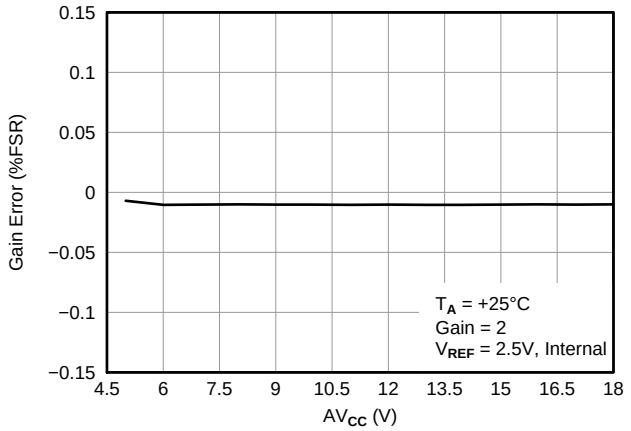



**Figure 24. GAIN ERROR vs SUPPLY**

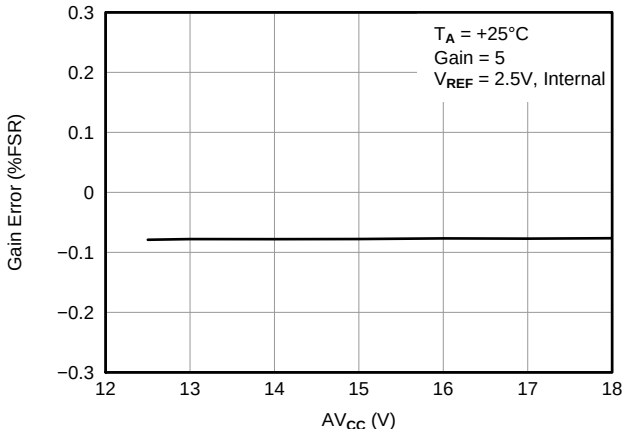



**Figure 25. GAIN ERROR vs SUPPLY**

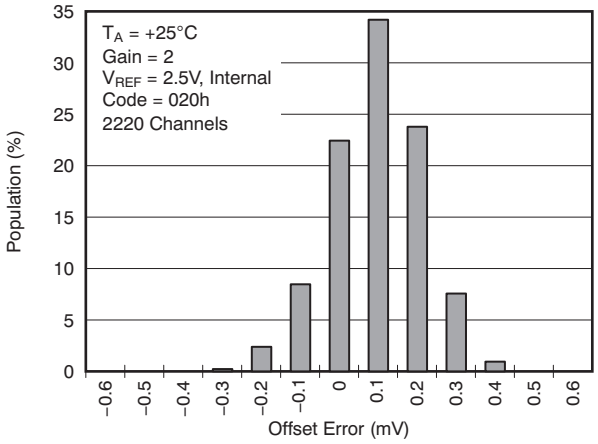



**Figure 26. OFFSET VOLTAGE**

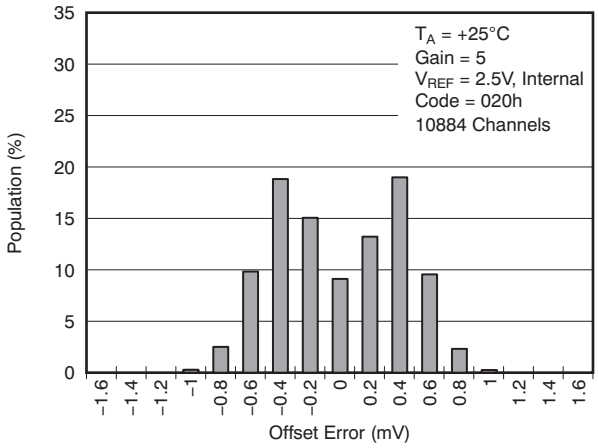



**Figure 27. OFFSET VOLTAGE**

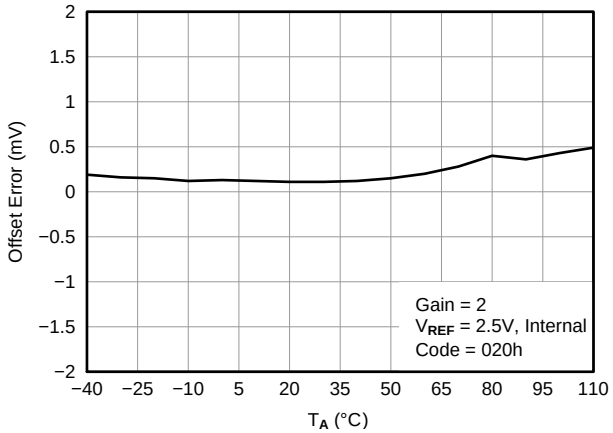



**Figure 28. OFFSET VOLTAGE vs TEMPERATURE**

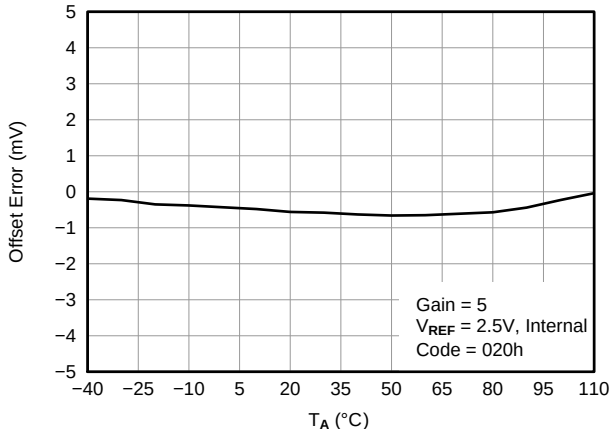



**Figure 29. OFFSET VOLTAGE vs TEMPERATURE**

## TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

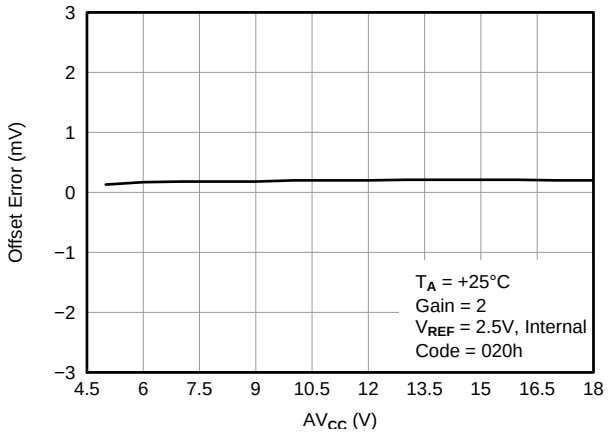



**Figure 30. OFFSET VOLTAGE vs SUPPLY VOLTAGE**

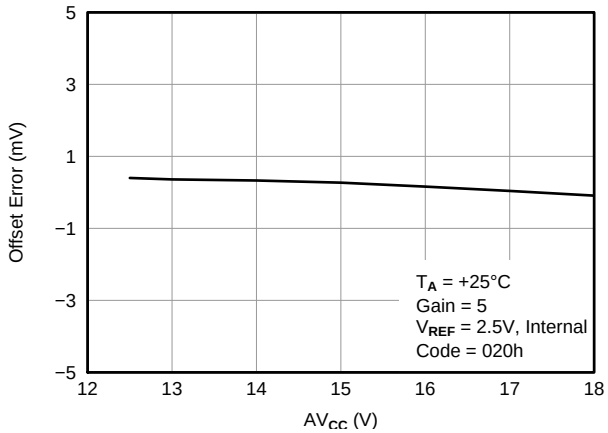



**Figure 31. OFFSET VOLTAGE vs SUPPLY VOLTAGE**

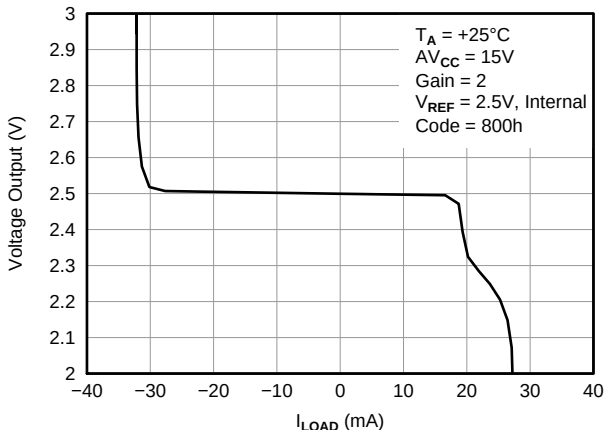



**Figure 32. OUTPUT VOLTAGE vs OUTPUT CURRENT**

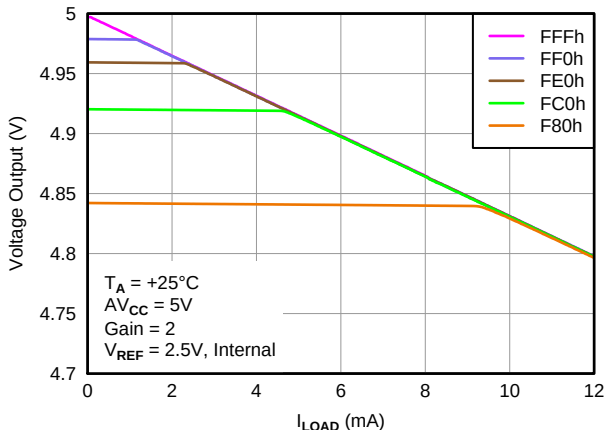



**Figure 33. OUTPUT VOLTAGE vs SOURCE CURRENT CAPABILITY**

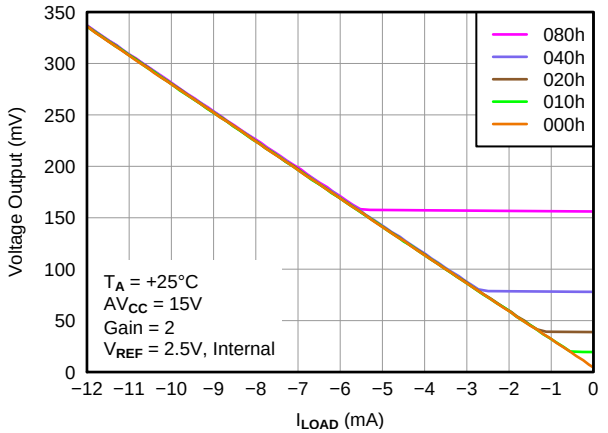



**Figure 34. OUTPUT VOLTAGE vs SINK CURRENT CAPABILITY**

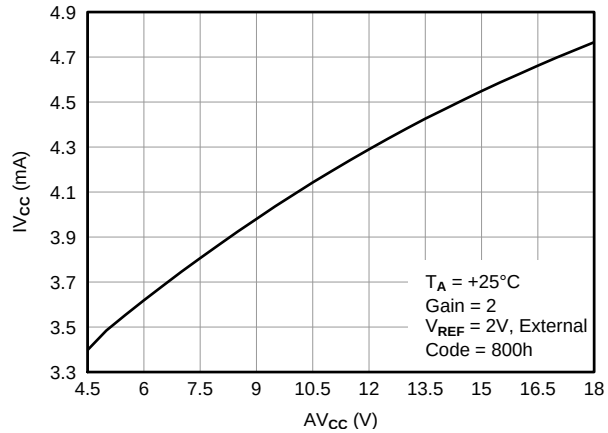



**Figure 35. DAC SUPPLY CURRENT vs DAC SUPPLY VOLTAGE**

## TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

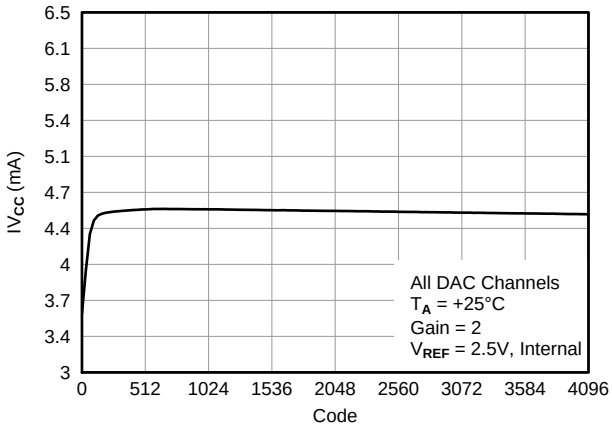



**Figure 36. SUPPLY CURRENT vs DAC CODE**

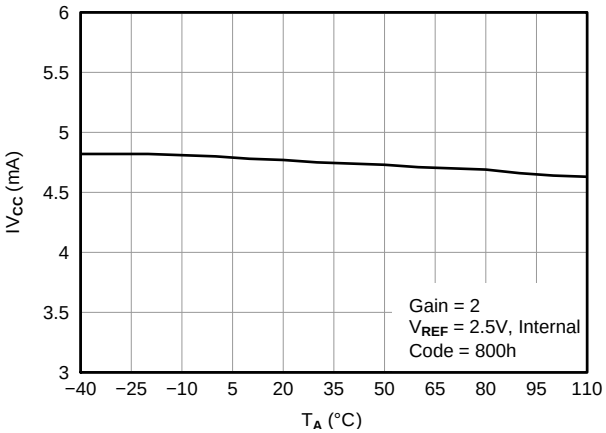



**Figure 37. SUPPLY CURRENT vs TEMPERATURE**

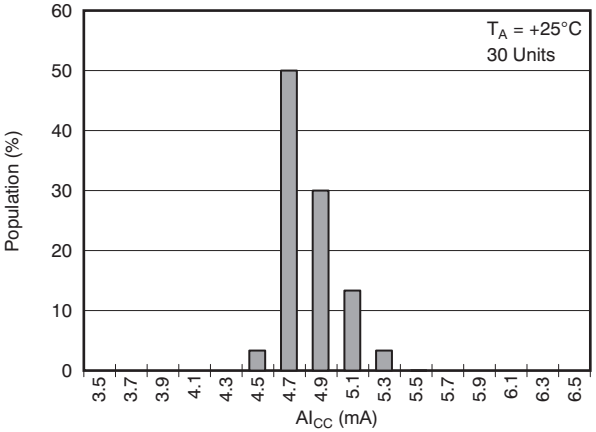



**Figure 38. DAC SUPPLY CURRENT**

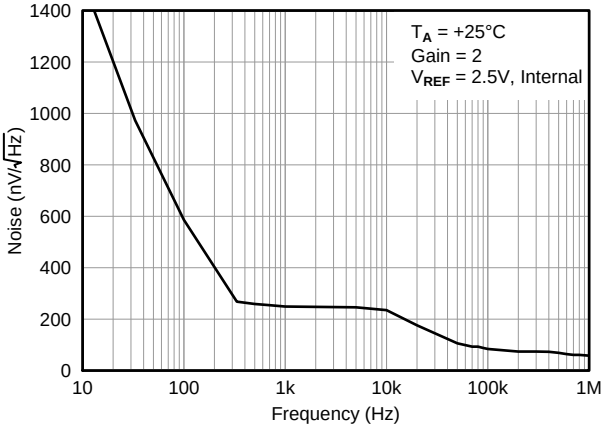



**Figure 39. DAC NOISE VOLTAGE vs FREQUENCY**

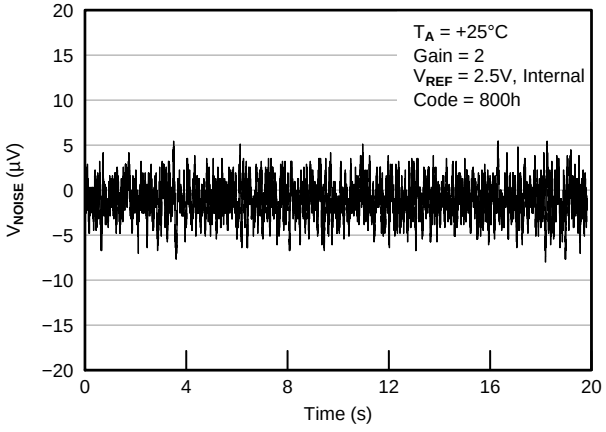



**Figure 40. DAC NOISE (0.1 Hz to 10 Hz)**

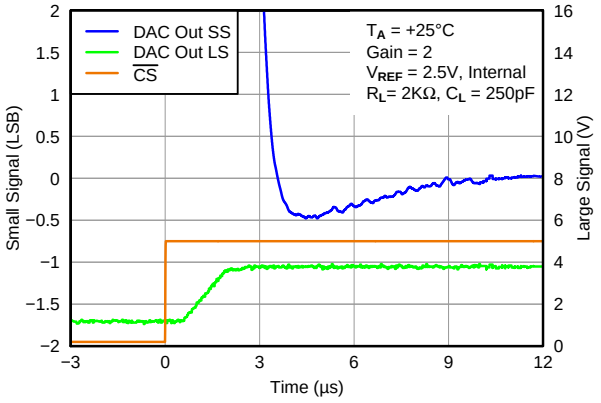



**Figure 41. SETTLING TIME RISING EDGE**

## TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

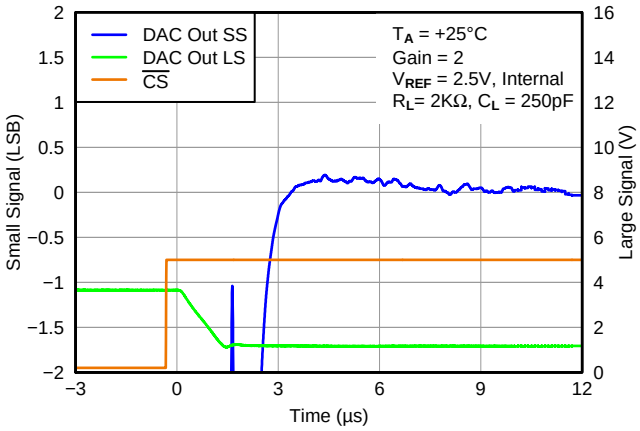



**Figure 42. SETTLING TIME FALLING EDGE**

## TYPICAL CHARACTERISTICS: ADC

At +25°C, unless otherwise noted.

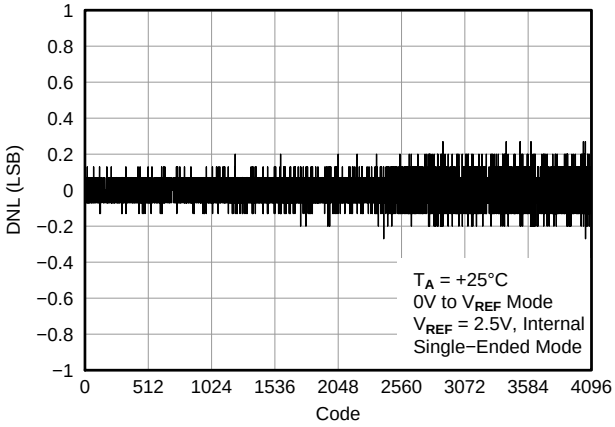



**Figure 43. DIFFERENTIAL LINEARITY ERROR vs CODE**

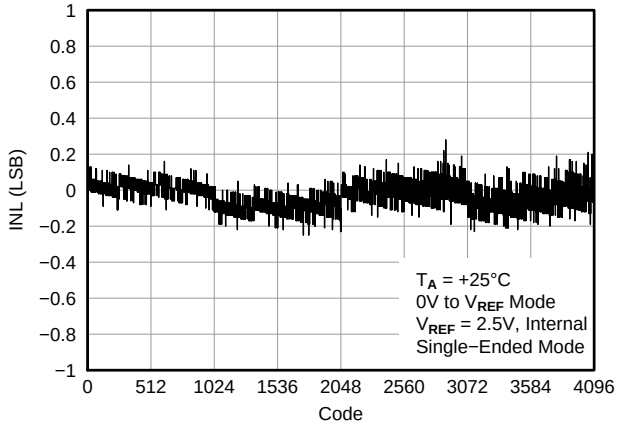



**Figure 44. LINEARITY ERROR vs CODE**

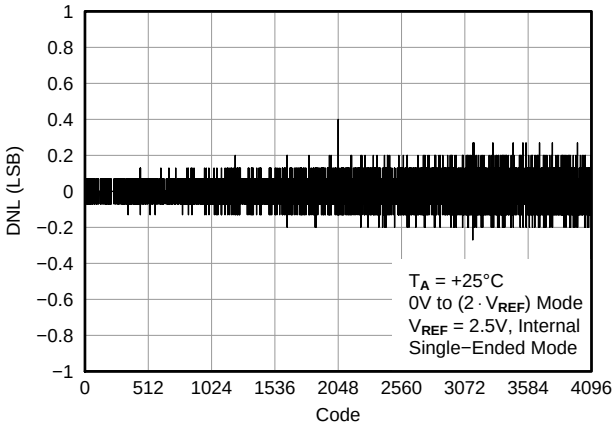



**Figure 45. DIFFERENTIAL LINEARITY ERROR vs CODE**

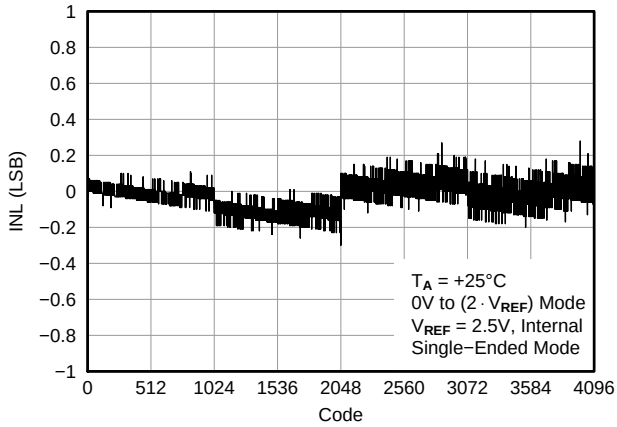



**Figure 46. LINEARITY ERROR vs CODE**

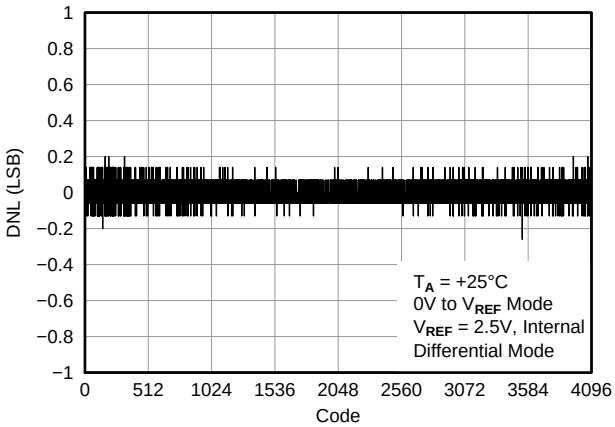



**Figure 47. DIFFERENTIAL LINEARITY ERROR vs CODE**

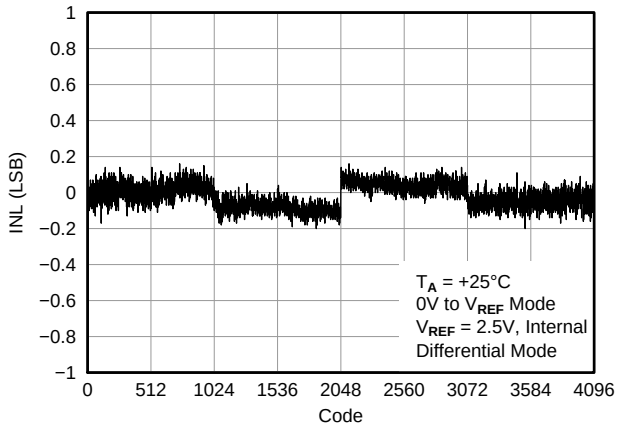



**Figure 48. LINEARITY ERROR vs CODE**

## TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

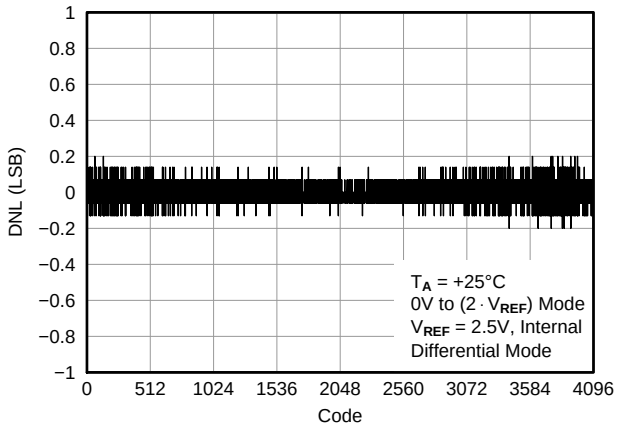



**Figure 49. DIFFERENTIAL LINEARITY ERROR vs CODE**

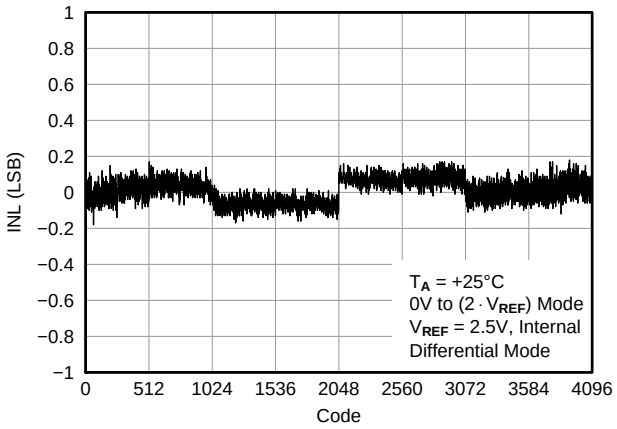



**Figure 50. LINEARITY ERROR vs CODE**

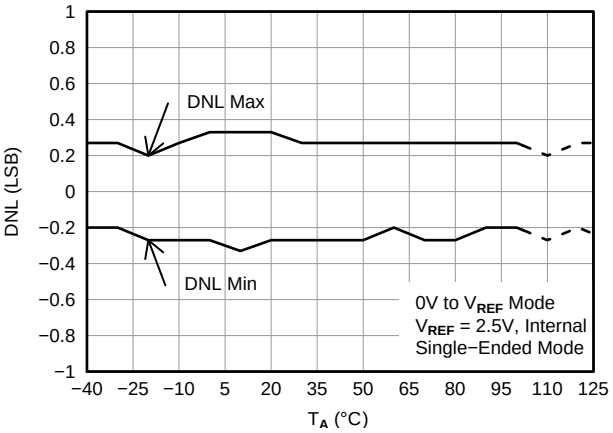



**Figure 51. DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE**

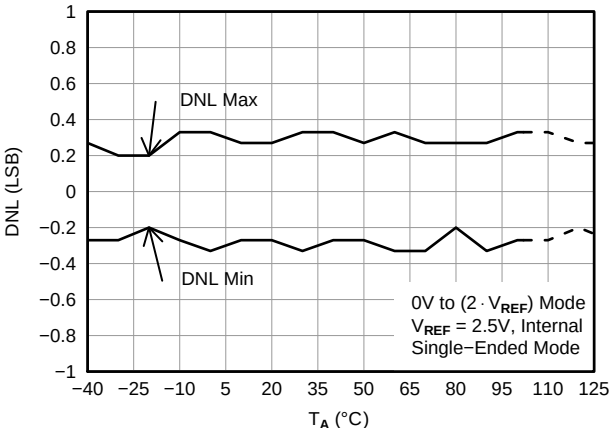



**Figure 52. DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE**

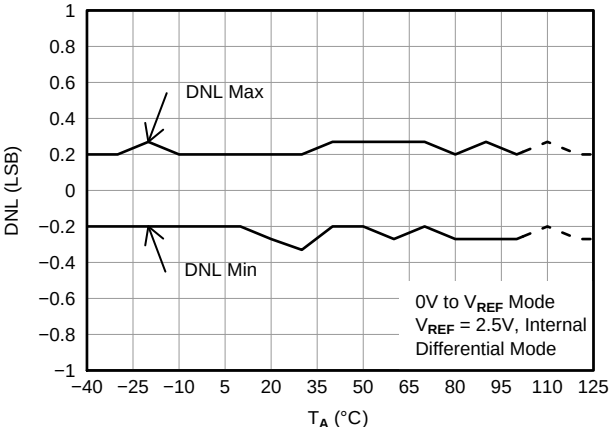



**Figure 53. DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE**

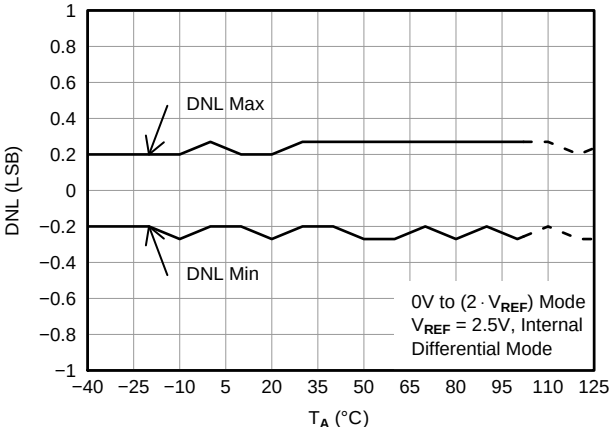



**Figure 54. DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE**

## TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

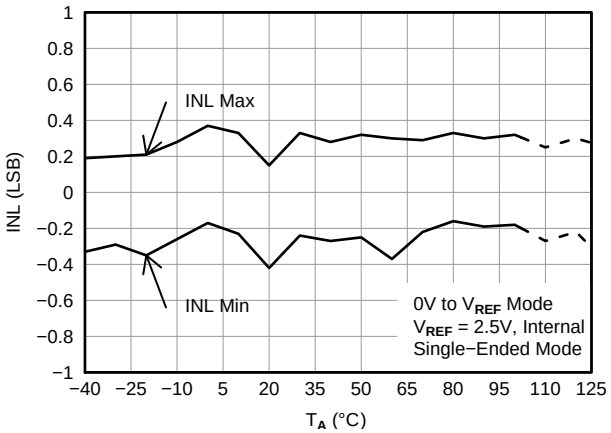



**Figure 55. LINEARITY ERROR vs TEMPERATURE**

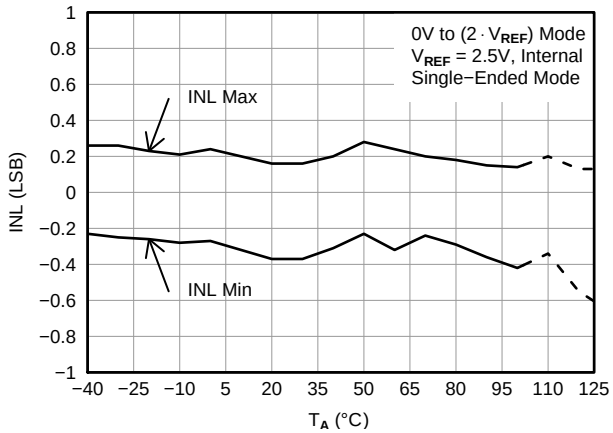



**Figure 56. LINEARITY ERROR vs TEMPERATURE**

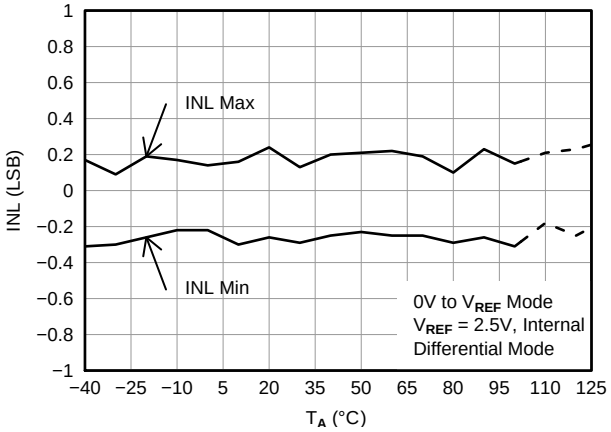



**Figure 57. LINEARITY ERROR vs TEMPERATURE**

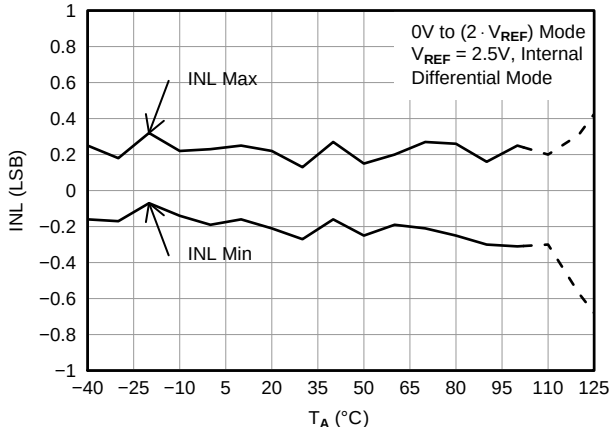



**Figure 58. LINEARITY ERROR vs TEMPERATURE**

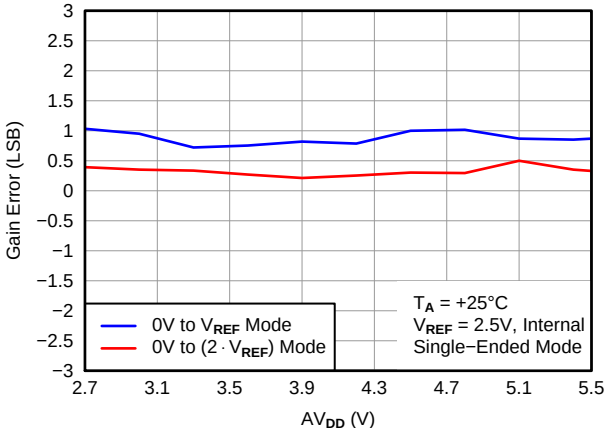



**Figure 59. GAIN ERROR vs SUPPLY**

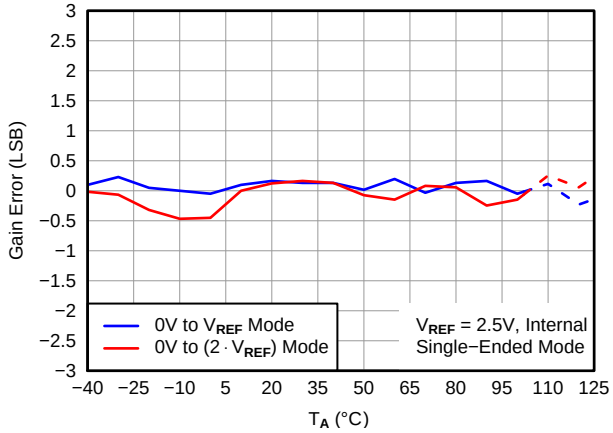



**Figure 60. GAIN ERROR vs TEMPERATURE**

## TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

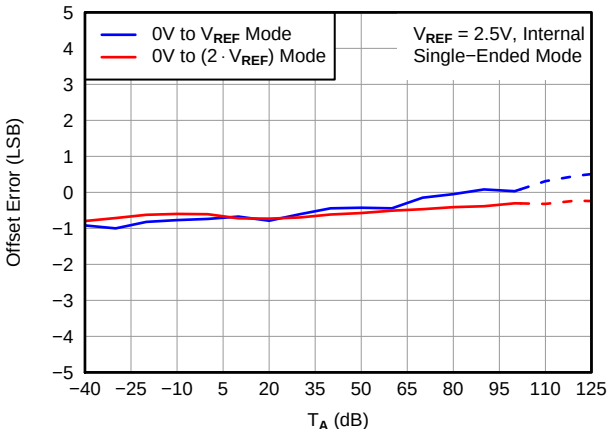



**Figure 61. OFFSET vs TEMPERATURE**

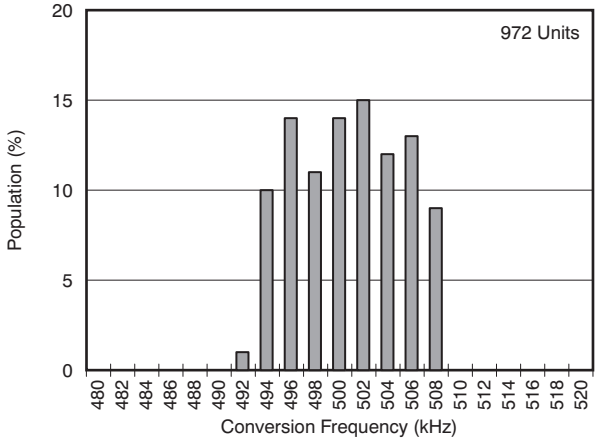



**Figure 62. CONVERSION FREQUENCY**

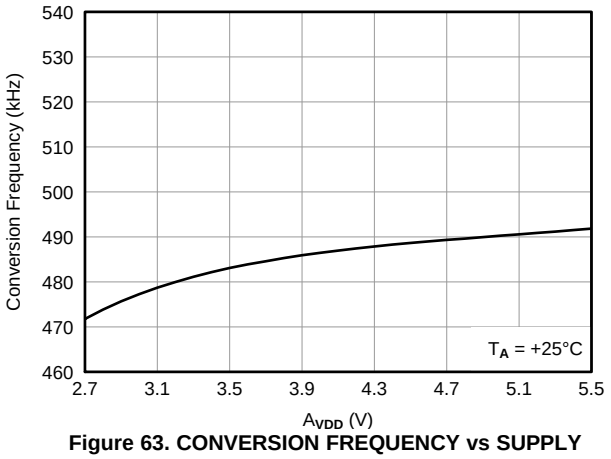



**Figure 63. CONVERSION FREQUENCY vs SUPPLY**

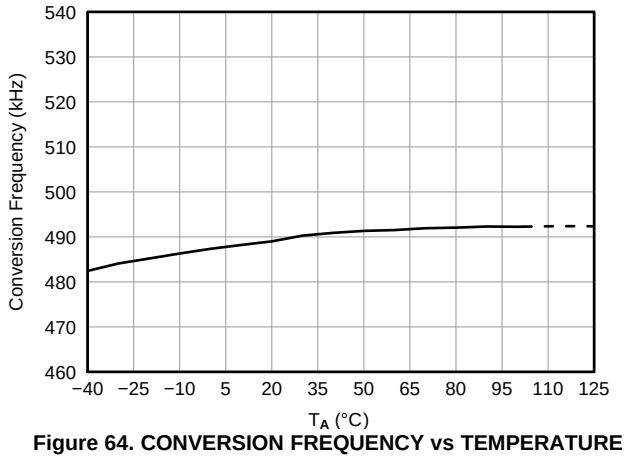



**Figure 64. CONVERSION FREQUENCY vs TEMPERATURE**

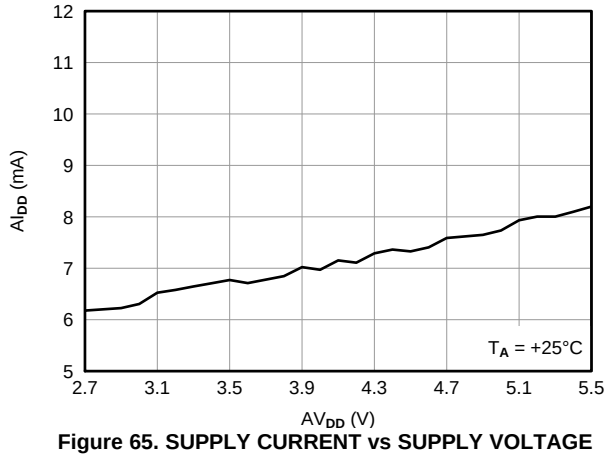



**Figure 65. SUPPLY CURRENT vs SUPPLY VOLTAGE**

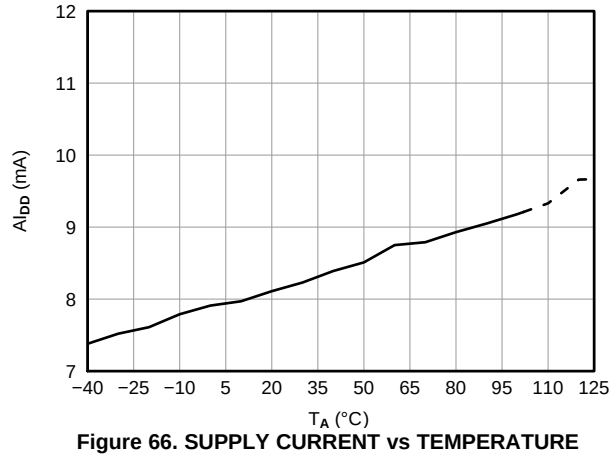



**Figure 66. SUPPLY CURRENT vs TEMPERATURE**

## TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

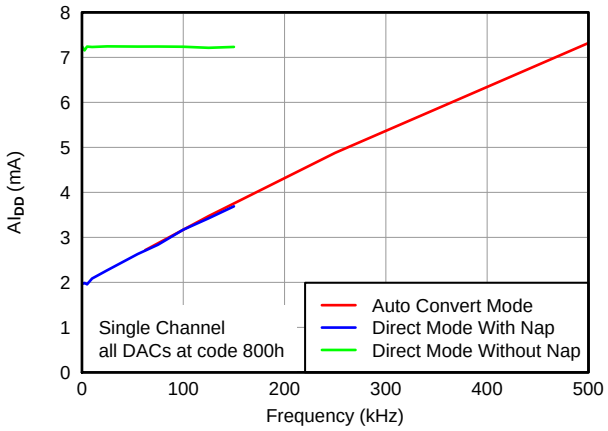



**Figure 67. SUPPLY CURRENT vs CONVERSION RATE**

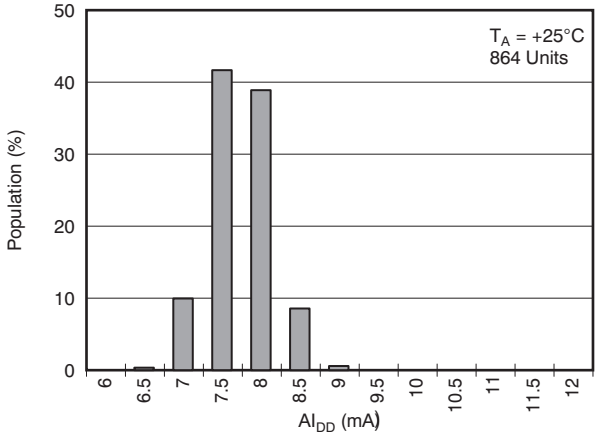



**Figure 68. COMBINED $AV_{DD}$ AND $DV_{DD}$ SUPPLY CURRENT**

## TYPICAL CHARACTERISTICS: INTERNAL REFERENCE

At +25°C, unless otherwise noted.

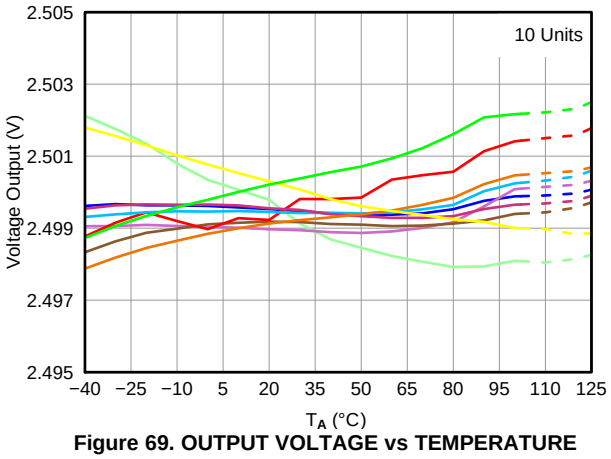



**Figure 69. OUTPUT VOLTAGE vs TEMPERATURE**

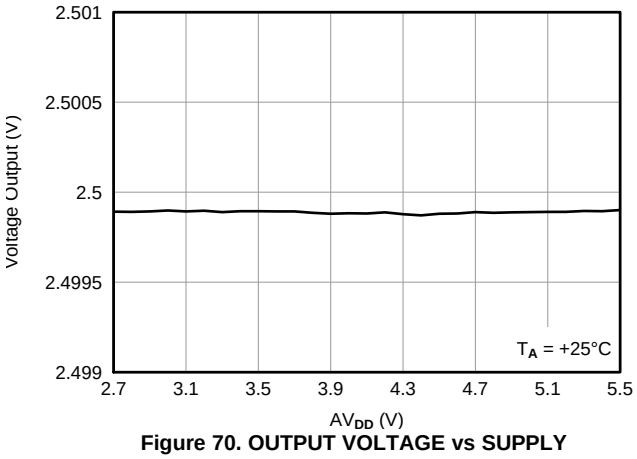



**Figure 70. OUTPUT VOLTAGE vs SUPPLY**

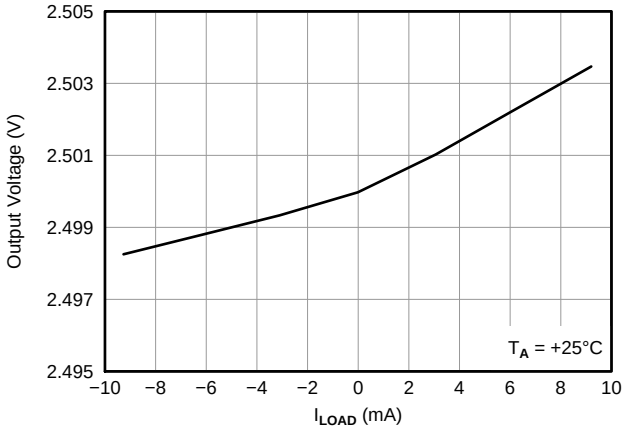



**Figure 71. OUTPUT VOLTAGE vs OUTPUT CURRENT**

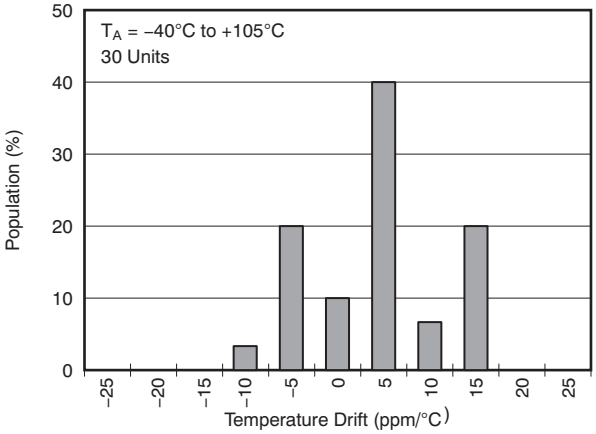



**Figure 72. OUTPUT VOLTAGE DRIFT**

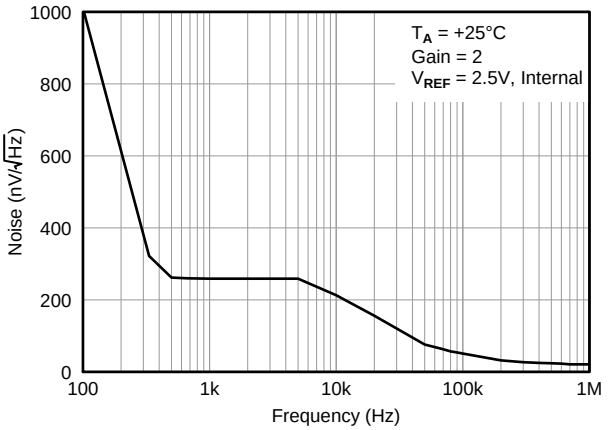



**Figure 73. INTERNAL REFERENCE NOISE vs FREQUENCY**

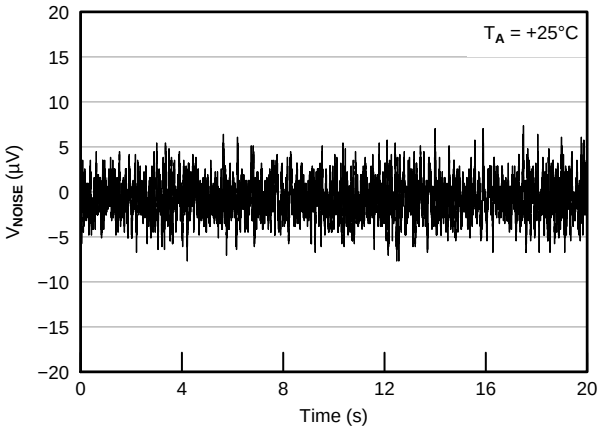



**Figure 74. INTERNAL REFERENCE NOISE (0.1 Hz to 10 Hz)**

## TYPICAL CHARACTERISTICS: TEMPERATURE SENSOR

At +25°C, unless otherwise noted.

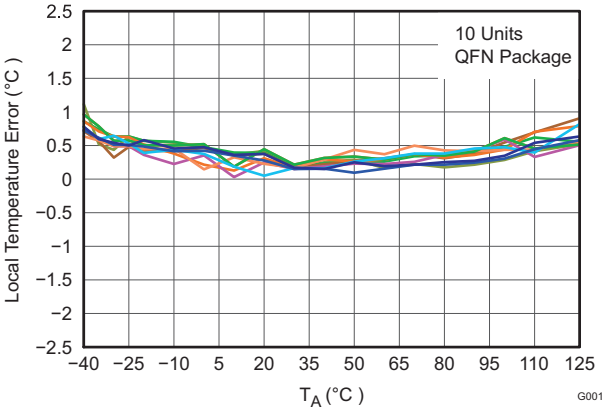



**Figure 75. LOCAL TEMPERATURE ERROR vs TEMPERATURE**

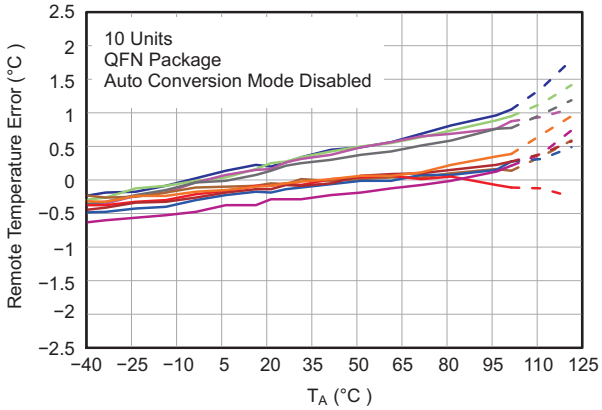



**Figure 76. REMOTE TEMPERATURE ERROR vs TEMPERATURE**

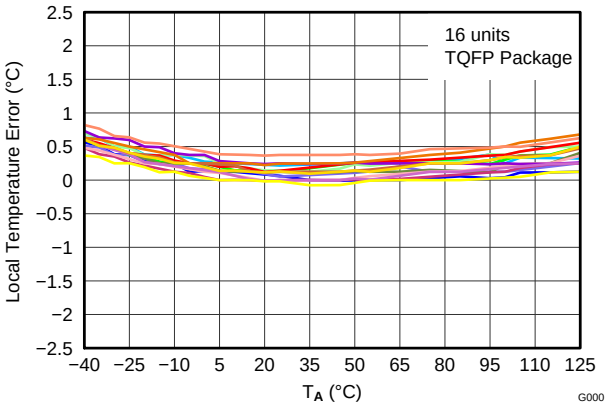



**Figure 77. LOCAL TEMPERATURE ERROR vs TEMPERATURE**

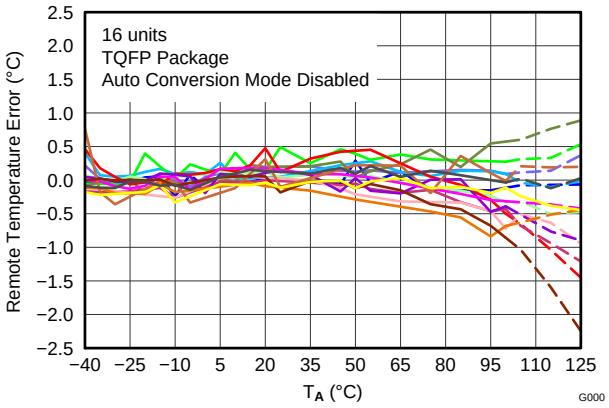



**Figure 78. REMOTE TEMPERATURE ERROR vs TEMPERATURE**

## TYPICAL CHARACTERISTICS: DIGITAL INPUTS

At +25°C, unless otherwise noted.

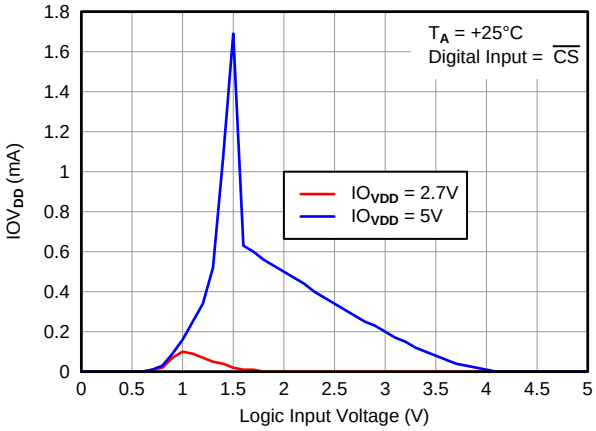



**Figure 79. SUPPLY CURRENT vs INPUT VOLTAGE**

# THEORY OF OPERATION

## ADC OVERVIEW

The AMC7812B has two analog-to-digital converters (ADCs): a primary ADC and a secondary ADC. The primary ADC features a 16-channel multiplexer, an on-chip track-and-hold, and a successive approximation register (SAR) ADC based on a capacitive digital-to-analog converter (DAC). This ADC runs at 500 kSPS and converts the analog channel inputs, CH0 to CH15. The analog input range for the device can be selected as 0 V to $V_{REF}$ or 0 V to (2 × $V_{REF}$). The analog input can be configured for either single-ended or differential signals. The device has an on-chip 2.5-V reference that can be disabled when an external reference is preferred. If the internal ADC reference is to be used elsewhere in the system, the output must first be buffered. The various monitored and uncommitted input signals are multiplexed into the ADC. The secondary ADC is a part of the temperature-sensing function that converts the analog temperature signals.

## ANALOG INPUTS

The device has 16 uncommitted analog inputs; 12 of these inputs (CH4 to CH15) are single-ended. The inputs for CH0 to CH3 can be configured as four single-ended inputs or two fully-differential channels, depending on the setup of the ADC channel registers, ADC Channel Register 0 and ADC Channel Register 1. See the *Registers* section for details. Figure 80 shows the device equivalent input circuit. The (peak) input current through the analog inputs depends on the sample rate, input voltage, and source impedance. The current into the device charges the internal capacitor array during the sample period. After this capacitance is fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the acquisition time. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

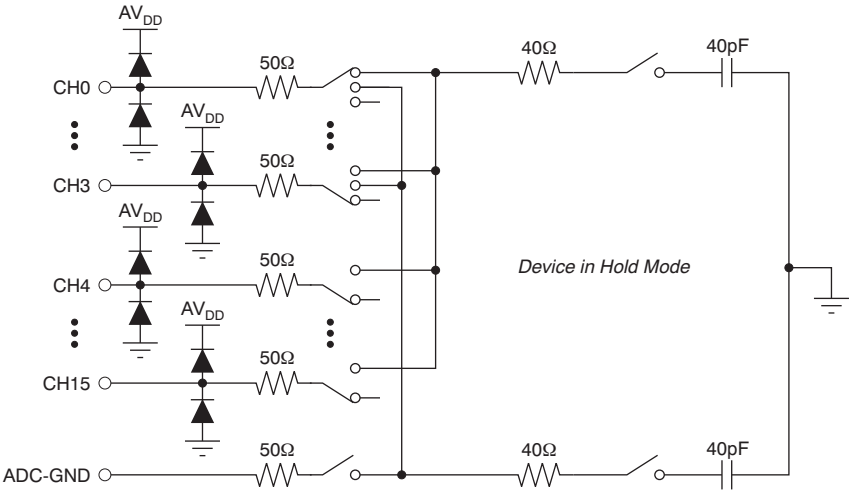



**Figure 80. Equivalent Input Circuit**

### Single-Ended Analog Input

In applications where the signal source has high impedance, TI recommends buffering the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 V to $V_{REF}$ or 0 V to (2 × $V_{REF}$). In 2 × $V_{REF}$ mode, the input is effectively divided by two before the conversion takes place. Note that the voltage with respect to GND on the ADC analog input pins cannot exceed $AV_{DD}$.

### Fully-Differential Input

When the device is configured as a differential input, the differential signal is defined as $V_{DM}$, as shown in Figure 81(a). The differential signal is the equivalent of the difference between the V1 and V2 signals, as shown in Figure 81(b). The common-mode input $V_{COMMON}$ is equal to (V1 + V2) / 2.

When the conversion occurs, only the differential mode voltage ($V_{DM}$) is converted; the common-mode voltage ($V_{COMMON}$) is rejected. This process results in a virtually noise-free signal with a maximum amplitude of $-V_{REF}$ to $+V_{REF}$ for the $V_{REF}$ range, or (–2 × $V_{REF}$) to (+2 × $V_{REF}$) for the (2 × $V_{REF}$) range. The results are stored in straight binary or twos complement format.

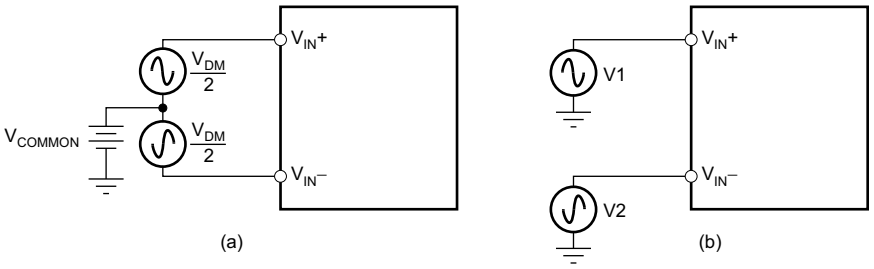



**Figure 81. Fully-Differential Analog Input**

## PRIMARY ADC OPERATION

This section describes the operation of the primary ADC.

### ADC Trigger Signals (see AMC configuration register 0)

The ADC can be triggered externally by the falling edge of the external trigger $\overline{CNVT}$, or internally by writing to the ICONV bit in AMC Configuration Register 0. The ADC channel registers specify which external analog channel is converted.

When a new trigger activates, the ADC stops any existing conversion immediately and starts a new cycle. For example, the ADC is programmed to sample channel 0 to channel 3 repeatedly (auto-mode). During the conversion of channel 1, an external trigger is activated. The ADC stops converting channel 1 immediately and starts converting channel 0 again, instead of proceeding to convert channel 2.

### Conversion Mode

Two types of ADC conversions are available: direct mode and auto mode. The conversion mode (CMODE) bit of the AMC configuration 0 register specifies the conversion mode.

In direct mode, each analog channel within the specified group is converted a single time. After the last channel is converted, the ADC enters an idle state and waits for a new trigger.

Auto mode is a continuous operation. In auto mode, each analog channel within the specified group is converted sequentially and repeatedly.

The flow chart of the ADC conversion sequence in Figure 82 shows the conversion process.

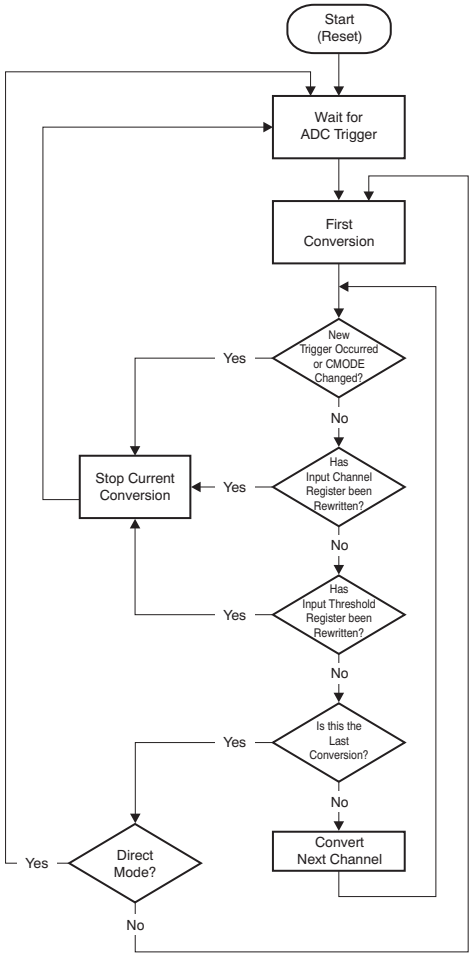



**Figure 82. ADC Conversion Sequence**

The current conversion cycle stops immediately if:

- A new trigger is issued.
- The conversion mode changes.
- Either ADC channel register is rewritten.
- Any of the analog input threshold registers are rewritten.

When a new external or internal trigger activates, the ADC starts a new conversion cycle. The internal trigger should not be issued at the same time the conversion mode is changed. If a '1' is simultaneously written to the ICONV bit when changing the CMODE bit to '0' or '1', the current conversion stops and immediately returns to the *wait for ADC trigger* state.

### Double-Buffered ADC Data Registers

The host can access all 16, double-buffered ADC data registers, as shown in Figure 83. The conversion result from the analog input with channel address *n* (where n = 0 to 15) is stored in the ADC-*n*-data register. When the conversion of an individual channel completes, the data are immediately transferred into the corresponding ADC-*n* temporary (TMPRY) register, the first stage of the data buffer. When the conversion of the last channel completes, all data in the ADC-*n* TMPRY registers are simultaneously transferred into the corresponding ADC-*n*-data registers, the second stage of the data buffer. However, if a data transfer is in progress between any ADC-*n*-data register and the AMC shift register, no ADC-*n*-data registers are updated until the data transfer is complete. The conversion result from channel address *n* is stored in the ADC-*n*-data register. For example, the result from channel 0 is stored in the ADC-0-data register, and the result from channel 3 is stored in the ADC-3-data register.

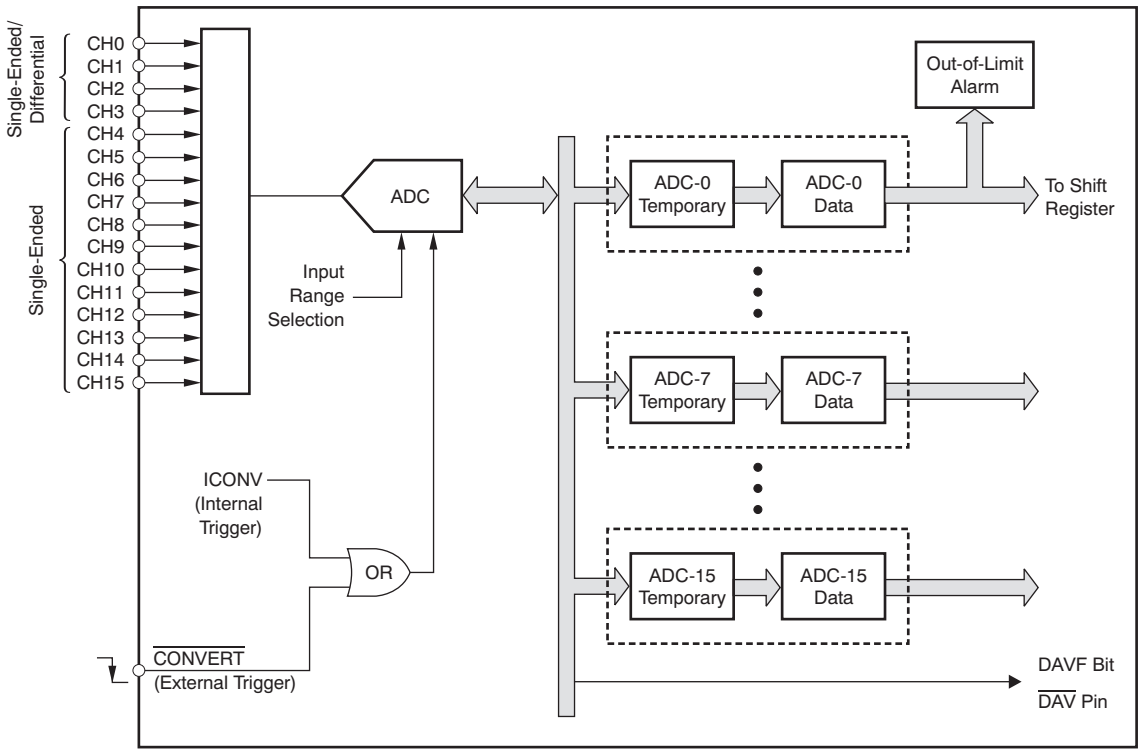



**Figure 83. Double-Buffered ADC Structure**

### ADC Data Format

For a single-ended input, the conversion result is stored in straight binary format. For a differential input, the results are stored in twos complement format.

### SCLK Clock Noise Reduction

To avoid noise caused by the bus clock, TI recommends that no bus clock activity occur for at least the conversion process time immediately after the ADC conversion starts.

### Programmable Conversion Rate

The maximum conversion rate is 500 kSPS for a single channel in auto mode, as shown in Table 1. The conversion rate is programmable through the CONV-RATE-[1:0] bits of the AMC configuration register 1. When more than one channel is selected, the conversion rate is divided by the number of channels selected in ADC channel register 0 and ADC channel register 1. In auto mode, the CONV-RATE-[1:0] bits determine the actual conversion rate. In direct mode, the CONV-RATE-[1:0] bits limit the maximum possible conversion rate. The actual conversion rate in direct mode is determined by the rate of the conversion trigger. Note that when a trigger is issued, there may be a delay of up to 4 µs to internally synchronize and initiate the start of the sequential channel conversion process. In both direct and auto modes, when the CONV-RATE-[1:0] bits are set to a value other than the maximum rate ('00'), nap mode is activated between conversions. By activating nap mode, the $AI_{DD}$ supply current is reduced; see Figure 67.

**Table 1. ADC Conversion Rate**

| CONV-RATE-1 | CONV-RATE-0 | $t_{ACQ}$ (µs) | $t_{CONV}$ (µs) | NAP ENABLED | THROUGHPUT (Single-Channel Auto Mode) |
|---|---|---|---|---|---|
| 0 | 0 | 0.375 | 1.625 | No | 500 kSPS (default) |
| 0 | 1 | 2.375 | 1.625 | Yes | 250 kSPS |
| 1 | 0 | 6.375 | 1.625 | Yes | 125 kSPS |
| 1 | 1 | 14.375 | 1.625 | Yes | 62.5 kSPS |

### Handshaking with the Host (see AMC configuration register 0)

The DAV pin and the DAVF (data available flag) bit in AMC configuration register 0 provide handshaking with the host. Pin and bit status depend on the conversion mode (direct or auto); see Figure 84 and Figure 85. In direct mode, after ADC-*n*-data registers of all selected channels are updated, the DAVF bit in AMC configuration register 0 is set immediately to '1', and the DAV pin is active (low) to signify that new data are available. By reading the ADC-*n*-data register or restarting via the external $\overline{CNVT}$ pin, the ADC clears the DAVF bit to '0' and deactivates the DAV pin (high). If an internal convert start (ICONV bit) is used to start the new ADC conversion, an ADC-*n*-data register must be read after the current conversion completes before a new conversion can be started in order to reset the DAV status.

In auto-mode, after the ADC-*n*-data registers of the selected channels are updated, a pulse of 1 µs (low) appears on the DAV pin to signify that new data are available. However, the DAVF bit is always cleared to '0' in auto-mode.

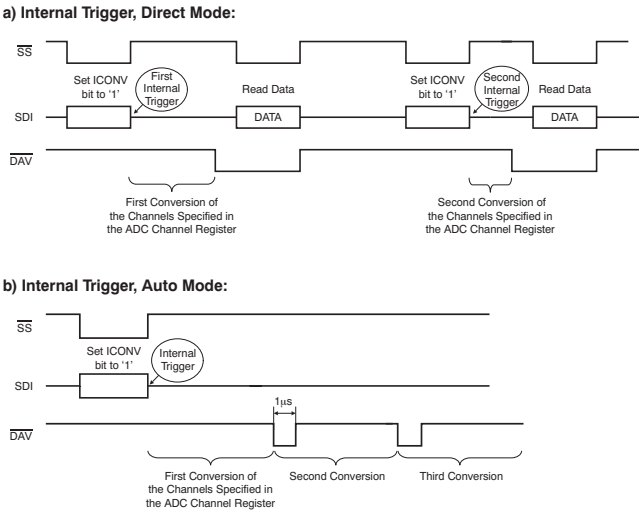



**Figure 84. ADC Internal Trigger**

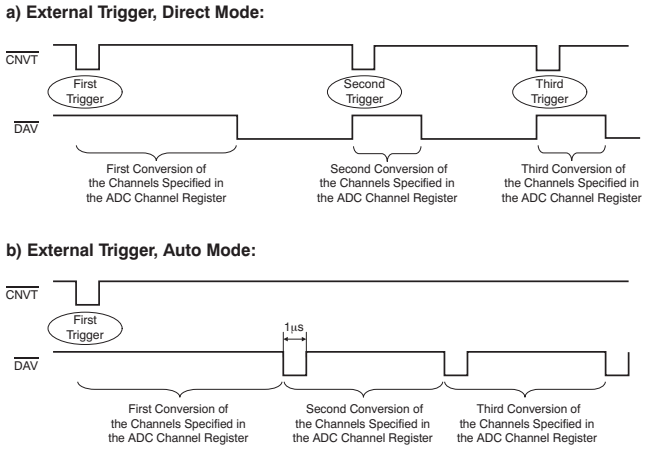



**Figure 85. ADC External Trigger**

### Data Available Pin ($\overline{DAV}$)

$\overline{DAV}$ is an output pin that indicates the completion of ADC conversions. The DAVF bit in AMC configuration register 0 determines the status of the $\overline{DAV}$ pin. In direct mode, after the selected group of input channels are converted and the ADC is stopped, the DAVF bit is set to '1' and the $\overline{DAV}$ pin is driven to logic low (active). In ADC auto mode, each time the group of input channels are sequentially converted, a 1-µs pulse (low) appears on the $\overline{DAV}$ pin.

### Convert Pin ($\overline{CNVT}$)

$\overline{CNVT}$ is the input pin for the external ADC trigger signal. ADC channel conversions begin on the falling edge of the $\overline{CNVT}$ pulse. If a $\overline{CNVT}$ pulse occurs when the ADC is already converting, then the ADC continues converting the current channel. After the current channel completes, the existing conversion cycle finishes and a new conversion cycle starts. The selected channels specified in the ADC channel registers are converted sequentially in order of enabled channels.

### Analog Input Out-of-Range Detection (see the *Analog Input Out-of-Range Alarm* Section)

The CH0 to CH3 analog inputs and the temperature inputs are implemented with out-of-range detection. When any of these inputs is out of the preset range, the corresponding alarm flag in the status register is set. If any inputs are out of range, the global out-of-range pin ($\overline{ALARM}$) goes low. To avoid a false alarm, the device is implemented with false-alarm protection. See the *Alarm Operation* section for more details.

### Full-Scale Range of the Analog Input

The gain bit of the ADC gain register determines the full-scale range of the analog input. Full-scale range is $V_{REF}$ when ADG*n* = 0, or ($2 \times V_{REF}$) when ADG*n* = 1. If a channel pair is configured for differential operation, the input ranges are either $\pm V_{REF}$ or $\pm(2 \times V_{REF})$. In ($2 \times V_{REF}$) mode, the input is effectively divided by two before the conversion takes place. Each input must not exceed the supply value of $AV_{DD}$ + 0.2 V or AGND – 0.2 V. When the REF-OUT pin is connected to the REF-ADC pin, the internal reference is used as the ADC reference. When an external reference voltage is applied to the REF-ADC pin, the external reference is used as the ADC reference.

## SECONDARY ADC AND TEMPERATURE SENSOR OPERATION

The AMC7812B contains one local and two remote temperature sensors. The temperature sensors continuously monitor the three temperature inputs, and new readings are automatically available every cycle. The on-chip integrated temperature sensor (shown in Figure 86) is used to measure the device temperature. Two remote diode sensor inputs are used to measure the two external temperatures. All analog signals are converted by the secondary ADC that runs in the background at a lower speed. The measurement relies on the characteristics of a semiconductor junction operation at a fixed current level. The forward voltage of the diode ($V_{BE}$) depends on the current passing through the diode and the ambient temperature. The change in $V_{BE}$ when the diode operates at two different currents (a low current of $I_{LOW}$ and a high current of $I_{HIGH}$) is shown in Equation 1:

$$V_{BE\_HIGH} - V_{BE\_LOW} = \frac{\eta kT}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right) \quad (1)$$

where:

- k is Boltzmann's constant,
- q is the charge of the carrier,
- T is the absolute temperature in Kelvin (K), and
- η is the ideality of the transistor as a sensor.

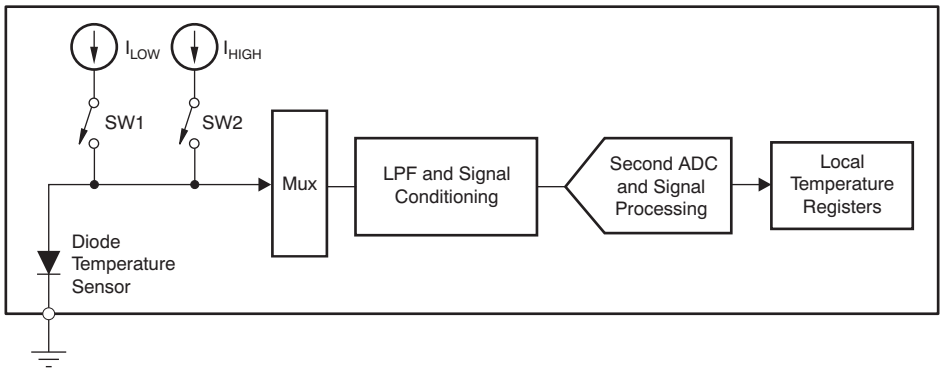



**Figure 86. Integrated Local Temperature Sensor**

The remote sensing transistor can be a discrete, small-signal type transistor or a substrate transistor built within the microprocessor. This architecture is shown in Figure 87. An internal voltage source biases the D– terminal above ground to prevent the ground noise from interfering with measurement. An external capacitor (up to 330 pF) may be placed between D+ and D– to further reduce noise interference.

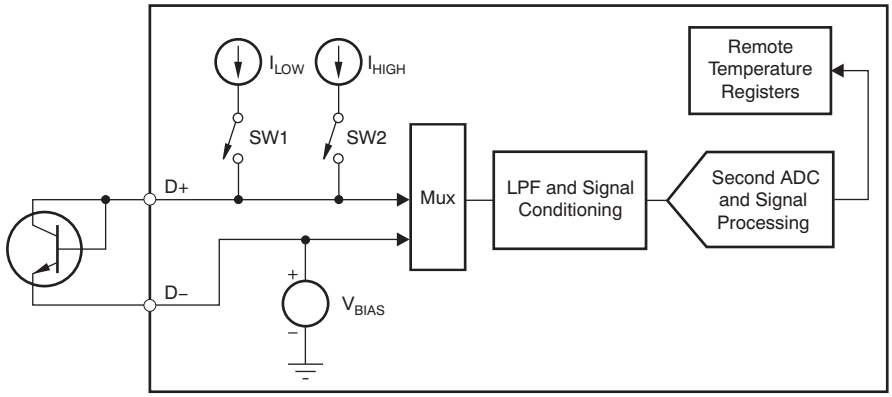



**Figure 87. Remote Temperature Sensor**

The device has three temperature sensors: two remote (D1 and D2) and one on-chip (LT). If any sensor is not used, it can be disabled by clearing the corresponding enable bit (bits D2EN, D1EN, and LTEN of the temperature configuration register). When disabled, the sensors are not converted. The device continuously monitors the selected temperature sensors in the background, leaving the user free to perform conversions on the other channels. When one monitor cycle finishes, a signal passes to the control logic to automatically initiate a new conversion.

The analog sensing signal is preprocessed by a low-pass filter and signal-conditioning circuitry, and then digitized by the ADC. The resulting digital signal is further processed by the digital filter and processing unit. The final result is stored in the LT-temperature-data register, the D1-temperature-data register, and the D2-temperature-data register, respectively. The format of the final result is in twos complement, as shown in Table 2. Note that the device measures the temperature from –40°C to +150°C.

**Table 2. Temperature Data Format**

| TEMPERATURE (°C) | DIGITAL CODE |
|---|---|
| +255.875 | 011111111111 |
| +150 | 010010110000 |
| +100 | 001100100000 |
| +50 | 000110010000 |
| +25 | 000011001000 |
| +1 | 000000001000 |
| 0 | 000000000000 |
| –1 | 111111111000 |
| –25 | 111100111000 |
| –50 | 111001110000 |
| –100 | 110011100000 |
| –150 | 101101010000 |
| –256 | 100000000000 |

### Remote Sensing Diode

Errors in remote temperature sensor readings are typically the consequence of the ideality factor and current excitation used by the device versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a low-level ($I_{LOW}$) and high-level ($I_{HIGH}$) current for the temperature-sensing substrate transistors. The AMC7812B uses 6 µA for $I_{LOW}$ and 120 µA for $I_{HIGH}$. The device is designed to function with discrete transistors, such as the 2N3904 and 2N3906. If an alternative transistor is used, the device operates as specified, as long as the following conditions are met:

1. Base-emitter voltage is greater than 0.25 V at 6 µA, at the highest sensed temperature.
2. Base-emitter voltage is less than 0.95 V at 120 µA, at the lowest sensed temperature.
3. Base resistance is less than 100 Ω.
4. Tight control of $V_{BE}$ characteristics indicated by small variations in $h_{FE}$ (that is, 50 to 150).

#### *Ideality Factor*

The ideality factor (η) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The device allows for different η-factor values, according to Table 3. The device is trimmed for a power-on reset (POR) value of η = 1.008. If η is different, the η-factor correction register can be used. The value ($N_{ADJUST}$) written in this register must be in twos complement format, as shown in Table 3. This value is used to adjust the effective η-factor according to Equation 2 and Equation 3.

**Table 3. η-Factor Range (Single Byte)**

| $N_{ADJUST}$ | | | $\eta_{EFF}$ |
|---|---|---|---|
| BINARY | HEX | DECIMAL | |
| 0111 1111 | 7F | 127 | 1.747977 |
| 0000 1010 | 0A | 10 | 1.042759 |
| 0000 1000 | 08 | 8 | 1.035616 |
| 0000 0110 | 06 | 6 | 1.028571 |
| 0000 0100 | 04 | 4 | 1.021622 |
| 0000 0010 | 02 | 2 | 1.014765 |
| 0000 0001 | 01 | 1 | 1.011371 |
| 0000 0000 | 00 | 0 | 1.008 |
| 1111 1111 | FF | –1 | 1.004651 |
| 1111 1110 | FE | –2 | 1.001325 |
| 1111 1100 | FC | –4 | 0.994737 |
| 1111 1010 | FA | –6 | 0.988235 |
| 1111 1000 | F8 | –8 | 0.981818 |
| 1111 0110 | F6 | –10 | 0.975484 |
| 1000 0000 | 80 | –128 | 0.706542 |

$$\eta_{eff} = \frac{1.008 \times 300}{300 - N_{ADJUST}} \quad (2)$$

$$N_{ADJUST} = 300 - \left( \frac{300 \times 1.008}{\eta_{eff}} \right) \quad (3)$$

where:

- $\eta_{EFF}$ is the actual ideality of the transistor used and
- $N_{ADJUST}$ is the corrected ideality used in the calculation.

### Filtering

Figure 88(a) and Figure 88(b) show the connection of recommended NPN or PNP transistors, respectively. Remote junction temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals, and can corrupt measurements. The AMC7812B has a built-in 65-kHz filter on the D+ and D– inputs to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor can make the application more robust against unwanted coupled signals. If filtering is required, the capacitance between D+ and D– should be limited to 330 pF or less for optimum measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and the device.


(a) NPN (b) PNP

**Figure 88. Remote Temperature Sensor Using Transistor**

### Series Resistance Cancellation

Parasitic resistance (in series with the remote diode) to the D+ and D– inputs of the device is caused by a variety of factors, including printed circuit board (PCB) trace resistance and trace length. This series resistance appears as a temperature offset in the remote sensor temperature measurement, and causes more than 0.45°C error per ohm. The device implements a technology to automatically cancel out the effect of this series resistance, thus providing a more accurate result without requiring user characterization of this resistance. With this technology, the device is able to reduce the effects of series resistance to typically less than 0.0075°C per ohm. The resistance cancellation is disabled when the RC bit in the temperature configuration register is cleared ('0').

### Reading Temperature Data

Temperature is always read as 12-bit data. When the conversion finishes, the temperature is sent to the corresponding temperature-data register. However, if a data transfer is in progress between the temperature-data register and the AMC shift register, the temperature-data register is frozen until data transfer completes.

### Conversion Time

The conversion time depends on the type of sensor and configuration, as shown in Table 4.

**Table 4. Conversion Times**

| TEMPERATURE SENSOR | MONITORING CYCLE TIME (ms) | PROGRAMMABLE DELAY RANGE (s) |
|---|---|---|
| Local sensor is active, remote sensors are disabled or in power-down | 15 | 0.48 to 3.84 |
| One remote sensor is active and RC = 0, local sensor and one remote sensor are disabled or in power-down | 44 | 1.40 to 11.2 |
| One remote sensor is active and RC = 1, local sensor and one remote sensor are disabled or in power-down | 93 | 2.97 to 23.8 |
| One remote sensor and local sensor are active and RC = 0, one remote sensor is disabled or in power-down | 59 | 1.89 to 15.1 |
| One remote sensor and local sensor are active and RC = 1, one remote sensor is disabled or in power-down | 108 | 3.45 to 27.65 |
| Two remote sensors are active and RC = 0, local sensor is disabled or in power-down | 88 | 2.81 to 22.5 |
| Two remote sensors are active and RC = 1, local sensor is disabled or in power-down | 186 | 5.95 to 47.6 |
| All sensors are active and RC is '0' | 103 | 3.92 to 26.38 |
| All sensors are active and RC is '1' | 201 | 6.43 to 51.45 |

## REFERENCE OPERATION

This section describes the operation of the internal and external references.

### Internal Reference

The device includes a 2.5-V internal reference. The internal reference is externally available at the REF-OUT pin. A 100-pF to 10-nF capacitor is recommended between the reference output and GND for noise filtering. The internal reference is a bipolar transistor-based, precision band-gap voltage reference. The output current is limited by design to approximately 100 mA.

The internal reference drives all temperature sensors. When connecting the REF-OUT pin to the REF-DAC pin, the internal reference functions as the DAC reference.

The ADC-REF-IN/CMP pin has a dual function. When an external reference is connected to this pin, the external reference is used as the ADC reference. When a compensation capacitor (4.7 µF, typical) is connected between this pin and AGND, the internal reference is used as the ADC reference. When using an external reference to drive the ADC, the ADC-REF-INT bit in AMC configuration register 0 must be cleared ('0') to turn off the ADC reference buffer. When using the internal reference to drive the ADC, the ADC-REF-INT bit in AMC configuration register 0 must be set to '1' to turn on the ADC reference buffer.

### External Reference

Figure 89 shows how the external reference is used as the DAC reference when applied on the DAC-REF pin, and as the ADC reference when applied on the ADC-REF pin. Figure 90 shows the use of the internal reference.

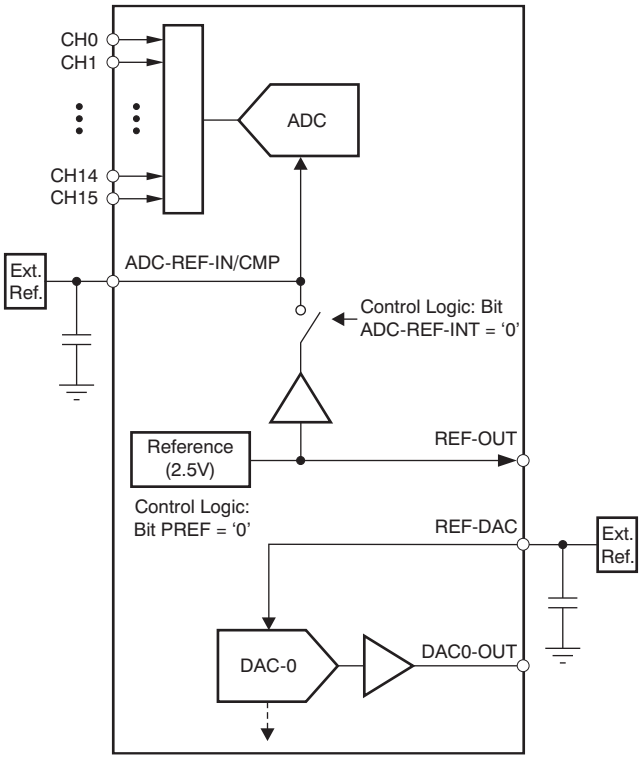



**Figure 89. Use of the External Reference**

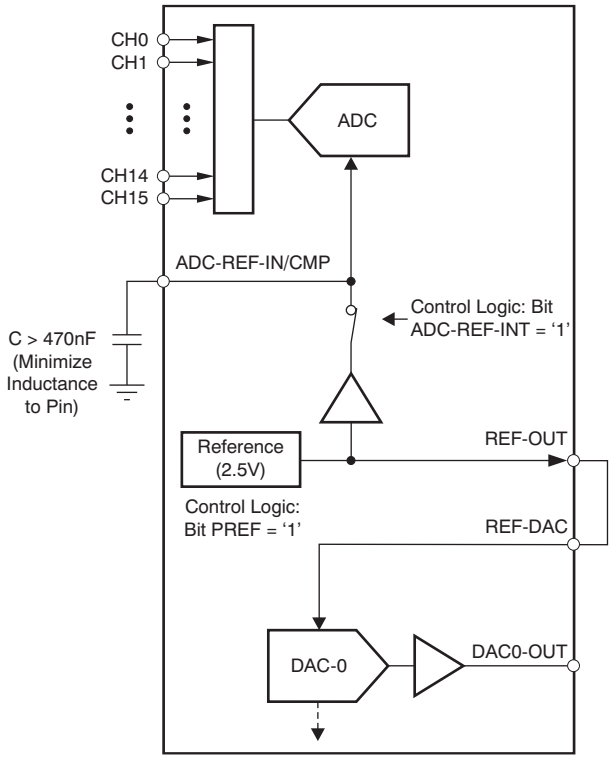
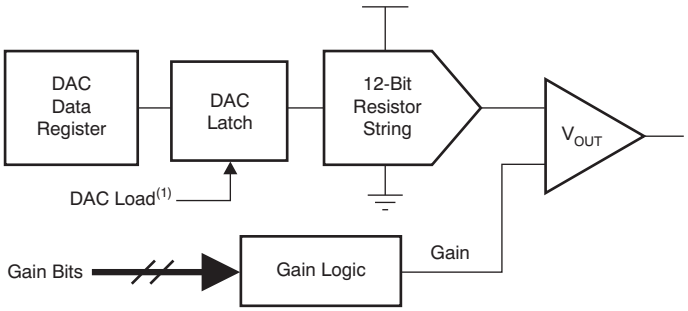



**Figure 90. Use of the Internal Reference**

## DAC OPERATION

The device contains 12 DACs that provide digital control with 12 bits of resolution using an internal or external reference. The DAC core is a 12-bit string DAC and output buffer. The DAC drives the output buffer to provide an output voltage. Refer to the DAC configuration register for details. Figure 91 shows a function block diagram of the DAC architecture. The DAC latch stores the code that determines the output voltage from the DAC string. The code is transferred from the DAC-*n*-data register to the DAC latch when the internal DAC-load signal is generated.




(1) Internal DAC load is generated by writing '1' to the ILDAC bit in synchronous mode. In asynchronous mode, the DAC latch is transparent.

**Figure 91. DAC Block Diagram**

### Resistor String

The resistor string structure is shown in Figure 92. The resistor string consists of a string of resistors, each of value *R*. The code loaded to the DAC latch determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture is inherently monotonic, voltage out, and low glitch. The resistor string architecture is also linear because all the resistors are of equal value.

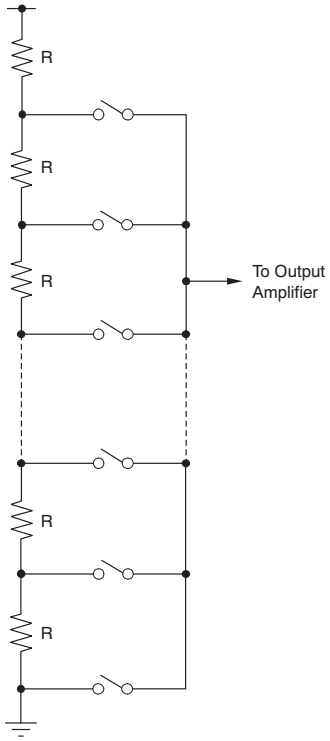



**Figure 92. Resistor String**

### DAC Output

The output range is programmable from 0 V to ($2 \times V_{REF}$) or from 0 V to ($5 \times V_{REF}$), depending on the gain bits in the DAC gain register. The maximum output is $AV_{CC}$. The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to $AV_{CC}$. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 1.5 V/µs with a typical 1/4 to 3/4 scale settling time of 3 µs with the output unloaded.

### Double-Buffered DAC Data Registers

There are 12 double-buffered DAC data registers. Each DAC has an internal latch preceded by a DAC data register. Data are initially written to an individual DAC-*n*-data register and then transferred to the corresponding DAC-*n* latch. When the DAC-*n* latch is updated, the output of DAC-*n* changes to the newly set value. When the host reads the register memory map location labeled DAC-*n*-data, the value held in the DAC-*n* latch is returned (not the value held in the input DAC-*n*-data register).

### Full-Scale Output Range

The full-scale output range of each DAC is set by the product of the value of the reference voltage times the gain of the DAC output buffer ($V_{REF} \times$ gain). The gain bits of the DAC gain register set the output range of the individual DAC-*n*. The full-scale output range of each DAC is limited by the analog power supply. The maximum output from the DAC must not be greater than $AV_{CC}$, and the minimum output must not be less than AGND.

### DAC Output After Power-On Reset

After power-on, the DAC output buffer is in power-down mode. The output buffer is in a Hi-Z state and the DACx-OUT (where x = 0 to 11) output pin connects to the analog ground through an internal 10-kΩ resistor. After power-on or a hardware reset, all DAC-*n*-data registers, DAC-*n* latches, and the DAC output are set to default values (000h).

### Load DAC Latch

See Figure 91 for the structure of the DAC register and DAC latch. The contents of the DAC-*n* latch determine the output level of the DAC-*n* pin. After writing to the DAC-*n*-data register, the DAC latch can be loaded either in asynchronous or synchronous mode.

In asynchronous mode (SLDAC-*n* bit = '0'), data are loaded into the DAC-*n* latch immediately after the write operation. In synchronous mode (SLDAC-*n* bit = '1'), the DAC latch updates when the synchronous DAC loading signal occurs. Setting the ILDAC bit in AMC configuration register 0 generates the loading signal.

### Synchronous Load, Asynchronous Load, and Output Updating

The SLDA-*n* (synchronous load) bit of the DAC configuration register determines the DAC updating mode, as shown in Table 5. When SLDA-*n* is cleared to '0', asynchronous mode is active, the DAC latch updates immediately after writing to the DAC-*n*-data register, and the output of DAC-*n* changes accordingly.

**Table 5. DAC-*n* Output Update Summary for Manual Mode Update**

| SLDA-*n* BIT | WRITING TO ILDAC BIT | OPERATION |
|---|---|---|
| 0 | Don't care | Update DAC-*n* individually. The DAC-*n* latch and DAC-*n* output are immediately updated after writing to the DAC-*n*-data register. |
| 1 | 1 | Simultaneously update all DACs by internal trigger. Writing '1' to the ILDAC bit generates an internal load DAC trigger signal that updates the DAC-*n* latches and DAC-*n* outputs with the contents of the corresponding DAC-*n*-data register. |

When the SLDA-*n* bit is set to '1', synchronous mode is selected. The value of the DAC-*n*-data register is transferred to the DAC-*n* latch only after an active DAC synchronous loading signal (ILDAC) occurs, which immediately updates the DAC-*n* output. Under synchronous loading operation, writing data into a DAC-*n*-data register changes only the value in that register, but not the content of DAC-*n* latch nor the output of DAC-*n*, until the synchronous load signal occurs.

The DAC synchronous load is triggered by writing '1' to the ILDAC bit in AMC configuration register 0. When this DAC synchronous load signal occurs, all DACs with the SLDA-*n* bit set to '1' are simultaneously updated with the value of the corresponding DAC-*n*-data register. By setting the SLDA-n bit properly, several DACs can be updated at the same time. For example, to update DAC0 and DAC1 synchronously, set bits SLDA-0 and SLDA-1 to '1' first, and then write the proper values into the DAC-0-data and DAC-1-data registers, respectively. After this presetting, set the ILDAC bit to '1' to simultaneously load DAC0 and DAC1. The outputs of DAC0 and DAC1 change at the same time.

The device updates the DAC latch only if the latch was accessed from the last time ILDAC was issued, thereby eliminating any unnecessary glitches. Any DAC channels that are not accessed are not reloaded again. When the DAC latch is updated, the corresponding output changes to the new level immediately.

**NOTE**

When DACs are *cleared* by an external DAC-CLR-n or by the internal CLR bit, the DAC latch is loaded with the predefined value of the DAC-*n*-CLR-setting register and the output is set to the corresponding level immediately, regardless of the SLDA-*n* bit value. However, the DAC data register does not change.

### Clear DACs

DAC-*n* can be cleared with hardware or software, as shown in Figure 93. When DAC-*n* goes to a *clear* state, it is immediately loaded with predefined code in the DAC-*n*-CLR-setting register, and the output is set to the corresponding level to shut down the external LDMOS device. However, the DAC-*n*-data register does not change. When the DAC goes back to normal operation, DAC-*n* is immediately loaded with the previous data from the DAC-*n*-data register and the output of DAC*n*-OUT is set back to the previous level to restore LDMOS to the status before shutdown, regardless of the SLDAC-*n* bit status.

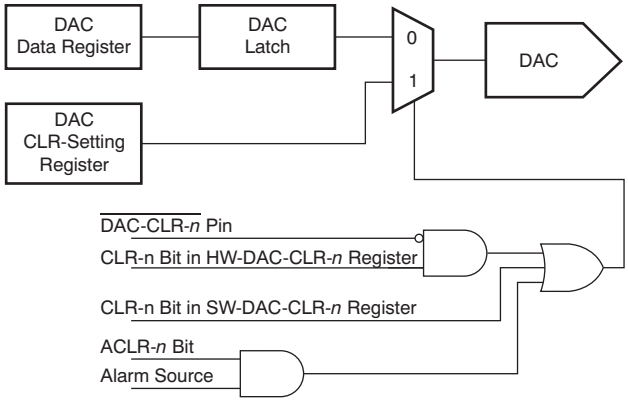



**Figure 93. Clearing DAC-*n***

The device is implemented with two external control lines, the $\overline{\text{DAC-CLR-0}}$ and $\overline{\text{DAC-CLR-1}}$ pins, to clear the DACs. When either pin goes low, the corresponding user-selected DACs are in a *cleared* state. The HW_DAC-CLR-0 register determines which DAC is cleared when the $\overline{\text{DAC-CLR-0}}$ pin is low. The register contains 12 clear bits (CLR-*n*), one per DAC. If the CLR-*n* bit is '1', DAC-*n* is in a cleared state when the $\overline{\text{DAC-CLR-0}}$ pin is low. However, if the CLR-*n* bit is '0', DAC-*n* does not change when the pin is low. Likewise, the HW-DAC-CLR-1 register determines which DAC is cleared when the $\overline{\text{DAC-CLR-1}}$ pin is low.

Writing directly to the SW_DAC_CLR register puts the selected DACs in a cleared state. DACs can also be forced into a clear state by alarm events. The AUTO-DAC-CLR-SOURCE register specifies which alarm events force the DACs into a clear state, and the AUTO-DAC-CLR-EN register defines which DACs are forced into a clear state. Refer to the AUTO-DAC-CLR-SOURCE register and AUTO-DAC-CLR-EN register for further details.

### DAC Output Thermal Protection

A significant amount of power can be dissipated in the DAC outputs. The AMC7812B is implemented with a thermal protection circuit that sets the THERM-ALR bit in the status register if the die temperature exceeds +150°C. The THERM-ALR bit can be used in combination with THERM-ALR-CLR (bit 2 in the AUTO-DAC-CLR-SOURCE register) and ACLR-*n* (bits[14:3] in the AUTO-DAC-CLR-EN register) to set the DAC output to a predefined code when this condition occurs. Note that this feature is disabled when the local temperature sensor powers down.

### Alarm Operation

The device continuously monitors all analog inputs and temperatures in normal operation. When any input is out of the specified range, an alarm triggers. When an alarm state occurs, the corresponding individual alarm bit in the status register is set ('1'). The global alarm bit (GALR) in AMC configuration register 0 is the OR of individual alarms, see Figure 94. When the ALARM-LATCH-DIS bit in the alarm control register is cleared ('0'), the alarm is latched. The global alarm bit (GALR) maintains '1' until the corresponding error conditions subside and the alarm status is read. The alarm bits are referred to as being *latched* because they remain set until read by software. This design ensures that out-of-limit events cannot be missed if the software is polling the device periodically. All bits are cleared when reading the status register, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle, unless otherwise noted.

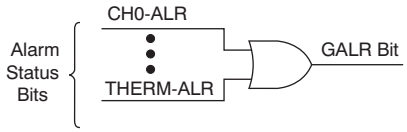



**Figure 94. Global Alarm Bit**

When the ALARM-LATCH-DIS bit in the alarm control register is set ('1'), the alarm bit is not latched. The alarm bit in the status register goes to '0' when the error condition subsides, regardless of whether the bit is read or not. When GALR is '1', the ALARM pin goes low. When the GALR bit is '0', the ALARM is high (inactive).

### Analog Input Out-of-Range Alarm

The device provides out-of-range detection for four individual analog inputs (CH0, CH1, CH2, and CH3), as shown in Figure 95. When the measurement is out-of-range, the corresponding alarm bit in the status register is set to '1' to flag the out-of-range condition. The value in the high-threshold register defines the upper bound threshold of the *N*th analog input, while the value in the low-threshold register defines the lower bound. These two bounds specify a window for the out-of-range detection.

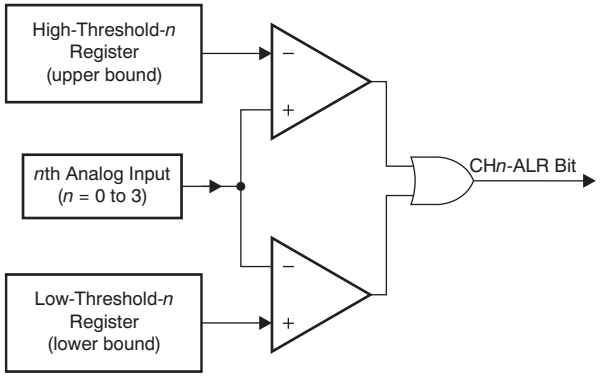



**Figure 95. CH*n* Out-of-Range Alarm**

The device also has high-limit or low-limit detection for the temperature sensors (D1, D2, and LT), as shown in Figure 96. To implement single, upper-bound threshold detection for analog input CH*n*, the host processor can set the upper-bound threshold to the desired value and the lower-bound threshold to the default value. For lower-bound threshold detection, the host processor can set the lower-bound threshold to the desired value and the upper-bound threshold to the default value. Note that the value of the high-threshold register must not be less than the value of the low-threshold register; otherwise, ALR-*n* is always set to '1' and the alarm indicator is always active. Each temperature sensor has two alarm bits: High-ALR (high-limit alarm) and Low-ALR (low-limit alarm).

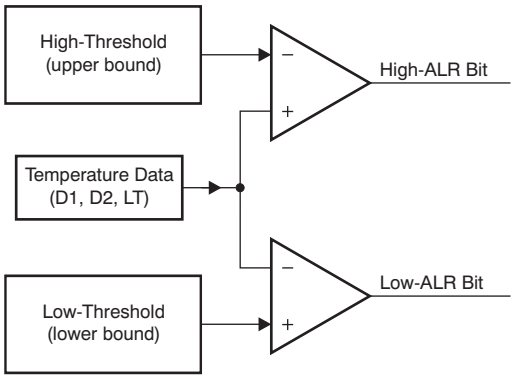



**Figure 96. Temperature Out-of-Range Alarm**

### $\overline{\text{ALARM}}$ pin

The $\overline{\text{ALARM}}$ pin is a global alarm indicator. $\overline{\text{ALARM}}$ is an open-drain pin, as Figure 97 illustrates; an external pull-up resistor is required. When the pin is activated, it goes low. When the pin is inactive, it is in Hi-Z status. The $\overline{\text{ALARM}}$ pin functions as an interrupt to the host so that it may query the status register to determine the alarm source. Any alarm event (including analog inputs, temperatures, diode status, and device thermal condition) activates the pin if the alarm is not masked (the corresponding EALR bit in the alarm control register is '1'). When the alarm pin is masked (EN-ALARM bit is '0'), the occurrence of the event sets the corresponding status bit in status register to '1', but does not activate the $\overline{\text{ALARM}}$ pin.

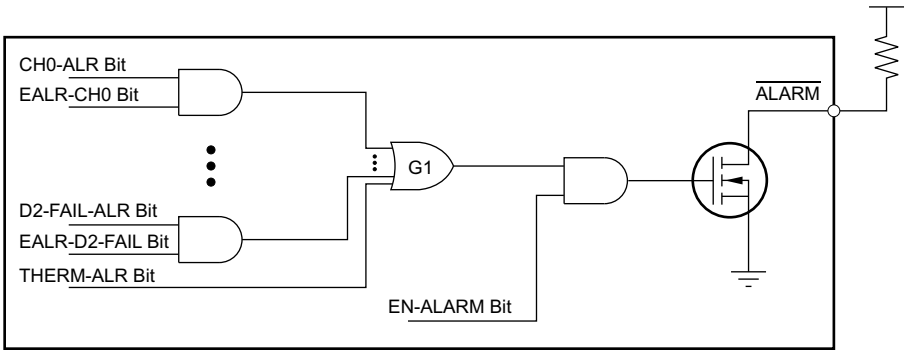



**Figure 97. $\overline{\text{ALARM}}$ Pin**

When the ALARM-LATCH-DIS bit in the alarm control register is cleared ('0'), the alarm is latched. Reading the status register clears the alarm status bit. Whenever an alarm status bit is set, indicating an alarm condition, the bit remains set until the event that caused the alarm is resolved and the status register is read. The alarm bit can only be cleared by reading the status register after the event is resolved, or by a hardware reset, software reset, or power-on reset (POR). All bits are cleared when reading the status register, and all bits are reasserted if the out-of-limit condition still exists after the next conversion cycle, unless otherwise noted. When the ALARM-LATCH-DIS bit in the alarm control register is set ('1'), the $\overline{\text{ALARM}}$ pin is not latched. The alarm bit clears to '0' when the error condition subsides, regardless of whether the bit is read or not.

### *Hysteresis*

The device continuously monitors the analog input channels and temperatures. If any alarms are out of range and the alarm is enabled, the alarm bit is set ('1'). However, the alarm condition is cleared only when the conversion result returns to a value of at least *hys* below the value of the high threshold register, or *hys* above the value of low threshold register. The hysteresis registers store the value for each analog input (CH0, CH1, CH2, and CH3) and temperature (D1, D2, and LT). *hys* is the value of hysteresis that is programmable: 0 LSB to 127 LSB for analog inputs, and 0°C to +31°C for temperatures. For the THERM-ALR bit, the hysteresis is fixed at 8°C. The hysteresis behavior is shown in Figure 98.

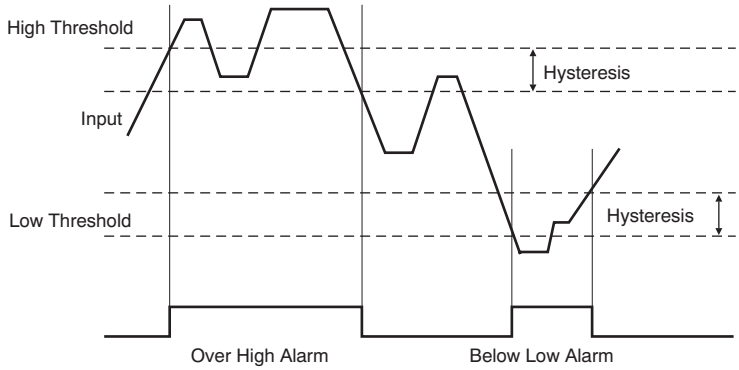



**Figure 98. Hysteresis**

### False-Alarm Protection

As noted previously, the device continuously monitors all analog inputs and temperatures in normal operation. When any input is out of the specified range in *N* consecutive conversions, the corresponding alarm bit is set ('1'). If the input returns to the normal range before *N* consecutive times, the alarm bit remains clear ('0'). This design avoids false alarms.

The number *N* is programmable by the CH-FALR-CT-[2:0] bits in AMC configuration register 1 for analog input CHn as shown in Table 6, or by the TEMP-FALR-CT-[1:0] bits for temperature monitors as shown in Table 7.

**Table 6. Consecutive Sample Number for False Alarm Protection for CH*n***

| CH-FALR-CT-2 | CH-FALR-CT-1 | CH-FALR-CT-0 | *N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 4 |
| 0 | 1 | 0 | 8 |
| 0 | 1 | 1 | 16 (default) |
| 1 | 0 | 0 | 32 |
| 1 | 0 | 1 | 64 |
| 1 | 1 | 0 | 128 |
| 1 | 1 | 1 | 256 |

**Table 7. Consecutive Sample Number for False Alarm Protection for Temperature Channels**

| TEMP-FALR-CT-1 | TEMP-FALR-CT-0 | *N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 (default) |
| 1 | 1 | 8 |

## GENERAL-PURPOSE INPUT AND OUTPUT PINS (GPIO-0 to GPIO-7)

The device has eight GPIO pins. The GPIO-0, -1, -2 and -3 pins are dedicated to general, bidirectional, digital I/O signals. GPIO-4, GPIO-5, GPIO-6, and GPIO-7 are dual-function pins and can be programmed as either bidirectional digital I/O pins or remote temperature sensors D1 and D2. When D1 or D2 is disabled, the pins function as GPIOs. These pins can receive an input or produce an output. When the GPIO-*n* pin functions as an output, it has an open-drain and the status is determined by the corresponding GPIO-*n* bit of the GPIO register. The output state is high impedance when the GPIO-*n* bit is set to '1', and is logic low when the GPIO-*n* bit is cleared ('0'). Note that a 10-kΩ pull-up resistor is required when using the GPIO-*n* pin as an output, see Figure 99. The dual-function GPIO-4, -5, -6, and -7 pins should not be tied to a pull-up voltage that exceeds the $AV_{DD}$ supply. The dedicated GPIO-0, -1, -2, and -3 pins are only restricted by the absolute maximum voltage. To use the GPIO-*n* pin as an input, the corresponding GPIO-*n* bits in the GPIO register must be set to '1'. When the GPIO-*n* pin functions as an input, the digital value on the pin is acquired by reading the corresponding GPIO-*n* bit. After a power-on reset or any forced hardware or software reset, all GPIO-*n* bits are set to '1', and the GPIO-*n* pin goes to a high-impedance state.

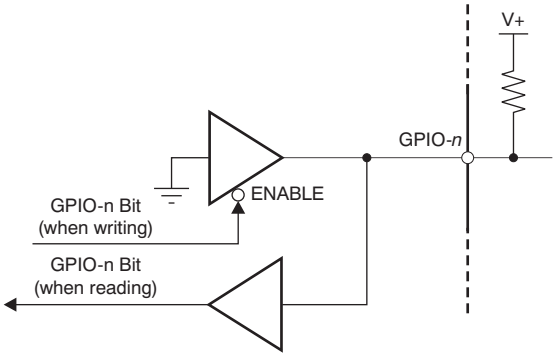



**Figure 99. GPIO Pins**

## HARDWARE RESET

Pulling the $\overline{\text{RESET}}$ pin low performs a hardware reset. When the $\overline{\text{RESET}}$ pin is low, the device enters a reset state and all registers are set to the default values (including the power-down register). Therefore, all function blocks (except the internal temperature sensor) are in power-down mode. On the $\overline{\text{RESET}}$ rising edge, the device returns to the normal operating mode. After returning to this mode, all registers remain set to the default value until a new value is written. Note that after reset, the power-down register must be properly written in order to activate the device. Hardware reset should only be issued when DVDD reaches the minimum specification of 2.7 V or above.

## SOFTWARE RESET

Software reset returns all register settings to their default values and can be performed by writing to the software reset register. In the case of $I^2C$ communication, any value written to this register results in a reset condition. In the case of SPI communications, only writing the specific value of 6600h to this register resets the device. See the *Registers* section for details. During reset, all communication is blocked. After issuing the reset, wait at least 30 µs before attempting to resume communication.

## POWER-ON RESET (POR)

When powered on, the internal POR circuit invokes a power-on reset, which performs the equivalent function of the $\overline{\text{RESET}}$ pin. To ensure a POR, DVDD must start from a level below 750 mV.

## POWER-SUPPLY SEQUENCE

The preferred (not required) order for applying power is IOVDD, DVDD/AVDD, and then AVCC. All registers initialize to the default values after these supplies are established. Communication with the device is valid after a 250-µs maximum power-on reset delay. The default state of all analog blocks is off as determined by the power-down register (6Bh). Before writing to this register, a hardware reset should be issued to ensure specified device operation. Device communication is valid after a maximum 250-µs reset delay from the $\overline{\text{RESET}}$ rising edge. If DVDD falls below 2.7 V, the minimum supply value of DVDD, either issue a hardware or power-on reset in order to resume proper operation.

To avoid activating the device ESD protection diodes, do not apply the GPIO-4, GPIO-5, GPIO-6, and GPIO-7 inputs before the AVDD is established. Also, if using the external reference configuration of the ADC, do not apply ADC-REF-IN/CMP before AVDD.

## PRIMARY COMMUNICATION INTERFACE

The device communicates with the system controller through the primary communication interface, which can be configured as either an $I^2C$-compatible two-wire bus or an SPI bus. When the SPI/I2C pin is tied to ground, the $I^2C$ interface is enabled and the SPI is disabled. When the SPI/I2C pin is tied to IOVDD, the $I^2C$ interface is disabled and the SPI is enabled.

### $I^2C$-Compatible Interface

This device uses a two-wire serial interface compatible with the $I^2C$-bus specification, version 2.1. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All $I^2C$-compatible devices connect to the $I^2C$ bus through open-drain I/O pins SDA and SCL. A master device, usually a microcontroller or a digital signal processor (DSP), controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the start and stop of data transfers. A slave device receives and transmits data on the bus under control of the master device. The AMC7812B functions as a slave and supports the following data transfer modes, as defined in the $I^2C$-bus specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps). The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S mode in this document. The protocol for high-speed mode is different from the F/S mode, and is referred to as Hs mode. The device supports 7-bit addressing. However 10-bit addressing and general-call addressing are not supported. The device slave address is determined by the status of pins A0, A1, and A2, as shown in Table 8.

**Table 8. Slave Addresses**

| A0 | A1 | A2 | SLAVE ADDRESS |
|---|---|---|---|
| GND | GND | GND | 1100001 |
| GND | GND | $IOV_{DD}$ | 0101100 |
| GND | $IOV_{DD}$ | GND | 1100100 |
| GND | $IOV_{DD}$ | $IOV_{DD}$ | 0101110 |
| $IOV_{DD}$ | GND | GND | 1100010 |
| $IOV_{DD}$ | GND | $IOV_{DD}$ | 0101101 |
| $IOV_{DD}$ | $IOV_{DD}$ | GND | 1100101 |
| $IOV_{DD}$ | $IOV_{DD}$ | $IOV_{DD}$ | 0101111 |

### F/S-Mode Protocol

The master initiates the data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high; see Figure 2. All $I^2C$-compatible devices must recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read or write direction bit (R/W) on the SDA line. During all transmissions, the master ensures that data are valid. A valid data condition requires that the SDA line is stable during the entire high period of the clock pulse (see Figure 2). All devices recognize the address sent by the master and compare the address to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 2) by pulling the SDA line low during the entire high period of the ninth SCL cycle. When this acknowledge is detected, the master recognizes that a communication link is established with a slave.

The master generates further SCL cycles to either transmit data to the slave (R/W bit is '1') or receive data from the slave (R/W bit is '0'). In either case, the receiver must acknowledge the data sent by the transmitter. Therefore, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high (see Figure 2). This action releases the bus and stops the communication link with the addressed slave. All $I^2C$-compatible devices must recognize the stop condition. When a stop condition is received, all devices recognize that the bus is released and wait for a start condition followed by a matching address.

### Hs-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing Hs master code 00001xxx. This transmission is made in F/S mode at no more than 400 kbps. No device is allowed to acknowledge the Hs master code, but all devices must recognize the Hs master code and switch their internal setting to support 3.4 Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as for F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends Hs mode and switches all internal settings of the slave devices to support F/S mode. Note that instead of using a stop condition, repeated start conditions are used to secure the bus in Hs mode.

### Address Pointer

The AMC7812B address pointer register is an 8-bit register. Each register has an address and, when accessed, the address pointer points to the register address. All AMC7812B registers are 16 bits, consisting of a high byte (D[15:8]) and a low byte (D[7:0]). The high byte is always accessed first, and the low byte accessed second. When the register is accessed, the entire register is frozen until the operation on the low byte is complete. During a write operation, the new content does not take effect until the low byte is written. In read operation, the whole register value is frozen until the low byte is read.

The address pointer does not change after the current register is accessed. To change the pointer, the master issues a slave address byte with the R/W bit low, followed by the pointer register byte; no additional data are required.

### Timeout Function

The device resets the serial interface if either SCL or SDA are held low for 32.8 ms (typical) between a START and STOP condition. If the device is holding the bus low, the device releases the bus and waits for a START condition. To avoid activating the timeout function, a communication speed of at least 1 kHz for the SCL operating frequency must be maintained.

### *Device Communication Protocol for I²C*

The device uses the following I²C protocols: writing a single word of data to a 16-bit register, writing multiple words to different registers, reading a single word from any register, and reading the same register multiple times. This section discusses these I²C protocols.

#### Writing a Single Word of Data to a 16-Bit Register (Figure 100)

Figure 100 shows a diagram of this protocol. Steps for this protocol are:

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812B slave address followed by a '0' for the direction bit, indicating a write operation.
3. The AMC7812B asserts an acknowledge signal on SDA.
4. The master sends a register address.
5. The AMC7812B asserts an acknowledge signal on SDA.
6. The master sends a data byte of the high byte of the register (D[15:8]).
7. The AMC7812B asserts an acknowledge signal on SDA.
8. The master sends a data byte of the low byte of the register (D[7:0]).
9. The AMC7812B asserts an acknowledge signal on SDA.
10. The master asserts a stop condition to end the transaction.

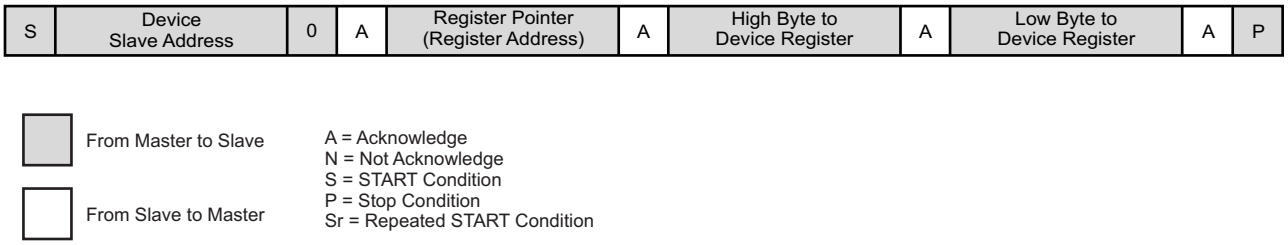



**Figure 100. Write Single Byte**

**Writing Multiple Words to Different Registers (Figure 101)**

A complete word must be written to a register (high byte and low byte) for proper operation, as shown in Figure 101. Steps for this process are:

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812B slave address followed by a '0' for the direction bit, indicating a write operation.
3. The AMC7812B asserts an acknowledge signal on SDA.
4. The master sends the first register address.
5. The AMC7812B asserts an acknowledge signal on SDA.
6. The master sends the high byte of the data word to the first register.
7. The AMC7812B asserts an acknowledge signal on SDA.
8. The master sends the low byte of the data word to the first register.
9. The AMC7812B asserts an acknowledge signal on SDA.
10. The master sends a second register address.
11. The AMC7812B asserts an acknowledge signal on SDA.
12. The master then sends the high byte of the data word to the second register.
13. The AMC7812B asserts an acknowledge on SDA.
14. The master sends the low byte of the data word to the second register.
15. The AMC7812B asserts an acknowledge signal on SDA.
16. The master and the AMC7812B repeat steps 4 to 15 until the last data are transferred.
17. The master then asserts a stop condition to end the transaction.

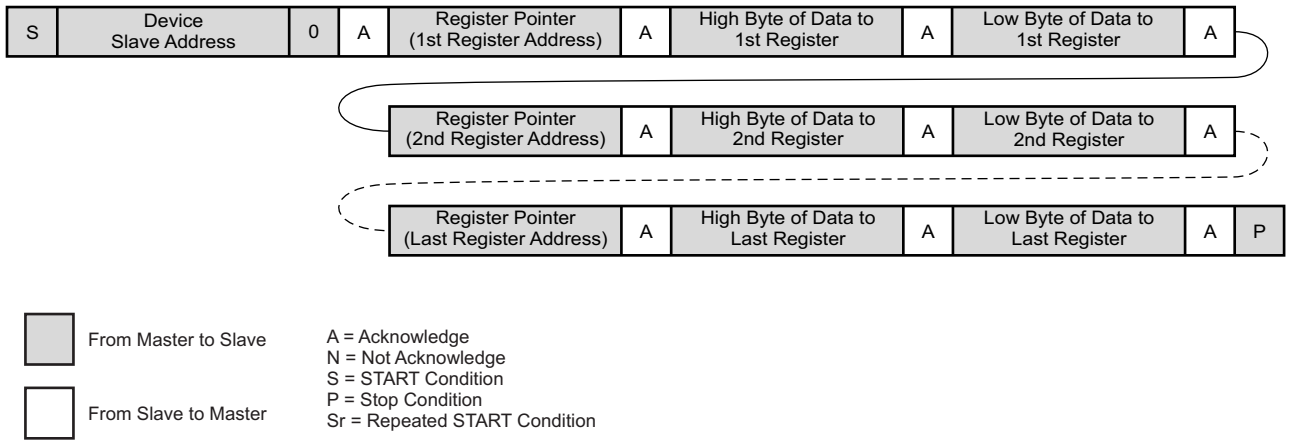



**Figure 101. Write to Multiple 16-Bit Registers**

**Reading a Single Word from Any Register (Figure 102)**

Figure 102 shows a diagram of this protocol. Steps for this protocol are:

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812B slave address followed by a '0' for the direction bit, indicating a write operation.
3. The AMC7812B asserts an acknowledge signal on SDA.
4. The master sends a register address.
5. The AMC7812B asserts an acknowledge signal on SDA.
6. The master device asserts a restart condition.
7. The master then sends the 7-bit AMC7812B slave address followed by a '1' for the direction bit, indicating a read operation.
8. The AMC7812B asserts an acknowledge signal on SDA.
9. The AMC7812B then sends the high byte of the register (D[15:8]).
10. The master asserts an acknowledge signal on SDA.
11. The AMC7812B sends the low byte of the register (D[7:0]).
12. The master asserts a not acknowledge signal on SDA.
13. The master then asserts a stop condition to end the transaction.

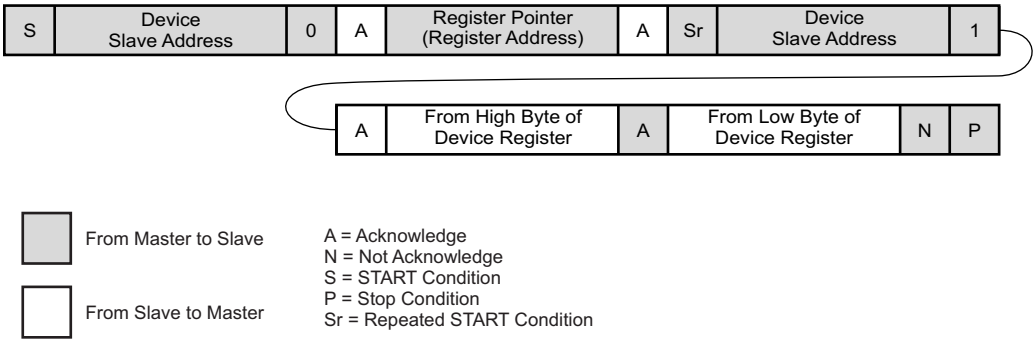



**Figure 102. Read a Single Word**

**Reading the Same Register Multiple Times (Figure 103 and Figure 104)**

Figure 103 and Figure 104 illustrate the process for this protocol. Steps for this protocol are:

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812B slave address followed by a '0' for the direction bit, indicating a write operation.
3. The AMC7812B asserts an acknowledge signal on SDA.
4. The master sends a register address.
5. The AMC7812B asserts an acknowledge signal on SDA.
6. The master device asserts a restart condition.
7. The master then sends the 7-bit AMC7812B slave address followed by a '1' for the direction bit, indicating a read operation.
8. The AMC7812B asserts an acknowledge signal on SDA.
9. The AMC7812B then sends the high byte of the register (D[15:8]).
10. The master asserts an acknowledge signal on SDA.
11. The AMC7812B sends the low byte of the register (D[7:0]).
12. The master asserts an acknowledge signal on SDA.
13. The AMC7812B and the master repeat steps 9 to 12 until the low byte of last reading is transferred.
14. After receiving the low byte of the last register, the master asserts a not acknowledge signal on SDA.
15. The master then asserts a stop condition to end the transaction.

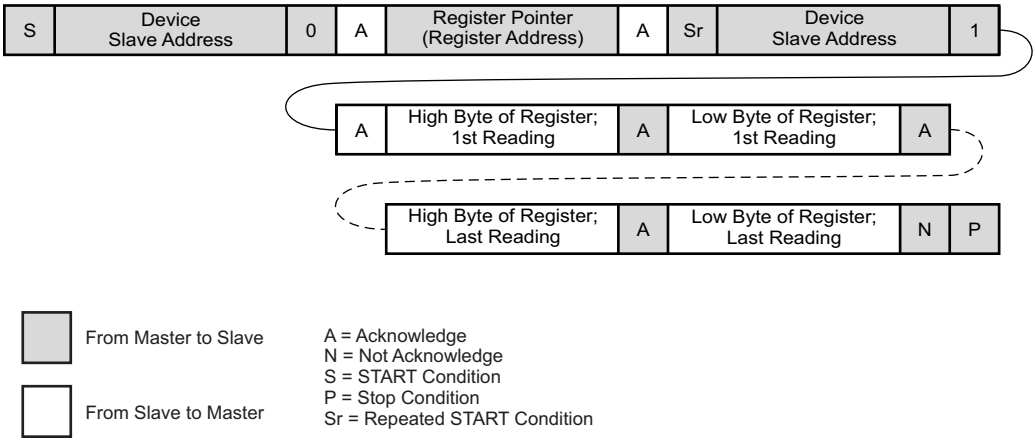



**Figure 103. Read Multiple Words**

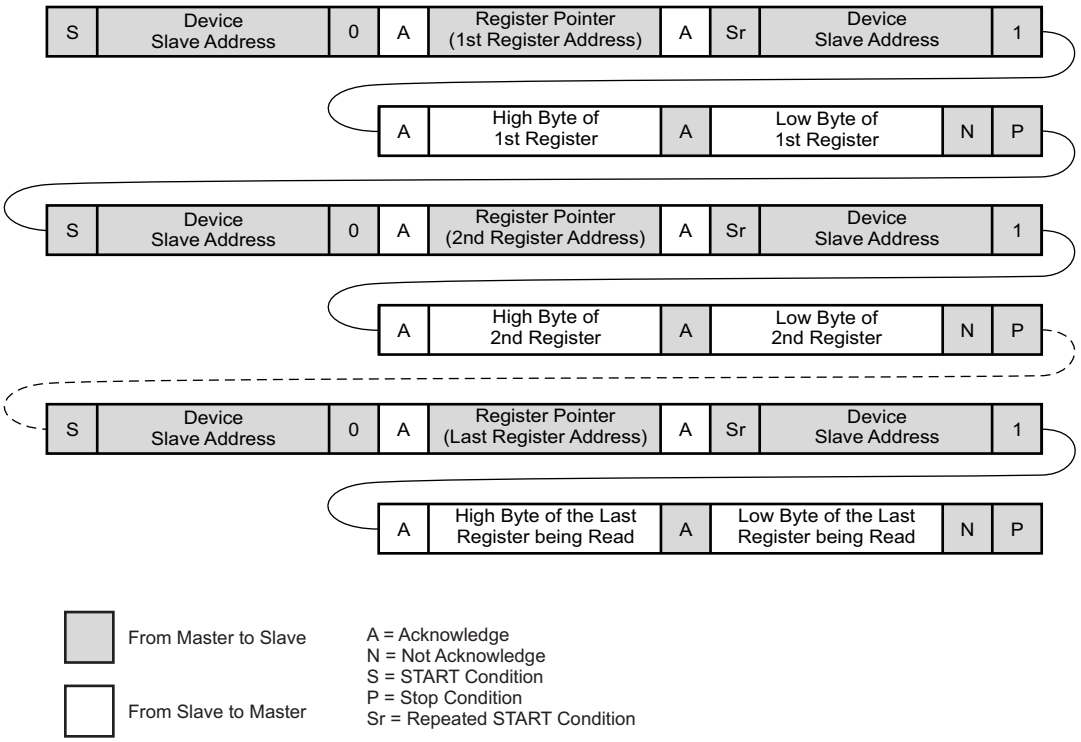



**Figure 104. Read Multiple Registers Using the *Reading Single Word from Any Register* Method**

### Serial Peripheral Interface (SPI)

The AMC7812B can be controlled over a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards. The SPI communication command consists of a read or write (R/W) bit, seven register address bits, and 16 data bits (as shown in Table 9), for a total of 24 bits. The timing for this operation is shown in the SPI timing diagrams (Figure 3, Figure 4, and Figure 5).

#### *SPI Shift Register*

The SPI shift register is 24 bits wide. Data are loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. The $\overline{CS}$ falling edge starts the communication cycle. Data are latched into the SPI shift register on the SCLK falling edge, while $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked out and the SDO line is in a high-impedance state. The contents of the SPI shift register are loaded into the device internal register on the $\overline{CS}$ rising edge (with delay). During the transfer, the command is decoded and new data are transferred into the proper registers.

The serial interface functions with both a continuous and non-continuous serial clock. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock to latch the data.

#### *AMC7812B Communications Command for SPI*

The AMC7812B is entirely controlled by registers. Reading from and writing to these registers is accomplished by issuing a 24-bit operation word shown in Table 9.

**Table 9. 24-Bit Word Structure for Read/Write Operation**

| OPERATION | I/O | BIT 23 (MSB) | BIT22:BIT16 | BIT15:BIT0 |
|---|---|---|---|---|
| Write | SDI | 0 (R/W) | Addr[6:0] | Data to be written |
| | SDO | Data are undefined | Data are undefined | Undefined or data depending on the previous frame |
| Read frame 1 | SDI | 1 (R/W) | Addr[6:0] | Don't care |
| | SDO | Data are undefined | Data are undefined | Undefined or data depending on the previous frame |
| Read frame 2 | SDI | 1 (R/W) | Addr[6:0] | Don't care |
| | SDO | Data are undefined | Data are undefined | Data for address specified in frame 1 |

**Bit 23** **R/W**. Indicates a read from or a write to the addressed register.

0 = The write operation is set and data are written to the specified register
1 = A read operation where bits Addr[6:0] select the register to be read. The remaining bits are *don't care*. Data read from the selected register appear on the SDO pin in the next SPI cycle.

**Bits[22:16]** **Addr6:Addr0.** Register address; specifies which register is accessed.

**Bits[15:0]** **DATA.** 16-bit data bits.

In a write operation, these bits are written to bits[15:0] of the register with the address of (Addr[6:0]).
In a read operation, these bits are determined by the previous operation. If the previous operation is a read, these bits are from bits[15:0] of the internal register specified in previous read operation. If the previous operation is a write, these data bits are *don't care* (undefined). Data read from the current read operation appear on SDO in the next operation cycle.

### Standalone Operation

In standalone mode, as shown in Figure 105, each device has its own SPI bus. The serial clock can be continuous or gated. The first $\overline{CS}$ falling edge starts the operation cycle. Exactly 24 falling clock edges must be applied before $\overline{CS}$ is brought high again. If $\overline{CS}$ is brought high before the 24th falling SCLK edge, or if more than 24 SCLK falling edges are applied before $\overline{CS}$ is brought high, then the input data are incorrect. The device input register is updated from the shift register on the $\overline{CS}$ rising edge, and data are automatically transferred to the addressed registers as well. In order for another serial transfer to occur, $\overline{CS}$ must be brought low again. Figure 106 and Figure 107 show write and read operations in standalone mode.

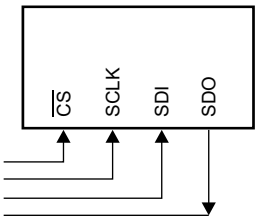
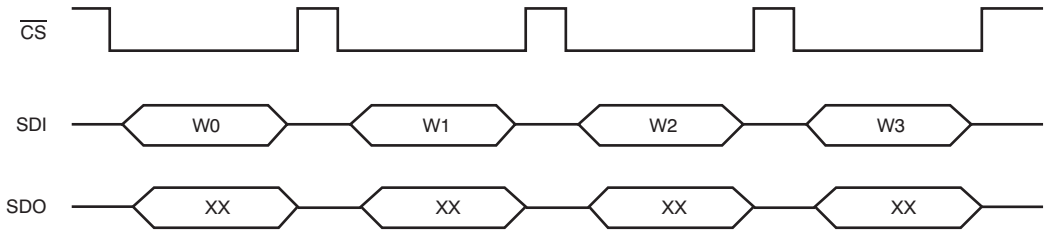
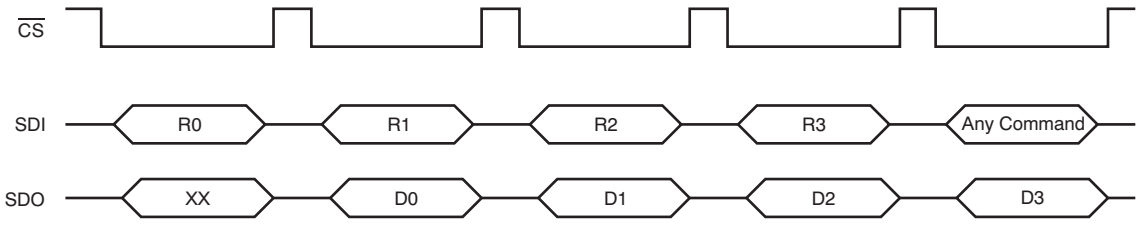



**Figure 105. Standalone Operation**




W*n* = Write Command for Register *N*
XX = Don't care, undefined

**Figure 106. Write Operation in Standalone Mode**




R*n* = Read Command for Register *N*
D*n* = Data from Register *N*
XX = Don't care, undefined

**Figure 107. Read Operation in Standalone Mode**

### Daisy-Chain Operation

For systems that contain several AMC7812Bs, the SDO pin can be used to daisy-chain multiple devices together. This daisy-chain feature is useful in reducing the number of serial interface lines. The first $\overline{CS}$ falling edge starts the operation cycle. SCLK is continuously applied to the input shift register when $\overline{CS}$ is low.

If more than 24 clock pulses are applied, data ripple out of the shift register and appear on the SDO line. These data are clocked out on the SCLK rising edge and are valid on the falling edge. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24*N*, where *N* is the total number of AMC7812Bs in the daisy chain. When the serial transfer to all devices is complete, $\overline{CS}$ is taken high. This action transfers data from the SPI shifter registers to the internal register of each AMC7812B in the daisy-chain and prevents any further data from being clocked in. The serial clock can be continuous or gated. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data. Figure 108 to Figure 111 illustrate the daisy-chain operation.

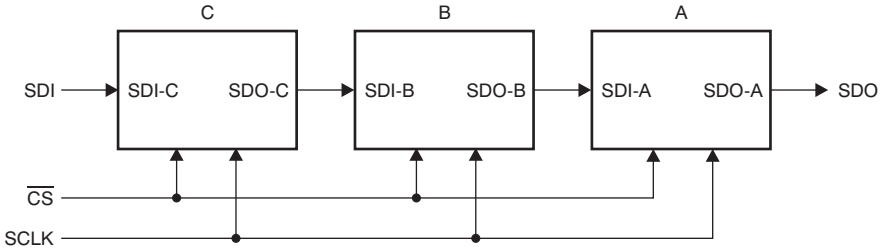
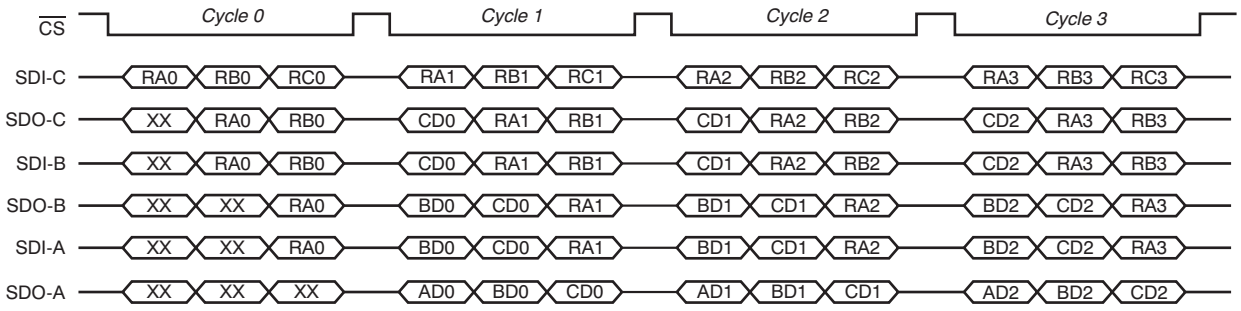
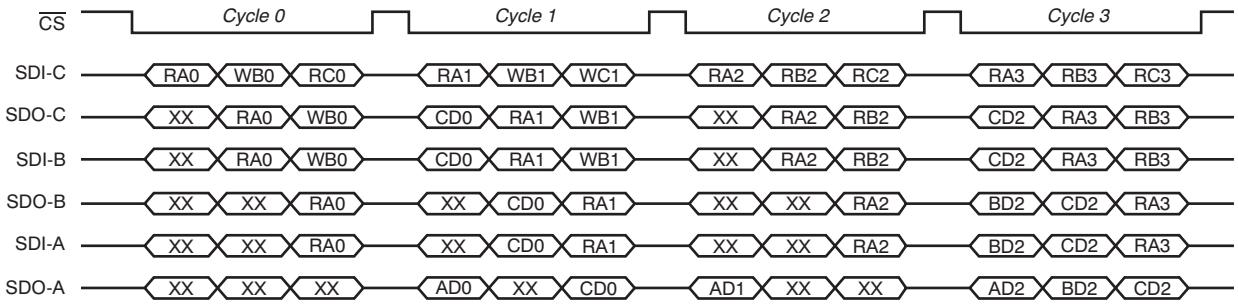



**Figure 108. Three AMC7812Bs in a Daisy-Chain Configuration**




RA*n* (RB*n*, RC*n*) = Read Command for Register *N* of device A (B,C)
AD*n* (BD*n*, CD*n*) = Data from Register *N* of device A (B, C)
XX = Don't care, undefined

**Figure 109. Reading Multiple Registers**




WB*n* (WC*n*) = Write Command for Register *N* of device A (B,C)
RA*n* (RB*n*, RC*n*) = Read Command for Register *N* of device A (B, C)
AD*n* (BD*n*, CD*n*) = Data from Register *N* of device A (B, C)
XX = Don't care, undefined

**Figure 110. Mixed Operation: Reading Devices A and C, and Writing to Device B; then Reading A, and Writing to B and C; then Reading A, B, and C Twice**

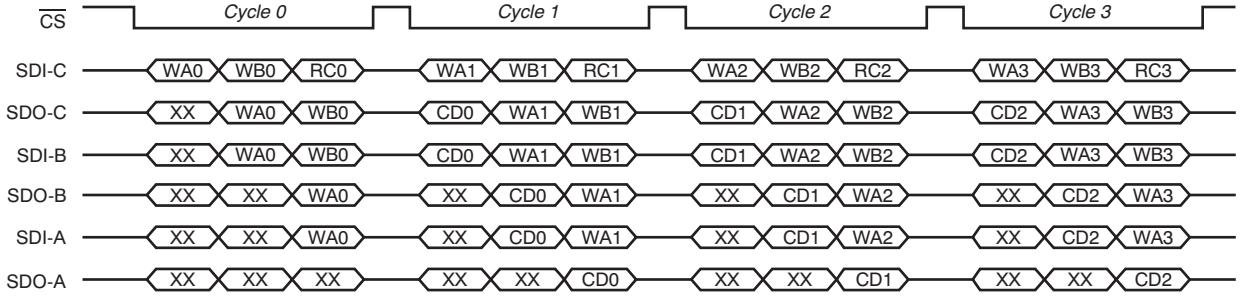



**Figure 111. Writing to Devices A and B, and Reading Device C**

# REGISTERS

## REGISTER MAP

The AMC7812B has several 16-bit registers that consist of a high byte (8 MSBs) and a low byte (8 LSBs). An 8-bit register pointer points to the proper register. The pointer does not change after an operation. Table 10 lists the registers for the AMC7812B. Note that the default values are for SPI operation; see the *Register Descriptions* section for $I^2C$ default values.

**Table 10. Register Map**

| ADDRESS (HEX) | R/W | DEFAULT (HEX) | REGISTER | ADDRESS (HEX) | R/W | DEFAULT (HEX) | REGISTER |
|---|---|---|---|---|---|---|---|
| 00 | R | 0000 | LT-temperature-data | 45 | R/W | 0000 | DAC-6-CLR-setting |
| 01 | R | 0000 | D1-temperature-data | 46 | R/W | 0000 | DAC-7-CLR-setting |
| 02 | R | 0000 | D2-temperature-data | 47 | R/W | 0000 | DAC-8-CLR-setting |
| 0A | R/W | 003C(1) | Temperature configuration | 48 | R/W | 0000 | DAC-9-CLR-setting |
| 0B | R/W | 0007(1) | Temperature conversion rate | 49 | R/W | 0000 | DAC-10-CLR-setting |
| 21 | R/W | 0000(1) | η-factor correction (for D1) | 4A | R/W | 0000 | DAC-11-CLR-setting |
| 22 | R/W | 0000(1) | η-factor correction (for D2) | 4B | R/W | 00FF | GPIO |
| 23 | R | 0000 | ADC-0-data | 4C | R/W | 2000 | AMC configuration 0 |
| 24 | R | 0000 | ADC-1-data | 4D | R/W | 0070 | AMC configuration 1 |
| 25 | R | 0000 | ADC-2-data | 4E | R/W | 0000 | Alarm control |
| 26 | R | 0000 | ADC-3-data | 4F | R | 0000 | Status |
| 27 | R | 0000 | ADC-4-data | 50 | R/W | 0000 | ADC channel 0 |
| 28 | R | 0000 | ADC-5-data | 51 | R/W | 0000 | ADC channel 1 |
| 29 | R | 0000 | ADC-6-data | 52 | R/W | FFFF | ADC gain |
| 2A | R | 0000 | ADC-7-data | 53 | R/W | 0004 | AUTO-DAC-CLR-SOURCE |
| 2B | R | 0000 | ADC-8-data | 54 | R/W | 0000 | AUTO-DAC-CLR-EN |
| 2C | R | 0000 | ADC-9-data | 55 | R/W | 0000 | SW-DAC-CLR |
| 2D | R | 0000 | ADC-10-data | 56 | R/W | 0000 | HW-DAC-CLR-EN-0 |
| 2E | R | 0000 | ADC-11-data | 57 | R/W | 0000 | HW-DAC-CLR-EN-1 |
| 2F | R | 0000 | ADC-12-data | 58 | R/W | 0000 | DAC configuration |
| 30 | R | 0000 | ADC-13-data | 59 | R/W | 0000 | DAC gain |
| 31 | R | 0000 | ADC-14-data | 5A | R/W | 0FFF | Input-0-high-threshold |
| 32 | R | 0000 | ADC-15-data | 5B | R/W | 0000 | Input-0-low-threshold |
| 33 | R/W | 0000 | DAC-0-data | 5C | R/W | 0FFF | Input-1-high-threshold |
| 34 | R/W | 0000 | DAC-1-data | 5D | R/W | 0000 | Input-1-low-threshold |
| 35 | R/W | 0000 | DAC-2-data | 5E | R/W | 0FFF | Input-2-high-threshold |
| 36 | R/W | 0000 | DAC-3-data | 5F | R/W | 0000 | Input-2-low-threshold |
| 37 | R/W | 0000 | DAC-4-data | 60 | R/W | 0FFF | Input-3-high-threshold |
| 38 | R/W | 0000 | DAC-5-data | 61 | R/W | 0000 | Input-3-low-threshold |
| 39 | R/W | 0000 | DAC-6-data | 62 | R/W | 07FF | LT-high-threshold |
| 3A | R/W | 0000 | DAC-7-data | 63 | R/W | 0800 | LT-low-threshold |
| 3B | R/W | 0000 | DAC-8-data | 64 | R/W | 07FF | D1-high-threshold |
| 3C | R/W | 0000 | DAC-9-data | 65 | R/W | 0800 | D1-low-threshold |
| 3D | R/W | 0000 | DAC-10-data | 66 | R/W | 07FF | D2-high-threshold |
| 3E | R/W | 0000 | DAC-11-data | 67 | R/W | 0800 | D2-low-threshold |
| 3F | R/W | 0000 | DAC-0-CLR-setting | 68 | R/W | 0810 | Hysteresis-0 |
| 40 | R/W | 0000 | DAC-1-CLR-setting | 69 | R/W | 0810 | Hysteresis-1 |
| 41 | R/W | 0000 | DAC-2-CLR-setting | 6A | R/W | 2108 | Hysteresis-2 |
| 42 | R/W | 0000 | DAC-3-CLR-setting | 6B | R/W | 0000 | Power-down |
| 43 | R/W | 0000 | DAC-4-CLR-setting | 6C | R | 1221 | Device ID |
| 44 | R/W | 0000 | DAC-5-CLR-setting | 7C | R/W | N/A | Software reset |

(1) See register descriptions for $I^2C$ default values.

## REGISTER DESCRIPTIONS

### Temperature Data Registers (Read-Only)

In twos complement format, 0.125°C/LSB.

#### *LT-Temperature-Data Register (Address = 00h, Default 0000h, 0°C)*

Store the local temperature sensor reading in twos complement data format.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LT-11 | LT-10 | LT-9 | LT-8 | LT-7 | LT-6 | LT-5 | LT-4 | LT-3 | LT-2 | LT-1 | LT-0 | 0 | 0 | 0 | 0 |

#### *D1-Temperature-Data Register (Address = 01h, Default 0000h, 0°C)*

Store the remote temperature sensor D1 reading in twos complement data format.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D1-11 | D1-10 | D1-9 | D1-8 | D1-7 | D1-6 | D1-5 | D1-4 | D1-3 | D1-2 | D1-1 | D1-0 | 0 | 0 | 0 | 0 |

#### *D2-Temperature-Data Register (Address = 02h, Default 0000h, 0°C)*

Store the remote temperature sensor D2 reading in twos complement data format.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D2-11 | D2-10 | D2-9 | D2-8 | D2-7 | D2-6 | D2-5 | D2-4 | D2-3 | D2-2 | D2-1 | D2-0 | 0 | 0 | 0 | 0 |

### Temperature Configuration Register (Read or Write, Address = 0Ah)

When using the SPI, the following bit configuration must be used; default = 003Ch.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D2EN | D1EN | LTEN | RC | 0 | 0 |

When using the $I^2C$ interface, the following bit configuration must be used; default = 3CFFh.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | D2EN | D1EN | LTEN | RC | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bit descriptions for this register are shown in Table 11.

**Table 11. Temperature Configuration Register Bit Descriptions**

| NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|
| D2EN | 1 | R/W | Remote temperature sensor D2 enable.<br>0 = D2 is disabled<br>1 = D2 is enabled |
| D1EN | 1 | R/W | Remote temperature sensor D1 enable.<br>0 = D1 is disabled<br>1 = D1 is enabled |
| LTEN | 1 | R/W | Local temperature sensor enable.<br>0 = LT is disabled<br>1 = LT is enabled |
| RC | 1 | R/W | Resistance correction enable.<br>0 = Correction is disabled<br>1 = Correction is enabled |

### Temperature Conversion Rate Register (Read or Write, Address = 0Bh)

When using the SPI, the following bit configuration must be used; default = 0007h.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R2 | R1 | R0 |

When using the $I^2C$ interface, the following bit configuration must be used; default = 07FFh.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | R2 | R1 | R0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bit descriptions for this register are shown in Table 12.

**Table 12. Temperature Conversion Time**

| R2 | R1 | R0 | CONVERSION TIME |
|---|---|---|---|
| 0 | 0 | 0 | 128x minimum |
| 0 | 0 | 1 | 64x minimum |
| 0 | 1 | 0 | 32x minimum |
| 0 | 1 | 1 | 16x minimum |
| 1 | 0 | 0 | 8x minimum |
| 1 | 0 | 1 | 4x minimum |
| 1 | 1 | 0 | 2x minimum |
| 1 | 1 | 1 | Minimum cycle time |

**Table 13. Temperature Monitoring Cycle Time**

| TEMPERATURE SENSOR STATUS | MONITORING CYCLE TIME (ms) |
|---|---|
| Local sensor is active, remote sensors are disabled or in power-down. | 15 |
| One remote sensor is active and RC is '0', local sensor and one remote sensor are disabled or in power-down. | 44 |
| One remote sensor is active and RC is '1', local sensor and one remote sensor are disabled or in power-down. | 93 |
| One remote sensor and local sensor are active and RC is '0', one remote sensor is disabled or in power-down. | 59 |
| One remote sensor and local sensor are active and RC is '1', one remote sensor is disabled or in power-down. | 108 |
| Two remote sensors are active and RC is '0', local sensor is disabled or in power-down. | 88 |
| Two remote sensors are active and RC is '1', local sensor is disabled or in power-down. | 186 |
| All sensors are active and RC is '0'. | 103 |
| All sensors are active and RC is '1'. | 201 |

### η-Factor Correction Register (Read or Write, Addresses = 21h and 22h)

Only the low byte is used; the high byte is ignored.

When using the SPI interface, the following bit configuration must be used; default = 0000h.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $N_{ADJUST}$ | | | | | | | |

When using the $I^2C$, the following bit configuration must be used; default = 00FFh.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $N_{ADJUST}$ | | | | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The $N_{ADJUST}$ value for ideality correction is stored as shown in Table 14. $\eta_{EFF}$ is the actual ideality of the transistor being used. Refer to the *Ideality Factor* section for further details.

**Table 14. $N_{ADJUST}$ and $\eta_{EFF}$ Values**

| $N_{ADJUST}$ | | | $\eta_{EFF}$ |
|---|---|---|---|
| **BINARY** | **HEX** | **DECIMAL** | |
| 0111 1111 | 7F | 127 | 1.747977 |
| 0000 1010 | 0A | 10 | 1.042759 |
| 0000 1000 | 08 | 8 | 1.035616 |
| 0000 0110 | 06 | 6 | 1.028571 |
| 0000 0100 | 04 | 4 | 1.021622 |
| 0000 0010 | 02 | 2 | 1.014765 |
| 0000 0001 | 01 | 1 | 1.011371 |
| 0000 0000 | 00 | 0 | 1.008 (default) |
| 1111 1111 | FF | –1 | 1.004651 |
| 1111 1110 | FE | –2 | 1.001325 |
| 1111 1100 | FC | –4 | 0.994737 |
| 1111 1010 | FA | –6 | 0.988235 |
| 1111 1000 | F8 | –8 | 0.981818 |
| 1111 0110 | F6 | –10 | 0.975484 |
| 1000 0000 | 80 | –128 | 0.706542 |

### ADC-*n*-Data Registers (Read-Only, Addresses = 23h to 32h)

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**Bits[11:0]** ADC data.

Four ADC data registers are available. The ADC-*n*-data registers (where n = 0 to 15) store the conversion results of the corresponding analog channel-*n*, as shown in Table 15.

**Table 15. ADC Data Register Definitions**

| INPUT CHANNEL | INPUT TYPE | CONVERSION RESULT STORED IN | FORMAT |
|---|---|---|---|
| Channel 0 | Single-ended | ADC-0-data register | Straight binary |
| Channel 1 | Single-ended | ADC-1-data register | Straight binary |
| Channel 2 | Single-ended | ADC-2-data register | Straight binary |
| Channel 3 | Single-ended | ADC-3-data register | Straight binary |
| CH0+ or CH1– | Differential | ADC-0-data register | Twos complement |
| CH2+ or CH3– | Differential | ADC-2-data register | Twos complement |
| Channel 4 | Single-ended | ADC-4-data register | Straight binary |
| Channel 5 | Single-ended | ADC-5-data register | Straight binary |
| Channel 6 | Single-ended | ADC-6-data register | Straight binary |
| Channel 7 | Single-ended | ADC-7-data register | Straight binary |
| Channel 8 | Single-ended | ADC-8-data register | Straight binary |
| Channel 9 | Single-ended | ADC-9-data register | Straight binary |
| Channel 10 | Single-ended | ADC-10-data register | Straight binary |
| Channel 11 | Single-ended | ADC-11-data register | Straight binary |
| Channel 12 | Single-ended | ADC-12-data register | Straight binary |
| Channel 13 | Single-ended | ADC-13-data register | Straight binary |
| Channel 14 | Single-ended | ADC-14-data register | Straight binary |
| Channel 15 | Single-ended | ADC-15-data register | Straight binary |

### DAC-*n*-Data Registers (Read or Write, Addresses = 33h to 3Eh, Default 0000h)

Each DAC has a DAC data register to store the data (DAC[11:0]) that are loaded into the DAC latches.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Bits[11:0]** DAC data.

### DAC-*n*-CLR-Setting Registers (Read or Write, Addresses = 3Fh to 4Ah, Default 0000h)

Each DAC has a DAC-CLR-setting register to store the data to be loaded into the DAC latch when the DAC is cleared.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DCLR 11 | DCLR 10 | DCLR 9 | DCLR 8 | DCLR 7 | DCLR 6 | DCLR 5 | DCLR 4 | DCLR 3 | DCLR 2 | DCLR 1 | DCLR 0 |

### GPIO Register (Read or Write, Address = 4Bh, Default = 00FFh)

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GPIO-7 | GPIO-6 | GPIO-5 | GPIO-4 | GPIO-3 | GPIO-2 | GPIO-1 | GPIO-0 |

For write operations, the GPIO pin operates as an output. Writing a '0' sets the GPIO-*n* pin to logic low. An external pull-up resistor is required when using the GPIO pin as an output. Writing a '1' to the GPIO-*n* bit sets the GPIO-*n* pin to high impedance.

For read operations, the GPIO pin operates as an input. Read the GPIO-*n* bit to receive the status of the GPIO-*n* pin. Reading a '0' indicates that the GPIO-*n* pin is low; reading a '1' indicates that the GPIO-*n* pin is high.

After power-on reset, or any forced hardware or software reset, the GPIO-*n* bit is set to '1' and is in a high-impedance state.

When D1 is enabled, GPIO-4 and GPIO-5 are ignored.

When D2 is enabled, GPIO-6 and GPIO-7 are ignored.

### AMC Configuration Register 0 (Read or Write, Address = 4Ch, Default = 2000h)

**Table 16. AMC Configuration Register 0**

| BIT | NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|---|
| 15 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 14 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 13 | CMODE | 1 | R/W | ADC conversion mode bit. This bit selects between the two operating conversion modes (direct or auto).<br>0 = Direct mode. The analog inputs specified in the ADC channel registers are converted sequentially (see the ADC channel registers) one time. When one set of conversions are complete, the ADC is idle and waits for a new trigger.<br>1 = Auto mode. The analog inputs specified in the AMC channel registers are converted sequentially and repeatedly (see the ADC channel registers). When one set of conversions are complete, the ADC multiplexer returns to the first channel and repeats the process. Repetitive conversions continue until the CMODE bit is cleared ('0'). |
| 12 | ICONV | 0 | R/W | Internal conversion bit.<br>Set this bit to '1' to start the ADC conversion internally. The bit is automatically cleared ('0') after the ADC conversion starts. |
| 11 | ILDAC | 0 | R/W | Load DAC bit.<br>Set this bit to '1' to synchronously load the DAC data registers, which are programmed for synchronous update mode (SLDAC-*n* = 1). The AMC7812B updates the DAC latch only if the ILDAC bit is set ('1'), thereby eliminating any unnecessary glitches. Any DAC channels that are not accessed are not reloaded. When the DAC latch is updated, the corresponding output changes to the new level immediately. This bit is cleared ('0') after the DAC data register is updated. |
| 10 | ADC-REF-INT | 0 | R/W | ADC $V_{REF}$ select bit.<br>0 = The internal reference buffer is off and the external reference drives the ADC.<br>1 = The internal buffer is on and the internal reference drives the ADC. Note that a compensation capacitor is required. |
| 9 | EN-ALARM | 0 | R/W | Enable $\overline{\text{ALARM}}$ pin bit.<br>0 = The $\overline{\text{ALARM}}$ pin is disabled<br>1 = The $\overline{\text{ALARM}}$ pin is enabled |
| 8 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 7 | DAVF | | R | ADC Data available flag bit. For direct mode only. Always cleared (set to '0') in Auto mode.<br>0 = The ADC conversion is in progress (data are not ready) or the ADC is in auto mode.<br>1 = The ADC conversions are complete and new data are available.<br>In direct mode, the DAVF bit sets the DAV pin. DAV goes low when DAVF is '1', and goes high when DAVF is '0'.<br>In auto mode, DAVF is always cleared to '0'. However, a 1-µs pulse (active low) appears on the DAV pin when the last input specified in the ADC channel registers is converted. DAVF is cleared to '0' in one of three ways: by reading the ADC data register, by starting a new ADC conversion, or by writing '0' to this bit. Reading the status register does not clear this bit. |
| 6 | GALR | 0 | R | Global alarm bit.<br>This bit is the OR function of all individual alarm bits of the status register. This bit is set ('1') when any alarm condition occurs, and remains '1' until the status register is read. This bit is cleared ('0') after reading the status register. |
| 5 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 4 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 3 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 2 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 1 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 0 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |

### AMC Configuration Register 1 (Read or Write, Address = 4Dh, Default = 0070h)

**Table 17. AMC Configuration Register 1**

| BIT | NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|---|
| 15 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 14 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 13 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 12 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 11 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 10 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 9 | CONV-RATE-1 | 0 | R/W | ADC conversion rate bit. See Table 18. |
| 8 | CONV-RATE-0 | 0 | R/W | ADC conversion rate bit. See Table 18. |
| 7 | CH-FALR- CT-2 | 0 | R/W | False alarm protection bit for CH0 to CH3. See Table 19. |
| 6 | CH-FALR- CT-1 | 1 | R/W | False alarm protection bit for CH0 to CH3. See Table 19. |
| 5 | CH-FALR- CT-0 | 1 | R/W | False alarm protection bit for CH0 to CH3. See Table 19. |
| 4 | TEMP-FALR- CT-1 | 1 | R/W | False alarm protection bit for temperature monitor. See Table 20. |
| 3 | TEMP-FALR- CT-0 | 0 | R/W | False alarm protection bit for temperature monitor. See Table 20. |
| 2 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 1 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 0 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |

**Table 18. CONV-RATE-[1:0] Bit Settings**

| CONV-RATE-1 | CONV-RATE-0 | ADC CONVERSION RATE |
|---|---|---|
| 0 | 0 | 500 kSPS, the specified rate (default) |
| 0 | 1 | 1/2 of the specified rate |
| 1 | 0 | 1/4 of the specified rate |
| 1 | 1 | 1/8 of the specified rate |

**Table 19. CH-FALR-CT-[2:0] Bit Settings**

| CH-FALR-CT-2 | CH-FALR-CT-1 | CH-FALR-CT-0 | *N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 4 |
| 0 | 1 | 0 | 8 |
| 0 | 1 | 1 | 16 (default for CH0 to CH3) |
| 1 | 0 | 0 | 32 |
| 1 | 0 | 1 | 64 |
| 1 | 1 | 0 | 128 |
| 1 | 1 | 1 | 256 |

**Table 20. TEMP-FALR-CT-[1:0] Bit Settings**

| TEMP-FALR-CT-1 | TEMP-FALR-CT-0 | *N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 (default) |
| 1 | 1 | 8 |

### Alarm Control Register (Read or Write, Address = 4Eh, Default = 0000h)

The alarm control register determines whether the $\overline{\text{ALARM}}$ pin is accessed when a corresponding alarm event occurs. However, this register does not affect the status bit in the status register. Note that the thermal alarm is always enabled. When the THERM_ALR bit is '1', the $\overline{\text{ALARM}}$ pin goes low if the pin is enabled.

**Table 21. Alarm Control Register**

| BIT | NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|---|
| 15 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 14 | EALR-CH0 | 0 | R/W | CH0 and (CH0+, CH1–) alarm enable bit.<br>0 = The alarm is masked. When the input of CH0 or (CH0+, CH1–) is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH0-ALR bit is set.<br>1 = The alarm is enabled, the CH0-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH0 or (CH0+, CH1–) is out of range. |
| 13 | EALR-CH1 | 0 | R/W | CH1 alarm enable bit.<br>0 = The alarm is masked. When the input of CH1 is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH1-ALR bit is set.<br>1 = The alarm is enabled, the CH1-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH1 is out of range. |
| 12 | EALR-CH2 | 0 | R/W | CH2 and (CH2+, CH3–) alarm enable bit.<br>0 = The alarm is masked. When the input of CH2 or (CH2+, CH3–) is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH2-ALR bit is set.<br>1 = The alarm is enabled, the CH2-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH2 or (CH2+, CH3–) is out of range. |
| 11 | EALR-CH3 | 0 | R/W | CH3 alarm enable bit.<br>0 = The alarm is masked. When the input of CH3 is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH3-ALR bit is set.<br>1 = The alarm is enabled, the CH3-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH3 is out of range. |
| 10 | EALR-LT-Low | 0 | R/W | Local sensor low alarm enable bit.<br>0 = The LT-Low alarm is masked. When LT is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the LT-Low-ALR bit is set.<br>1 = The LT-Low alarm is enabled. When LT is below the specified range, the LT-Low-ALR bit is set ('1') and the $\overline{\text{ALARM}}$ pin goes low (if enabled). |
| 9 | EALR-LT-High | 0 | R/W | Local sensor high alarm enable bit.<br>0 = The LT-High alarm is masked. When LT is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the LT-High-ALR bit is set.<br>1 = The LT-High alarm is enabled. When LT is above the specified range, the LT-High-ALR bit is set ('1') and the $\overline{\text{ALARM}}$ pin goes low (if enabled). |
| 8 | EALR-D1-Low | 0 | R/W | D1 low alarm enable bit.<br>0 = The D1-Low alarm is masked. When D1 is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D1-Low-ALR bit is set.<br>1 = The D1-Low alarm is enabled. When D1 is below the specified range, the D1-Low-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). |
| 7 | EALR-D1-High | 0 | R/W | D1 high alarm enable bit.<br>0 = The D1-High alarm is masked. When D1 is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D1-High-ALR bit is set.<br>1 = The D1-High alarm is enabled. When D1 is above the specified range, the D1-High-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). |
| 6 | EALR-D2-Low | 0 | R/W | D2 low alarm enable bit.<br>0 = The D2-Low alarm is masked. When D2 is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D2-Low-ALR bit is set.<br>1 = The D2-Low alarm is enabled. When D2 is below the specified range, the D2-Low-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). |
| 5 | EALR-D2-High | 0 | R/W | D2 high alarm enable bit.<br>0 = The D2-High alarm is masked. When D2 is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D2-High-ALR bit is set.<br>1 = The D2-High alarm is enabled. When D2 is above the specified range, the D2-High-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). |

**Table 21. Alarm Control Register (continued)**

| BIT | NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|---|
| 4 | EALR-D1-FAIL | 0 | R/W | D1 fail alarm enable bit.<br>0 = The D1-FAIL alarm is masked. When D1 fails, the $\overline{\text{ALARM}}$ pin does not go low, but the D1-FAIL-ALR bit is set.<br>1 = The D1-Fail alarm is enabled. When D1 fails, the D1-FAIL-ALR bit is set ('1'), the $\overline{\text{ALARM}}$ pin goes low (if enabled). |
| 3 | EALR-D2-FAIL | 0 | R/W | D2 fail alarm enable bit.<br>0 = The D2-FAIL alarm is masked. When D2 fails, the $\overline{\text{ALARM}}$ pin does not go low, but the D2-FAIL-ALR bit is set.<br>1 = The D2-Fail alarm is enabled. When D2 fails, the D2-FAIL-ALR bit is set ('1'), the $\overline{\text{ALARM}}$ pin goes low (if enabled). |
| 2 | ALARM-LATCH-DIS | 0 | R/W | Alarm latch disable bit.<br>0 = The status register bits are latched. When an alarm occurs, the corresponding alarm bit is set ('1'). The alarm bit remains '1' until the error condition subsides and the status register is read. Before reading, the alarm bit is not cleared ('0') even if the alarm condition disappears.<br>1 = The status register bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the status register is read or not. |
| 1 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 0 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |

### Status Register (Read-Only, Address = 4Fh, Default = 0000h)

The AMC7812B continuously monitors all analog inputs and temperatures during normal operation. When any input is out of the specified range for *N* consecutive times, the corresponding alarm bit is set ('1'). If the input returns to the normal range before *N* consecutive times, the corresponding alarm bit remains clear ('0'). This configurations avoids any false alarms.

When an alarm status occurs, the corresponding alarm bit is set ('1'). When the ALARM-LATCH-DIS bit in the alarm control register is cleared ('0'), the $\overline{\text{ALARM}}$ pin is latched. Whenever an alarm status bit is set, that bit remains set until the event that caused the alarm is resolved and the status register is read. Reading the status registers clears the alarm status bit. The alarm bit can only be cleared by reading the status register after the event is resolved, or by hardware reset, software reset, or power-on reset. All alarm status bits are cleared when reading the status register, and all these bits are reasserted if the out-of-limit condition still exists after the next conversion cycle, unless otherwise noted.

When the ALARM-LATCH-DIS bit in the alarm control register is set ('1'), the $\overline{\text{ALARM}}$ pin is not latched. The alarm bit goes to '0' when the error condition subsides, regardless of whether the bit is read or not.

**Table 22. Status Register**

| BIT | NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|---|
| 15 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 14 | CH0-ALR | 0 | R | 0 = The analog input is not out of the specified range.<br>1 = The single-ended channel 0 or differential input pair (CH0+, CH1–) is out of the range defined by the corresponding threshold registers. |
| 13 | CH1-ALR | 0 | R | 0 = The analog input is not out of the specified range.<br>1 = The single-ended channel 1 is out of the range defined by the corresponding threshold registers. |
| 12 | CH2-ALR | 0 | R | 0 = The analog input is not out of the specified range.<br>1 = The single-ended channel 2 or differential input pair (CH2+, CH3–) is out of the range defined by the corresponding threshold registers. |
| 11 | CH3-ALR | 0 | R | 0 = The analog input is not out of the specified range.<br>1 = The single-ended channel 3 is out of the range defined by the corresponding threshold registers. |
| 10 | LT-Low-ALR | 0 | R | Local temperature underrange flag.<br>0 = The local temperature is not less than the range.<br>1 = The local temperature is less than the low-bound threshold.<br>This bit is only checked when LT is enabled (EN-LT is '1'); this bit is ignored when EN-LT is '0'. |
| 9 | LT-High-ALR | 0 | R | Local temperature overrange flag.<br>0 = The local temperature is not greater than the range.<br>1 = The local temperature is greater than the high-bound threshold.<br>This bit is only checked when LT is enabled (EN-LT is '1'); this bit is ignored when EN-LT is '0'. |
| 8 | D1-Low-ALR | 0 | R | Remote temperature reading of D1 when less than the range flag.<br>0 = The local temperature is not less than the range.<br>1 = The local temperature is less than the low-bound threshold.<br>This bit is only checked when D1 is enabled (EN-D1 is '1'); this bit is ignored when EN-D1 is '0'. |
| 7 | D1-High -ALR | 0 | R | Remote temperature reading of D1 when greater than the range flag.<br>0 = The local temperature is not greater than the range.<br>1 = The local temperature is greater than the high-bound threshold.<br>This bit is only checked when D1 is enabled (EN-D1 is '1'); this bit is ignored when EN-D1 is '0'. |
| 6 | D2-Low-ALR | 0 | R | Remote temperature reading of D2 when less than the range flag.<br>0 = The local temperature is not less than the range.<br>1 = The local temperature is less than the low-bound threshold.<br>This bit is only checked when D2 is enabled (EN-D2 is '1'); this bit is ignored when EN-D2 is '0'. |

**Table 22. Status Register (continued)**

| BIT | NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|---|
| 5 | D2-High -ALR | 0 | R | Remote temperature reading of D2 when greater than the range flag.<br>0 = The local temperature is not greater than the range.<br>1 = The local temperature is greater than the high-bound threshold.<br>This bit is only checked when D2 is enabled (EN-D2 is '1'); this bit is ignored when EN-D2 is '0'. |
| 4 | D1-FAIL-ALR | 0 | R | Remote sensor D1 failure flag.<br>0 = The sensor is in a normal condition.<br>1 = The sensor is an open-circuit or short-circuit.<br>This bit is only checked when D1 is enabled (EN-D1 is '1'); this bit is ignored when EN-D1 is '0'. |
| 3 | D2-FAIL-ALR | 0 | R | Remote sensor D2 failure flag.<br>0 = The sensor is in a normal condition.<br>1 = The sensor is an open-circuit or short-circuit.<br>This bit is only checked when D2 is enabled (EN-D2 is '1'); this is ignored when EN-D2 is '0'. |
| 2 | THERM-ALR | 0 | R | Thermal alarm flag.<br>When the die temperature is equal to or greater than +150°C, the bit is set ('1') and the THERM-ALR flag activates. The on-chip temperature sensor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always '0'. The hysteresis of this alarm is 8°C. |
| 1 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 0 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |

### ADC Channel Register 0 (Read or Write, Address = 50h, Default = 0000h)

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | SE0 | SE1 | DF (CH0+, CH1–) | SE2 | SE3 | DF (CH2+, CH3–) | SE4 | SE5 | SE6 | SE7 | SE8 | SE9 | SE10 | SE11 | SE12 |

These bits specify the external analog auxiliary input channels (CH0 to CH12) to be converted. The specified channels are accessed sequentially in order from bit 14 to bit 0. The input is converted when the corresponding bit is set ('1').

**Bit 15** **Reserved**

Writing to this bit causes no change. Reading this bit returns '0'.

**Bits 14, 13, 11, 10, 8:0** **SE0 to SE12**

External single-ended analog input for CH*n*. The result is stored in ADC-*n*-data register in straight binary format.

**Bit 12** **DF (CH0+, CH1–)**

External analog differential input pair, CH0 and CH1, with CH0 as positive and CH1 as negative. The difference of (CH0 – CH1) is converted and the result is stored in the ADC-0-data register in twos complement format.

**Bit 9** **DF(CH2+, CH3-)**

External analog differential input pair, CH2 and CH3, with CH2 as positive and CH3 as negative. The difference of (CH2 – CH3) is converted and the result is stored in the ADC-2-data register in twos complement format.

**Table 23. CH0 and CH1 Bit Settings**

| BIT 14 | BIT 13 | BIT 12 | DESCRIPTION |
|---|---|---|---|
| 1 | 1 | 0 | CH0 and CH1 are both accessed as single-ended inputs. Bit 12 is ignored. |
| 1 | 0 | 0 | CH0 is accessed as a single-ended input. CH1 is not accessed. Bit 12 is ignored. |
| 0 | 1 | 0 | CH1 is accessed as a singled-ended. CH0 is not accessed. Bit 12 is ignored. |
| 0 | 0 | 1 | Differential input pair CH0 + and CH1– is accessed as a differential input. |
| 0 | 0 | 0 | CH0, CH1, and differential pair CH0+, CH1– are not accessed. |

**Table 24. CH2 and CH3 Bit Settings**

| BIT 11 | BIT 10 | BIT 9 | DESCRIPTION |
|---|---|---|---|
| 1 | 1 | 0 | CH2 and CH3 are both accessed as single-ended inputs. Bit 9 is ignored. |
| 1 | 0 | 0 | CH2 is accessed as a single-ended input. CH3 is not accessed. Bit 9 is ignored. |
| 0 | 1 | 0 | CH3 is accessed as a singled-end input. CH2 is not accessed. Bit 9 is ignored. |
| 0 | 0 | 1 | Differential input pair CH2+ and CH3– is accessed as a differential input. |
| 0 | 0 | 0 | CH2, CH3, and differential pair CH2+, CH3– are not accessed. |

**Table 25. CH4 to CH12 Bit Settings**

| BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|
| 1 | — | — | — | — | — | — | — | — | CH4 is accessed as a single-ended input |
| — | 1 | — | — | — | — | — | — | — | CH5 is accessed as a single-ended input |
| — | — | 1 | — | — | — | — | — | — | CH6 is accessed as a single-ended input |
| — | — | — | 1 | — | — | — | — | — | CH7 is accessed as a single-ended input |
| — | — | — | — | 1 | — | — | — | — | CH8 is accessed as a single-ended input |
| — | — | — | — | — | 1 | — | — | — | CH9 is accessed as a single-ended input |
| — | — | — | — | — | — | 1 | — | — | CH10 is accessed as a single-ended input |
| — | — | — | — | — | — | — | 1 | — | CH11 is accessed as a single-ended input |
| — | — | — | — | — | — | — | — | 1 | CH12 is accessed as a single-ended input |

### ADC Channel Register 1 (Read or Write, Address = 51h, Default = 0000h)

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | SE13 | SE14 | SE15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

These bits specify the external analog auxiliary input channels (CH13, CH14, and CH15) to be converted. The specified channel is accessed sequentially in the order from bit 14 to bit 0 of ADC channel register 0, and then bit 14 to bit 12 of ADC channel register 1. The input is converted when the corresponding bit is set ('1').

**Bits[14:12]** **SE*n***

External single-ended analog input CH*n*. The result is stored in the ADC-*n*-data register in straight binary format.

### ADC Gain Register (Read or Write, Address = 52h, Default = FFFFh)

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADG0 | ADG1 | ADG2 | ADG3 | ADG4 | ADG5 | ADG6 | ADG7 | ADG8 | ADG9 | ADG10 | ADG11 | ADG12 | ADG13 | ADG14 | ADG15 |

**Bit 15** **ADG0**
0 = The analog input range of single-ended input CH0 (SE0) is 0 V to $V_{REF}$ or differential input pair DF (CH0+, CH1–) is $–V_{REF}$ to $+V_{REF}$
1 = The analog input range of single-ended input CH0 (SE0) is 0 V to ($2 \times V_{REF}$) or differential input pair DF (CH0+, CH1–) is ($–2 \times V_{REF}$) to ($+2 \times V_{REF}$)

**Bit 14** **ADG1**
0 = The analog input range of single-ended input CH1 (SE1) is 0 V to $V_{REF}$
1 = The analog input range is 0 V to ($2 \times V_{REF}$)

**Bit 13** **ADG2**
0 = The analog input range of single-ended input CH2 (SE2) is 0 V to $V_{REF}$ or differential input pair DF (CH2+, CH3–) is $–V_{REF}$ to $+V_{REF}$
1 = The analog input range of single-ended input CH2 (SE2) is 0 V to ($2 \times V_{REF}$) or differential input pair DF (CH2+, CH3–) is ($–2 \times V_{REF}$) to ($+2 \times V_{REF}$)

**Bit 12** **ADG3**
0 = The analog input range of single-end input CH3 (SE3) is 0 V to $V_{REF}$
1 = The analog input range is 0 V to ($2 \times V_{REF}$)

**Bit[11:0]** **ADG4 to ADG15**
0 = The analog input range of CH*n* (where n = 4 to 15) is 0 V to $V_{REF}$
1 = The analog input range is 0 V to ($2 \times V_{REF}$)

### AUTO-DAC-CLR-SOURCE Register (Read or Write, Address = 53h, Default = 0004h)

This register selects which alarm forces the DAC into a *clear* state, regardless of which DAC operation mode is active, auto, or manual.

**Table 26. AUTO-DAC-CLR-SOURCE Register**

| BIT | NAME | DEFAULT | R/W | DESCRIPTION |
|---|---|---|---|---|
| 15 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 14 | CH0-ALR-CLR | 0 | R/W | CH0 alarm clear bit.<br>0 = CH1-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC-*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the CH0-ALR bit in the status register are set ('1') |
| 13 | CH1-ALR-CLR | 0 | R/W | CH1 alarm clear bit.<br>0 = CH1-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the CH1-ALR bit in the status register are set ('1') |
| 12 | CH2-ALR-CLR | 0 | R/W | CH2 alarm clear bit.<br>0 = CH2-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the CH2-ALR bit in the status register are set ('1') |
| 11 | CH3-ALR-CLR | 0 | R/W | CH3 alarm clear bit.<br>0 = CH3-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the CH3-ALR bit in the status register are set ('1') |
| 10 | LT-Low-ALR-CLR | 0 | R/W | Local temperature sensor low alarm clear bit.<br>0 = LT-Low-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the LT-Low-ALR bit in the status register are set ('1') |
| 9 | LT-High-ALR-CLR | 0 | R/W | Local temperature sensor high alarm clear bit.<br>0 = LT-High-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the LT-High-ALR bit in the status register are set ('1') |
| 8 | D1-Low-ALR-CLR | 0 | R/W | Remote temperature sensor D1 low alarm clear bit.<br>0 = D1-Low-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the D1-Low-ALR bit in the status register are set ('1') |
| 7 | D1-High-ALR-CLR | 0 | R/W | Remote temperature sensor D1 high alarm clear bit.<br>0 = D1-High-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the D1-High-ALR bit in the status register are set ('1') |
| 6 | D2-Low-ALR-CLR | 0 | R/W | Remote temperature sensor D2 low alarm clear bit.<br>0 = D2-Low-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the D2-Low-ALR bit in the status register are set ('1') |
| 5 | D2-High-ALR-CLR | 0 | R/W | Remote temperature sensor D2 high alarm clear bit.<br>0 = D2-High-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the D2-High-ALR bit in the status register are set ('1') |
| 4 | D1-FAIL-CLR | 0 | R/W | D1 fail alarm clear bit.<br>0 = D1-FAIL-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the D2-FAIL-ALR bit in the status register are set ('1') |
| 3 | D2-FAIL-CLR | 0 | R/W | D2 fail alarm clear bit.<br>0 = D2-FAIL-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the D2-FAIL-ALR bit in the status register are set ('1') |
| 2 | THERM-ALR-CLR | 1 | R/W | Thermal alarm clear bit.<br>0 = THERM-ALR goes to '1' and does not force any DAC to a clear status<br>1 = DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO-DAC-CLR-EN register and the THERM-ALR bit in the status register are set ('1') |
| 1 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |
| 0 | — | 0 | R | Reserved. Writing to this bit causes no change. Reading this bit returns '0'. |

### AUTO-DAC-CLR-EN Register (Read or Write, Address = 54h, Default = 0000h)

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ACLR 11 | ACLR 10 | ACLR 9 | ACLR 8 | ACLR 7 | ACLR 6 | ACLR 5 | ACLR 4 | ACLR 3 | ACLR 2 | ACLR 1 | ACLR 0 | 0 | 0 | 0 |

**Bits[14:3]** **ACLR*n***

Auto clear DAC-*n* enable bit.
0 = DAC-*n* is not forced to a clear state when the alarm occurs (default)
1 = DAC-*n* is forced to a clear state when the alarm occurs

**NOTE**

ACLR*n* is always ignored when an alarm occurs for a temperature greater than +150°C (THERM-ALR is '1'). If an alarm activates for a temperature greater than +150°C, and if the THERM-ALR-CLR bit in the AUTO-DAC-CLR-SOURCE register is set ('1'), all DACs are forced into a clear status. However, if THERM-ALR-CLR is cleared ('0'), the over +150°C alarm does not force any DAC to a clear status.

### SW-DAC-CLR Register (Read or Write, Address = 55h, Default = 0000h)

This register uses software to force the DAC into a clear state.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ICLR 11 | ICLR 10 | ICLR 9 | ICLR 8 | ICLR 7 | ICLR 6 | ICLR 5 | ICLR 4 | ICLR 3 | ICLR 2 | ICLR 1 | ICLR 0 | 0 | 0 | 0 |

**Bits[14:3]** **ICLR*n***

Software clear DAC*n* bit.
0 = DAC*n* is restored to normal operation
1 = DAC*n* is forced into a clear state

### HW-DAC-CLR-EN 0 Register (Read or Write, Address = 56h, Default = 0000h)

This register determines which DAC is in a clear state when the $\overline{\text{DAC-CLR-0}}$ pin goes low.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | H0CLR 11 | H0CLR 10 | H0CLR 9 | H0CLR 8 | H0CLR 7 | H0CLR 6 | H0CLR 5 | H0CLR 4 | H0CLR 3 | H0CLR 2 | H0CLR 1 | H0CLR 0 | 0 | 0 | 0 |

**Bits[14:3]** **H0CLR*n*:** Hardware clear DAC-*n* enable 1 bit.

If H0CLR*n* = '1', DAC-*n* is forced into a clear state when the $\overline{\text{DAC-CLR-0}}$ pin goes low.

If H0CLR*n* = '0', pulling the $\overline{\text{DAC-CLR-0}}$ pin low does not effect the state of DAC-*n*.

### HW-DAC-CLR-EN 1 Register (Read or Write, Address = 57h, Default = 0000h)

This register determines which DAC is in a clear state when the $\overline{\text{DAC-CLR-1}}$ pin goes low.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | H1CLR 11 | H1CLR 10 | H1CLR 9 | H1CLR 8 | H1CLR 7 | H1CLR 6 | H1CLR 5 | H1CLR 4 | H1CLR 3 | H1CLR 2 | H1CLR 1 | H1CLR 0 | 0 | 0 | 0 |

**Bits[14:3]** **H1CLR*n***

Hardware clear DAC-*n* enable 1 bit.
0 = Pulling the $\overline{\text{DAC-CLR-1}}$ pin low does not effect the state of DAC-*n*
1 = DAC-*n* is forced into a clear state when the $\overline{\text{DAC-CLR-1}}$ pin goes low

### DAC Configuration Register (Read or Write, Address = 58h, Default = 0000h)

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | SLDA 11 | SLDA 10 | SLDA 9 | SLDA 8 | SLDA 7 | SLDA 6 | SLDA 5 | SLDA 4 | SLDA 3 | SLDA 2 | SLDA 1 | SLDA 0 |

**Bits[11:0]** **SLDA-*n***

DAC synchronous load enable bit.
0 = Asynchronous load is enabled. A write command to the DAC-*n*-data register immediately updates the DAC-*n* latch and the output of DAC-*n*. The synchronous load DAC signal (ILDAC) does not affect DAC*n*. the default value of SLDA-*n* is '0'. The device updates the DAC latch only if the ILDAC bit is set ('1'), thereby eliminating unnecessary glitches. Any DAC channels that are not accessed are not reloaded. When the DAC latch is updated, the corresponding output changes to the new level immediately. Note that the SLDA-*n* bit is ignored in auto mode (DAC-*n* mode bits do not equal '00'). In auto mode, the DAC latch is always updated asynchronously.
1 = Synchronous load is enabled. When internal load DAC signal ILDAC occurs, the DAC-*n* latch is loaded with the value of the corresponding DAC*n*-data register, and the output of DAC-*n* is updated immediately. The internal load DAC signal ILDAC is generated by writing a '1' to the ILDAC bit in the AMC configuration register. In synchronous load, a write command to the DAC-*n*-data register updates that register only, and does not change the DAC-*n* output.

**NOTE**

The DACs can be forced to a clear state immediately by the external $\overline{\text{DAC-CLR-n}}$ signal, by alarm events, and by writing to the SW-DAC-CLR register. In these cases, the SLDA-*n* bit is ignored.

### DAC Gain Register (Read or Write, Address = 59h, Default = 0000h)

The DAC*n* GAIN bits specify the output range of DAC*n*.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DAC11 GAIN | DAC10 GAIN | DAC9 GAIN | DAC8 GAIN | DAC7 GAIN | DAC6 GAIN | DAC5 GAIN | DAC4 GAIN | DAC3 GAIN | DAC2 GAIN | DAC1 GAIN | DAC0 GAIN |

**Bits[11:0]** **DAC*n*GAIN:** DAC*n* gain bits.

1 = Gain is 5 and the output is 0 V to 5 × $V_{REF}$

0 = Gain is 2 and the output is 0 V to 2 × $V_{REF}$

### Analog Input Channel Threshold Registers (Read or Write, Addresses = 5Ah to 61h)

Four analog auxiliary inputs (CH0, CH1, CH2, and CH3) and three temperature sensors (LT, D1, and D2) implement an out-of-range alarm function. Threshold-High-*n* and Threshold-Low-*n* (where n = 0, 1, 2, 3) define the upper bound and lower bound of the *n*th analog input range, as shown in Table 27. This window determines whether the *n*th input is out-of-range. When the input is outside the window, the corresponding CH-ALR-*n* bit in the status register is set to '1'.

For normal operation, the value of Threshold-High-*n* must be greater than the value of Threshold-Low-*n*; otherwise, CH-ALR-*n* is always set to '1' and an alarm is always indicated. Note that when the analog channel is accessed as single-ended input, its threshold is in a straight binary format. However, when the channel is accessed as a differential pair, its threshold is in twos complement format.

**Table 27. Threshold Coding**

| INPUT CHANNEL | INPUT TYPE | THRESHOLD STORED IN | FORMAT |
|---|---|---|---|
| Channel 0 | Single-ended | Input-0-Threshold-High-Byte<br>Input-0-Threshold-Low-Byte | Straight binary |
| Channel 1 | Single-ended | Input-1-Threshold-High-Byte<br>Input-1-Threshold-Low-Byte | Straight binary |
| Channel 2 | Single-ended | Input-2-Threshold-High-Byte<br>Input-2-Threshold-Low-Byte | Straight binary |
| Channel 3 | Single-ended | Input-3-Threshold-High-Byte<br>Input-3-Threshold-Low-Byte | Straight binary |
| CH0+, CH1– | Differential | Input-0-Threshold-High-Byte<br>Input-0-Threshold-Low-Byte | Twos complement |
| CH2+, CH3– | Differential | Input-2-Threshold-High-Byte<br>Input-2-Threshold-Low-Byte | Twos complement |

#### *Input-n-High-Threshold Register (where n = 0, 1, 2, 3) (Read or Write, Default = 0FFFh)*

| MSB<br>BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB<br>BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRH 11 | THRH 10 | THRH 9 | THRH 8 | THRH 7 | THRH 6 | THRH 5 | THRH 4 | THRH 3 | THRH 2 | THRH 1 | THRH 0 |

**Bits[15:12]** **Reserved**

These bits are '0' when read back. Writing to these bits has no effect.

**Bits[11:0]** **THRH*n***

Data bits of the upper-bound threshold of the *n*th analog input.

#### *Input-n-Low-Threshold Register (where n = 0, 1, 2, 3) (Read or Write, Default = 0000h)*

| MSB<br>BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB<br>BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRL 11 | THRL 10 | THRL 9 | THRL 8 | THRL 7 | THRL 6 | THRL 5 | THRL 4 | THRL 3 | THRL 2 | THRL 1 | THRL 0 |

**Bits[15:12]** **Reserved**

These bits are '0' when read back. Writing to these bits has no effect.

**Bits[11:0]** **THRL*n***

Data bits of the lower-bound threshold of the *n*th analog input.

## Temperature Threshold Registers

### *LT-High-Threshold Register (Read or Write, Address = 62h, Default = 07FFh, +255.875°C)*

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRH 11 | THRH 10 | THRH 9 | THRH 8 | THRH 7 | THRH 6 | THRH 5 | THRH 4 | THRH 3 | THRH 2 | THRH 1 | THRH 0 |

Bits[15:12] are ‘0' when read back. Writing these bits causes no change

### *LT-Low-Threshold Register (Read or Write, Address = 63h, Default = 0800h, –256°C)*

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRL 11 | THRL 10 | THRL 9 | THRL 8 | THRL 7 | THRL 6 | THRL 5 | THRL 4 | THRL 3 | THRL 2 | THRL 1 | THRL 0 |

Bits[15:12] are reserved. Writing to these bits causes no change. Reading these bits returns '0'.

### *D1-High-Threshold Register (Read or Write, Address = 64h, Default = 07FFh, +255.875°C)*

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRH 11 | THRH 10 | THRH 9 | THRH 8 | THRH 7 | THRH 6 | THRH 5 | THRH 4 | THRH 3 | THRH 2 | THRH 1 | THRH 0 |

Bits[15:12] are ‘0' when read back. Writing these bits causes no change.

### *D1-Low-Threshold Register (Read or Write, Address = 65h, Default = 0800h, –256°C)*

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRL 11 | THRL 10 | THRL 9 | THRL 8 | THRL 7 | THRL 6 | THRL 5 | THRL 4 | THRL 3 | THRL 2 | THRL 1 | THRL 0 |

Bits[15:12] are ‘0' when read back. Writing these bits causes no change.

### *D2-High-Threshold Register (Read or Write, Address = 66h, Default = 07FFh, +255.875°C)*

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRH 11 | THRH 10 | THRH 9 | THRH 8 | THRH 7 | THRH 6 | THRH 5 | THRH 4 | THRH 3 | THRH 2 | THRH 1 | THRH 0 |

Bits[15:12] are ‘0' when read back. Writing these bits causes no change.

### *D2-Low-Threshold Register (Read or Write, Address = 67h, Default = 0800h, –256°C)*

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | THRL 11 | THRL 10 | THRL 9 | THRL 8 | THRL 7 | THRL 6 | THRL 5 | THRL 4 | THRL 3 | THRL 2 | THRL 1 | THRL 0 |

Bits[15:12] are ‘0' when read back. Writing these bits causes no change.

### Hysteresis Registers

The hysteresis registers define the hysteresis in the alarm detection of an individual alarm.

#### *Hysteresis Register 0 (Read or Write, Address = 68h, Default = 0810h, 8 LSB)*

This register contains the hysteresis values for CH0 and CH1.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | CH0-HYS-6 | CH0-HYS-5 | CH0-HYS-4 | CH0-HYS-3 | CH0-HYS-2 | CH0-HYS-1 | CH0-HYS-0 | CH1-HYS-6 | CH1-HYS-5 | CH1-HYS-4 | CH1-HYS-3 | CH1-HYS-2 | CH1-HYS-1 | CH1-HYS-0 | 0 |

**Bits[14:8]** **CH0-HYS-*n***

Hysteresis of CH0, 1 LSB per step.

**Bits[7:1]** **CH1-HYS-*n***

Hysteresis of CH1, 1 LSB per step.

#### *Hysteresis Register 1 (Read or Write, Address = 69h, Default = 0810h, 8 LSB)*

This register contains the hysteresis values for CH2 and CH3.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | CH2-HYS-6 | CH2-HYS-5 | CH2-HYS-4 | CH2-HYS-3 | CH2-HYS-2 | CH2-HYS-1 | CH2-HYS-0 | CH3-HYS-6 | CH3-HYS-5 | CH3-HYS-4 | CH3-HYS-3 | CH3-HYS-2 | CH3-HYS-1 | CH3-HYS-0 | 0 |

**Bits[14:8]** **CH2-HYS-*n***

Hysteresis of CH2, 1 LSB per step.

**Bits[7:1]** **CH3-HYS-*n***

Hysteresis of CH3, 1 LSB per step.

#### *Hysteresis Register 2 (Read or Write, Address = 6Ah, Default = 2108h, 8°C)*

This register contains the hysteresis values for D2, D1, and LT. The range is 0°C to +31°C.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | D2-HYS-7 | D2-HYS-6 | D2-HYS-5 | D2-HYS-4 | D2-HYS-3 | D1-HYS-7 | D1-HYS-6 | D1-HYS-5 | D1-HYS-4 | D1-HYS-3 | LT-HYS-7 | LT-HYS-6 | LT-HYS-5 | LT-HYS-4 | LT-HYS-3 |

**Bits[14:10]** **D2-HYS-*n***

Hysteresis of D2, 1°C per step. Note that bits D2-HYS-[2:0] are always '0'.

**Bits[9:5]** **D1-HYS-*n***

Hysteresis of D1, 1°C per step. Note that bits D1-HYS-[2:0] are always '0'.

**Bits[4:0]** **LT-HYS-*n***

Hysteresis of LT, 1°C per step. Note that bits LT-HYS-[2:0] are always '0'.

### Power-Down Register (Read or Write, Address = 6Bh, Default = 0000h)

After power-on or reset, all bits in the Power-Down Register are cleared to '0', and all the components controlled by this register are either powered-down or off. The Power-Down Register allows the host to manage the AMC7812B power dissipation. When not required, the ADC, the reference buffer amplifier, and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply. The bits in the Power-Down Register control this power-down function. Set the respective bit to '1' to activate the corresponding function.

| MSB BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | PADC | PREF | PDAC 0 | PDAC 1 | PDAC 2 | PDAC 3 | PDAC 4 | PDAC 5 | PDAC 6 | PDAC 7 | PDAC 8 | PDAC 9 | PDAC 10 | PDAC 11 | 0 |

**Bit 14** **PADC**

Power-down mode control bit.
0 = The ADC is inactive in low-power mode.
1 = The ADC is in normal operating mode.

**Bit 13** **PREF**

Internal reference in power-down mode control bit.
0 = The reference buffer amplifier is inactive in low-power mode.
1 = The reference buffer amplifier is powered on.

**Bits[12:1]** **PDAC*n***

DAC*n* power-down control bit.
0 = DAC*n* is inactive in low-power mode and its output buffer amplifier is in a Hi-Z state. The output pin of DAC*n* is internally switched from the buffer output to the analog ground through an internal resistor.
1 = DAC*n* is in normal operating mode.

### Device ID Register (Read-Only, Address = 6Ch, Default = 1221h)

Model and revision information.

### Software Reset Register (Read or Write, Address = 7Ch, Default = NA)

The software reset register resets all registers to the default values, except for the DAC data register, DAC latch, and DAC clear register. The software reset is similar to a hardware reset, which resets all registers including the DAC data register, DAC latch, and DAC clear register. After a software reset, make sure that the DAC data register, DAC latch, and DAC clear register are set to the desired values before the DAC is powered on.

#### *SPI Mode*

In SPI Mode, writing 6600h to this register forces the device reset.

#### *$I^2C$ Mode*

Writing to this register (with any data) forces the device to perform a software reset. Reading this register returns an undefined value that must be ignored. Note that this register is 8-bit, instead of 16-bit. Both reading from and writing to this register are single-byte operations. Writing data to the software reset register in $I^2C$ mode is described in the following steps:

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812B slave address followed by a '0' for the direction bit, indicating a write operation.
3. The AMC7812B asserts an acknowledge signal on SDA.
4. The master sends register address 7Ch.
5. The AMC7812B asserts an acknowledge signal on SDA.
6. The master sends a data byte.
7. The AMC7812B asserts an acknowledge signal on SDA.
8. The master asserts a stop condition to end the transaction.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (September 2013) to Revision A | Page |
|---|---|
| • Changed device status to Production Data | 1 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AMC7812BSPAP | ACTIVE | HTQFP | PAP | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC7812B | Samples |
| AMC7812BSPAPR | ACTIVE | HTQFP | PAP | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC7812B | Samples |
| AMC7812BSRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC7812B | Samples |
| AMC7812BSRGCT | ACTIVE | VQFN | RGC | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC7812B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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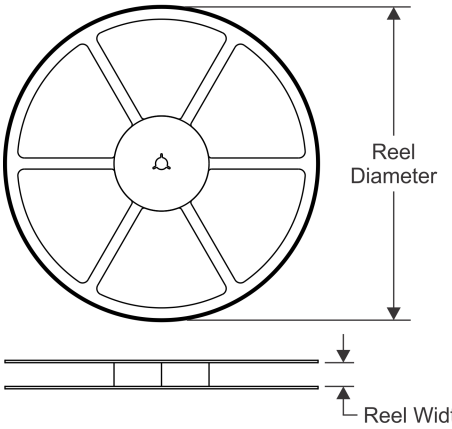
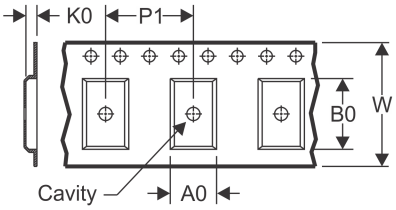
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

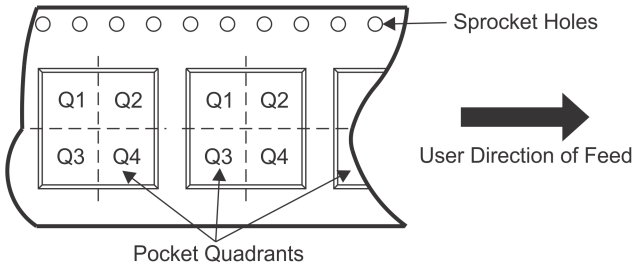



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

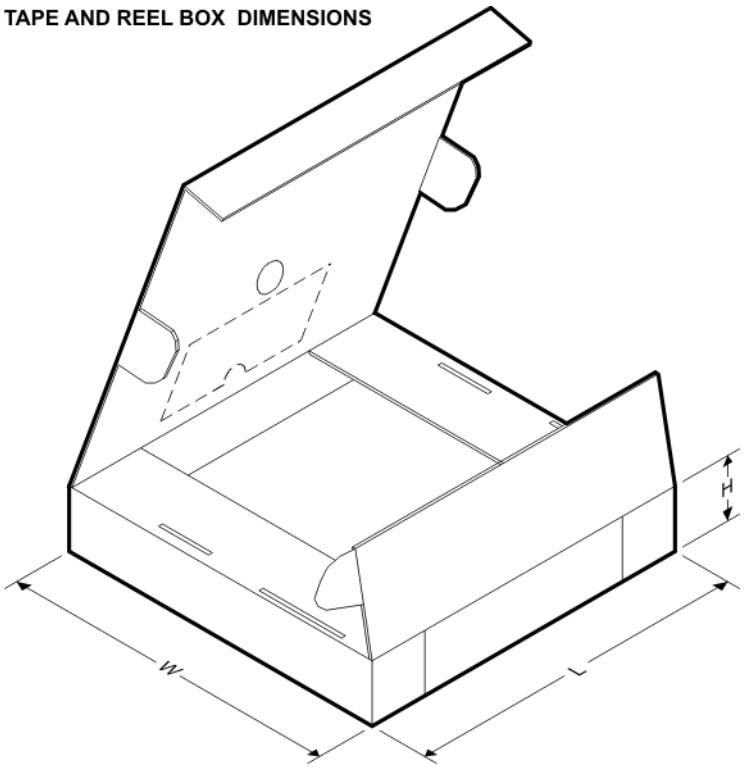
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMC7812BSPAPR | HTQFP | PAP | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |
| AMC7812BSRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| AMC7812BSRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |

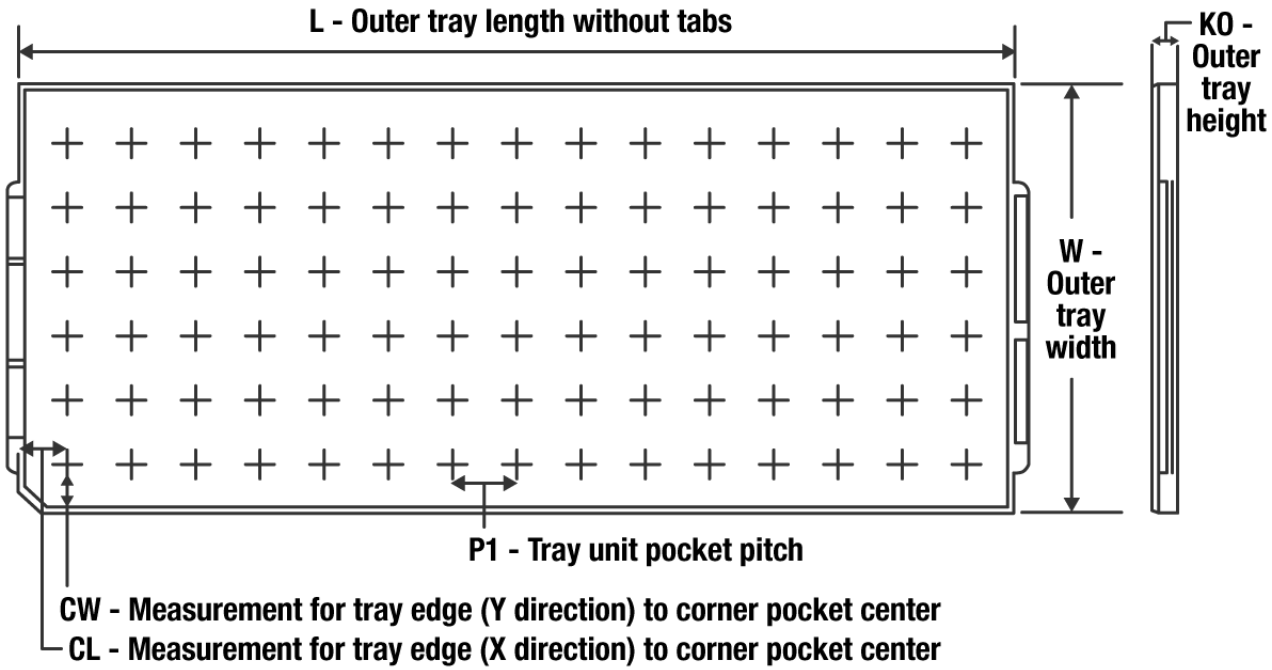
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| AMC7812BSPAPR | HTQFP | PAP | 64 | 1000 | 367.0 | 367.0 | 55.0 |
| AMC7812BSRGCR | VQFN | RGC | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| AMC7812BSRGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMC7812BSPAP | PAP | HTQFP | 64 | 160 | 8 X 20 | 150 | 322.6 | 135.9 | 7620 | 15.2 | 13.1 | 13 |

# GENERIC PACKAGE VIEW

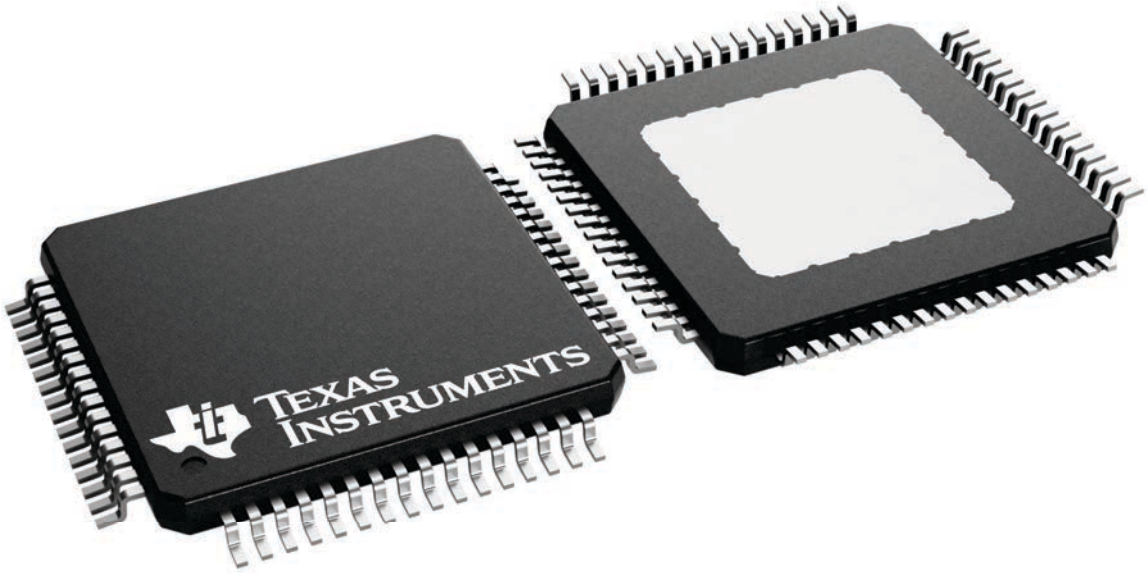
## PAP 64

## HTQFP - 1.2 mm max height

**10 x 10, 0.5 mm pitch**

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



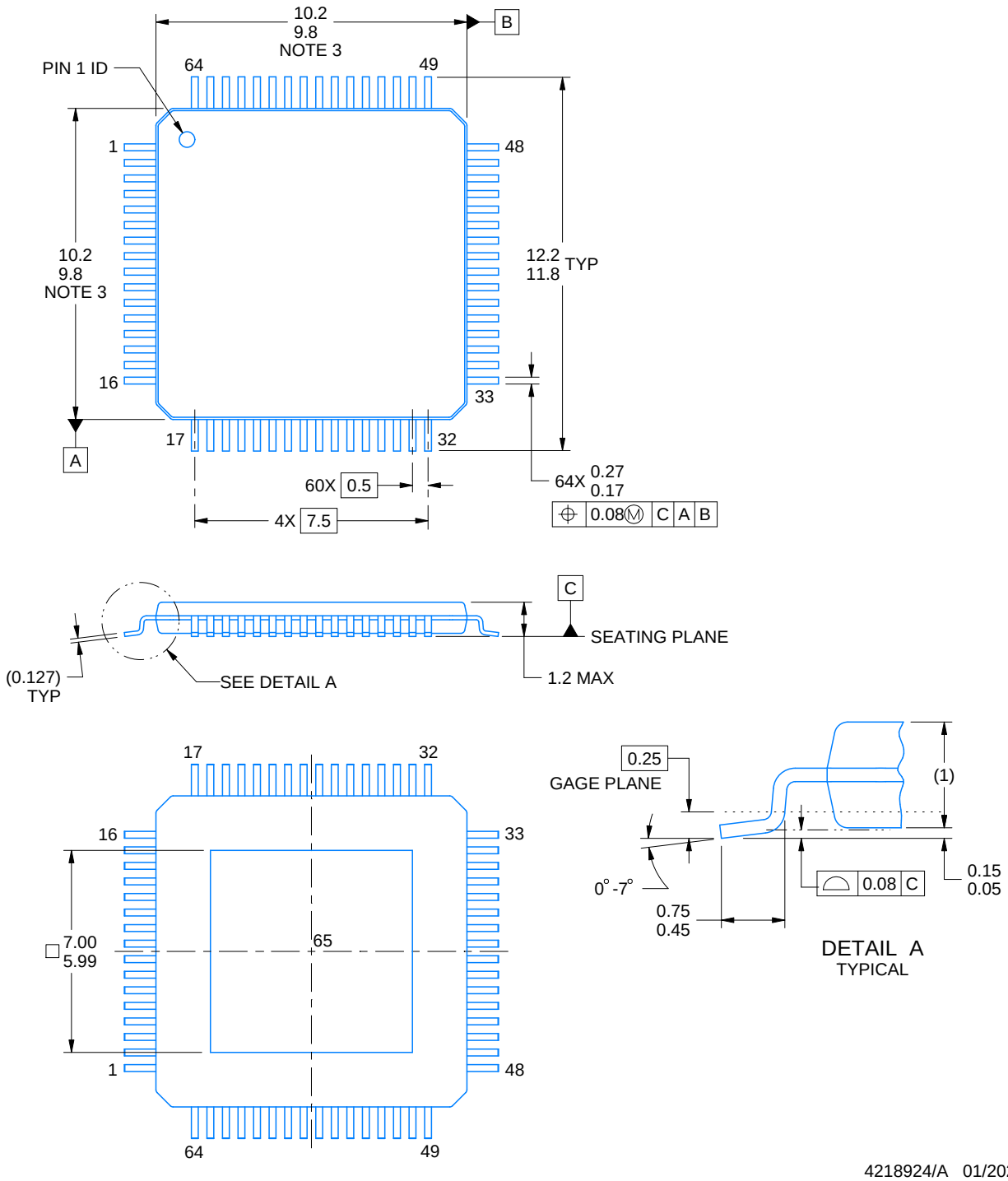

4226442/A

# PACKAGE OUTLINE

## PAP0064G

## PowerPAD™ TQFP - 1.2 mm max height

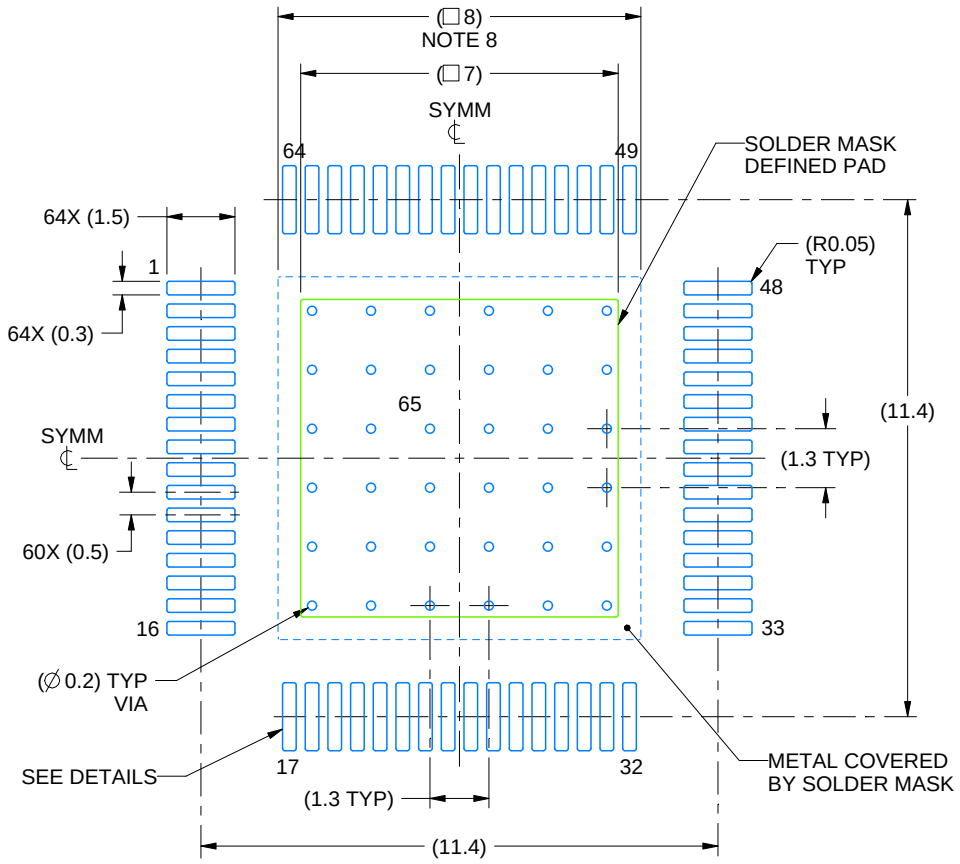
PLASTIC QUAD FLATPACK



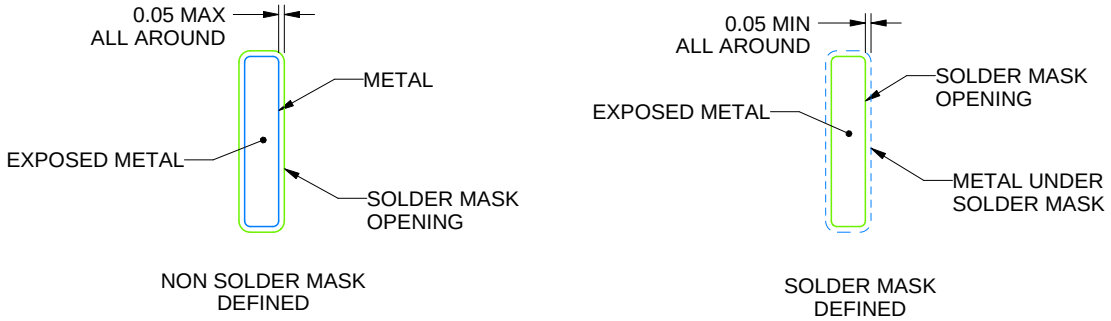

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

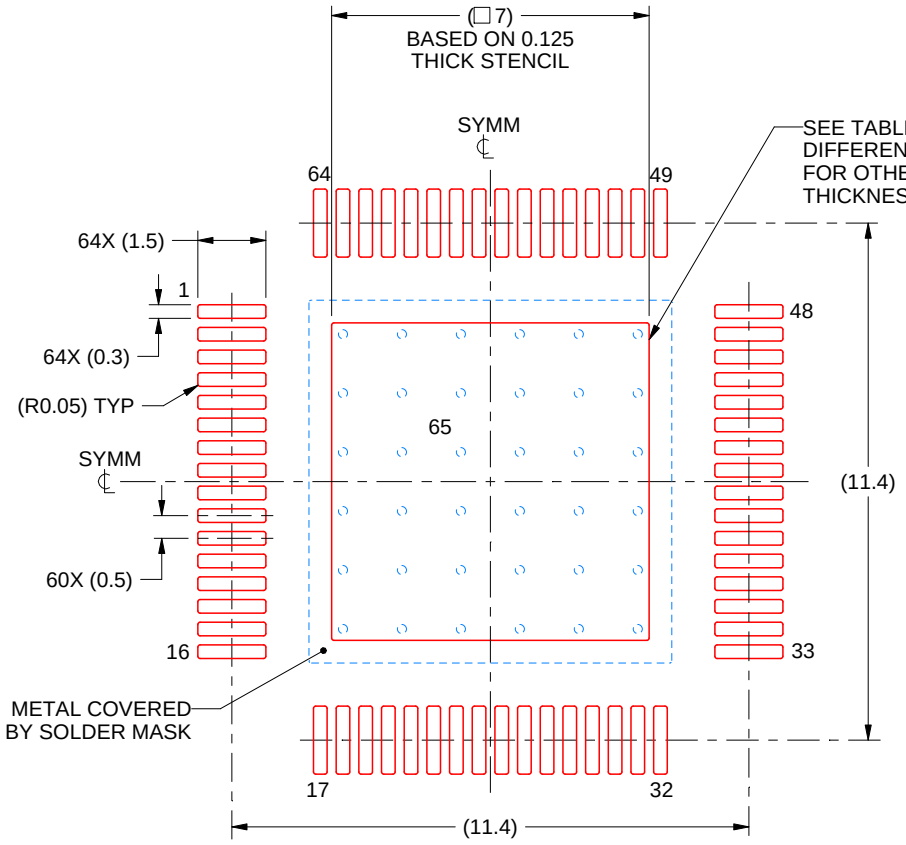



SOLDER MASK DETAILS

4218924/A 01/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 7.83 X 7.83 |
| 0.125 | 7.0 X 7.0 (SHOWN) |
| 0.15 | 6.39 X 6.39 |
| 0.175 | 5.92 X 5.92 |

4218924/A 01/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

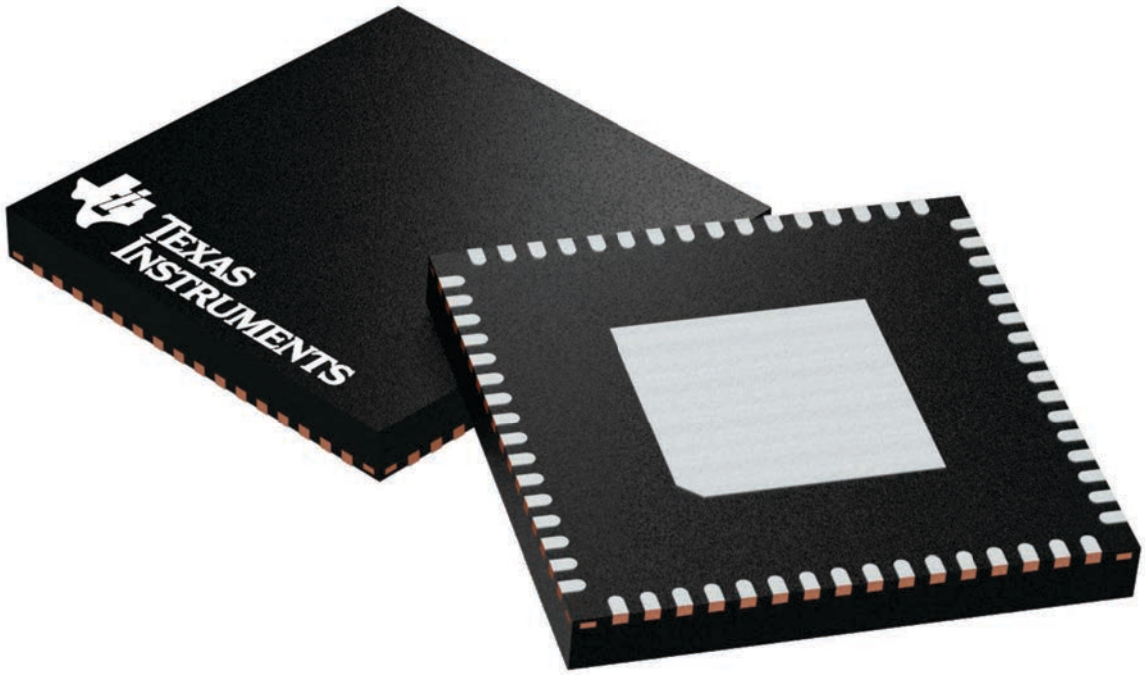
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

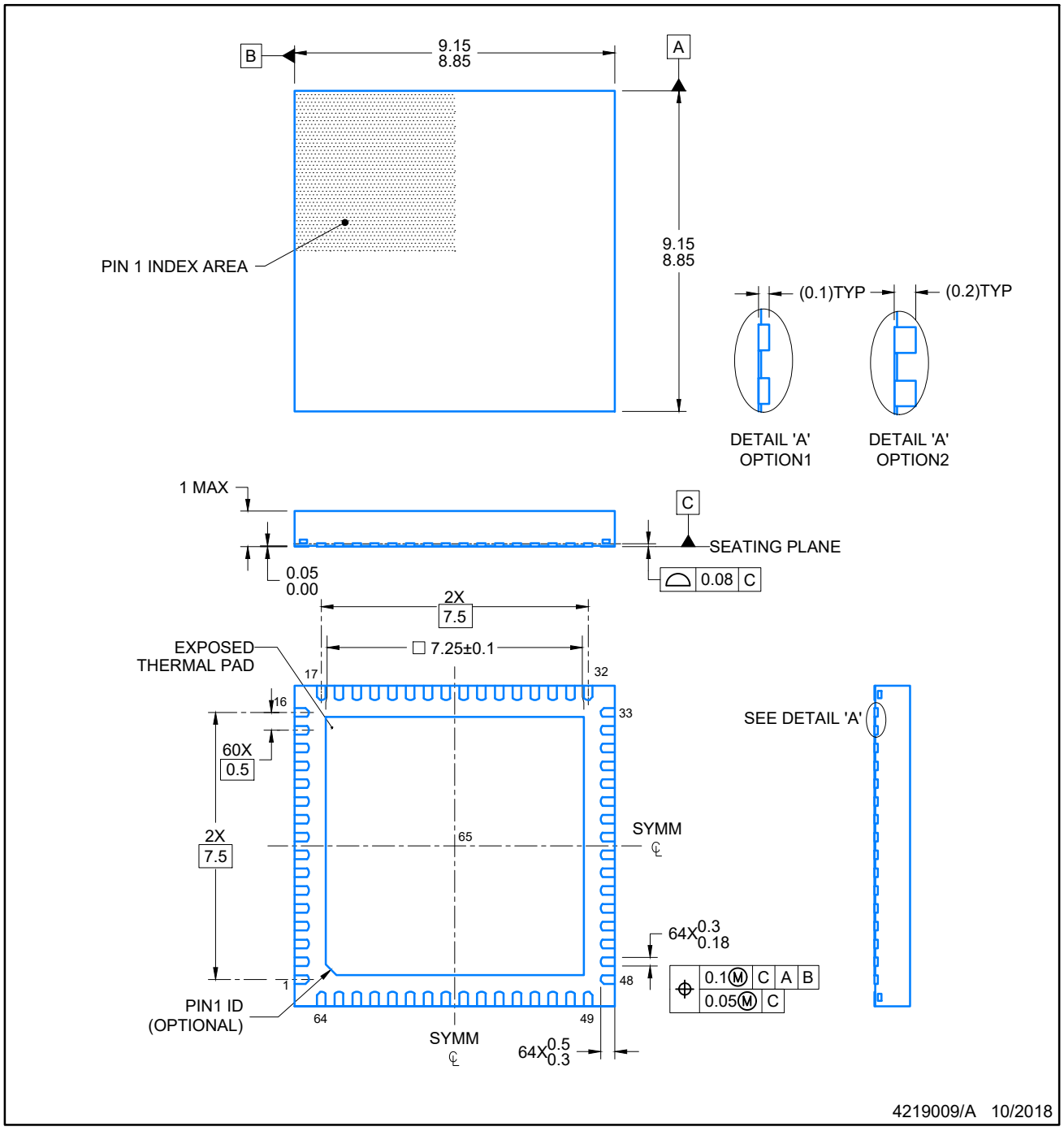
4224597/A

# PACKAGE OUTLINE

## RGC0064A

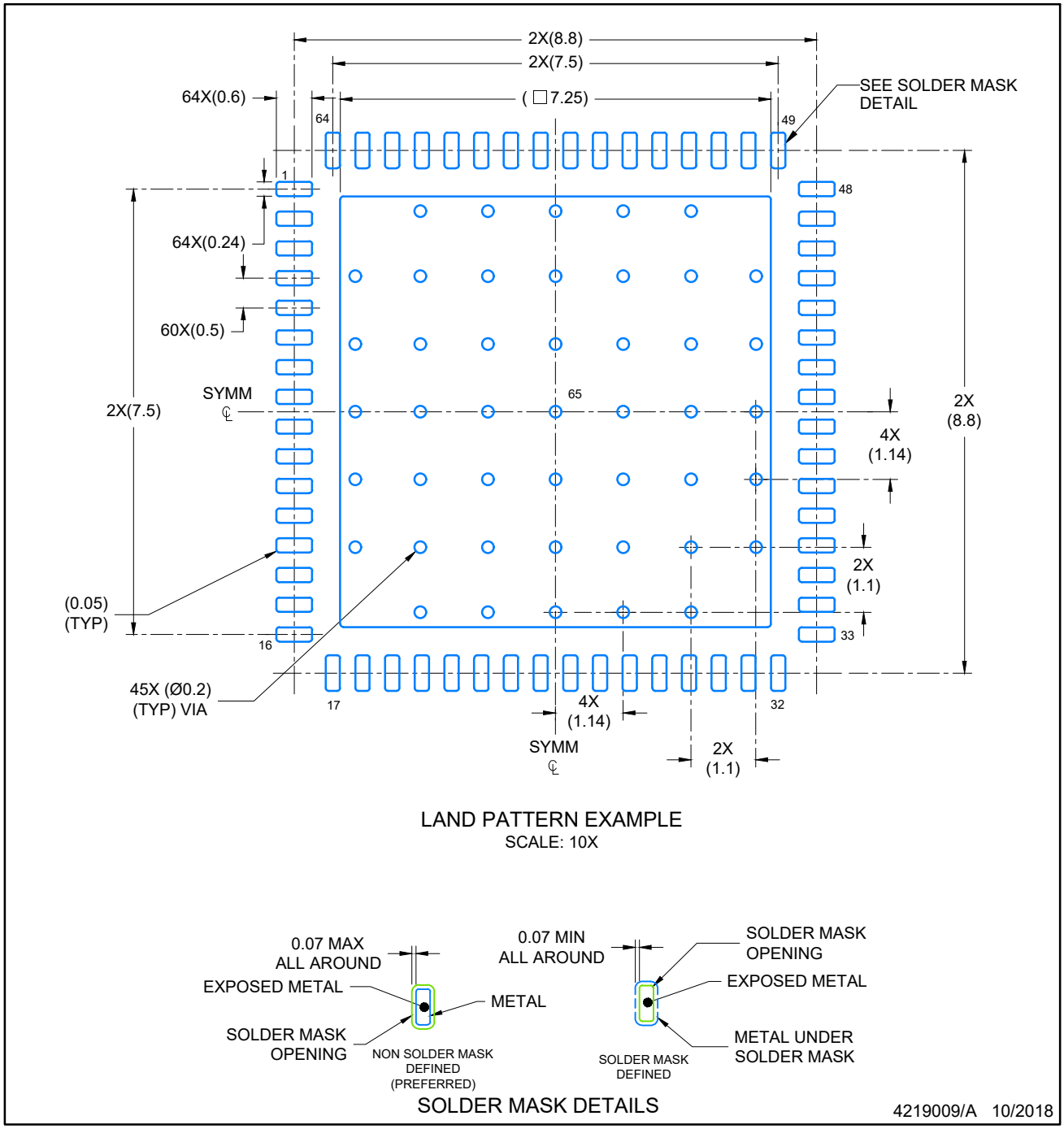
### VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



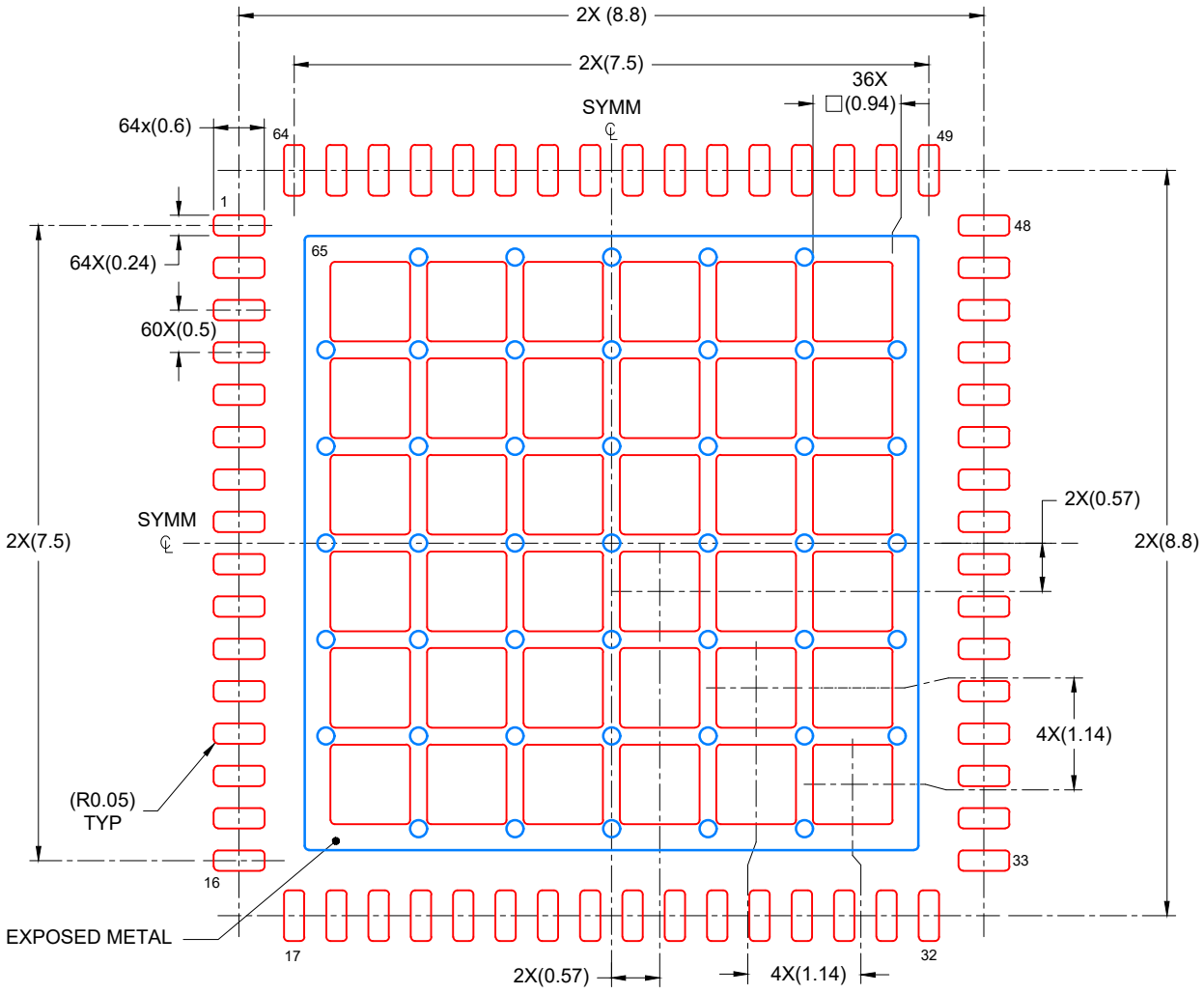

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED COVERAGE BY AREA
SCALE: 12X

4219009/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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