

## CSD17585F5 30-V N-Channel FemtoFET™ MOSFET

### 1 Features

- Low-on resistance
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Ultra-small footprint
  - 1.53 mm × 0.77 mm
- Low profile
  - 0.36-mm height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

### 2 Applications

- Optimized for industrial load switch applications
- Optimized for general purpose switching applications

### 3 Description

This 30-V, 22-mΩ, N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a significant reduction in footprint size.

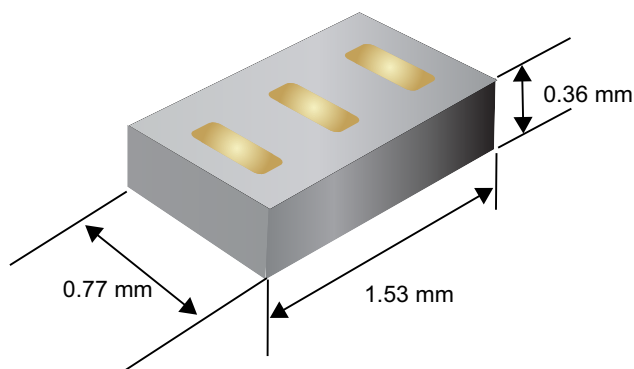


Figure 3-1. Typical Part Dimensions

### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$Q_g$	Gate Charge Total (4.5 V)	1.9	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	0.39	nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 4.5\text{ V}$	26
		$V_{GS} = 10\text{ V}$	22
$V_{GS(th)}$	Threshold Voltage	1.3	V

### Device Information

DEVICE <sup>(1)</sup>	QTY	MEDIA	PACKAGE	SHIP
CSD17585F5	3000	7-Inch Reel	Femto	Tape and Reel
CSD17585F5T	250		1.53-mm × 0.77-mm SMD Lead Less	

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	+20	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	3.6	A
	Continuous Drain Current <sup>(2)</sup>	5.9	
$I_{DM}$	Pulsed Drain Current <sup>(1) (3)</sup>	34	A
$P_D$	Power Dissipation <sup>(1)</sup>	0.5	W
	Power Dissipation <sup>(2)</sup>	1.4	
$V_{(ESD)}$	Human-Body Model (HBM)	4	kV
	Charged-Device Model (CDM)	2	
$T_J, T_{stg}$	Operating Junction, Storage Temperature	-55 to 150	$^\circ\text{C}$

- (1) Min Cu, typical  $R_{\theta JA} = 245^\circ\text{C/W}$ .  
 (2) Max Cu, typical  $R_{\theta JA} = 90^\circ\text{C/W}$ .  
 (3) Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

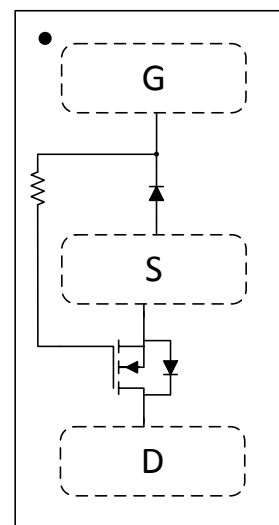


Figure 3-2. Top View



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>6 Device and Documentation Support</b> .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	6.1 Receiving Notification of Documentation Updates.....	7
<b>3 Description</b> .....	<b>1</b>	6.2 Trademarks.....	7
<b>4 Revision History</b> .....	<b>2</b>	<b>7 Mechanical, Packaging, and Orderable Information</b> ....	<b>8</b>
<b>5 Specifications</b> .....	<b>3</b>	7.1 Mechanical Dimensions.....	8
5.1 Electrical Characteristics.....	3	7.2 Recommended Minimum PCB Layout.....	9
5.2 Thermal Information.....	3	7.3 Recommended Stencil Pattern.....	9
5.3 Typical MOSFET Characteristics.....	4		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (February 2022) to Revision C (June 2022)</b>	<b>Page</b>
• Restored front page key graphic to match SLPS610A.....	1
• Restored layout of images to match SLPS610A.....	4

<b>Changes from Revision A (December 2016) to Revision B (February 2022)</b>	<b>Page</b>
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	8
• Added FemtoFET Surface Mount Guide note.....	9

<b>Changes from Revision * (October 2016) to Revision A (December 2016)</b>	<b>Page</b>
• Changed <a href="#">Figure 5-2</a> in the <i>Typical MOSFET Characteristics</i> section.....	4
• Added <a href="#">Table 7-1</a> in the <i>Mechanical Dimensions</i> section.....	8

## 5 Specifications

### 5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	30			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			100	nA
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			50	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.9	1.3	1.7	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 4.5\text{ V}, I_{DS} = 0.9\text{ A}$		26	33	m $\Omega$
		$V_{GS} = 10\text{ V}, I_{DS} = 0.9\text{ A}$		22	27	
$g_{fs}$	Transconductance	$V_{DS} = 3\text{ V}, I_{DS} = 0.9\text{ A}$		7		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V},$ $f = 1\text{ MHz}$		292	380	pF
$C_{oss}$	Output capacitance			166	215	pF
$C_{rss}$	Reverse transfer capacitance			5.7	7.4	pF
$R_G$	Series gate resistance			34		$\Omega$
$Q_g$	Gate charge total (4.5 V)	$V_{DS} = 15\text{ V}, I_{DS} = 0.9\text{ A}$		1.9	2.4	nC
$Q_g$	Gate charge total (10 V)			3.9	5.1	nC
$Q_{gd}$	Gate charge gate-to-drain			0.39		nC
$Q_{gs}$	Gate charge gate-to-source			0.53		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			0.42		nC
$Q_{oss}$	Output charge		$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		4.1	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{DS} = 0.9\text{ A}, R_G = 2\ \Omega$		4		ns
$t_r$	Rise time			4		ns
$t_{d(off)}$	Turnoff delay time			31		ns
$t_f$	Fall time			11		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 0.9\text{ A}, V_{GS} = 0\text{ V}$		0.74	1.0	V

### 5.2 Thermal Information

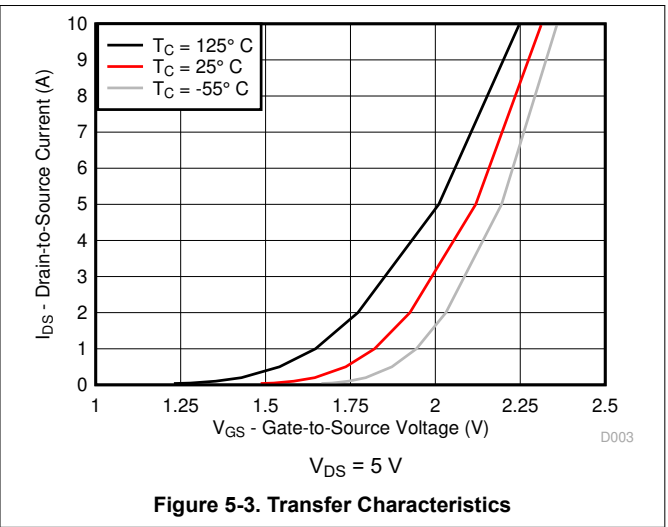
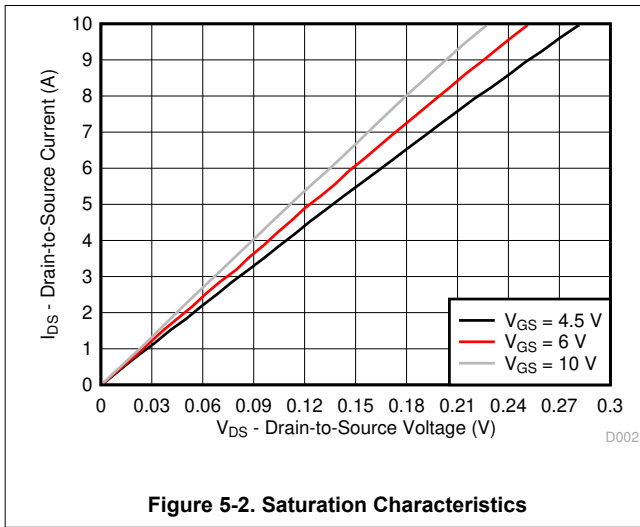
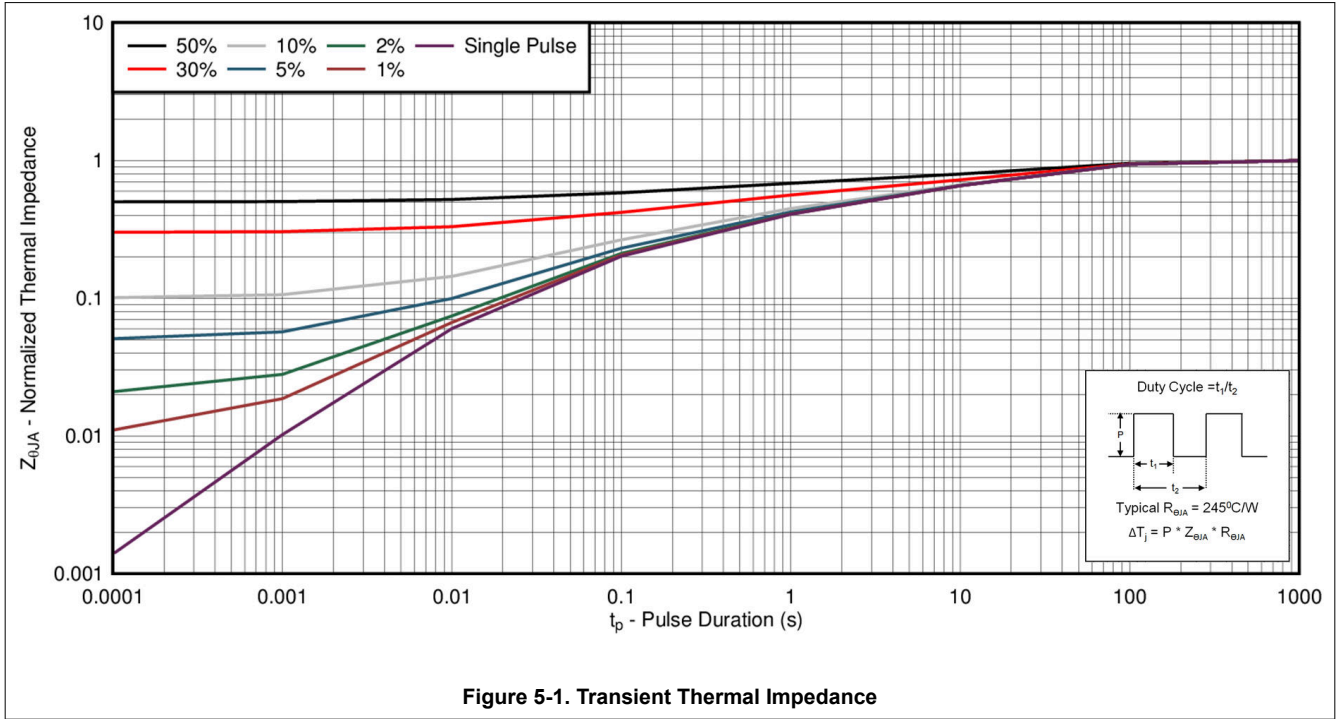
$T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>		90		$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance <sup>(2)</sup>		245		

- (1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.  
(2) Device mounted on FR4 material with minimum Cu mounting area.

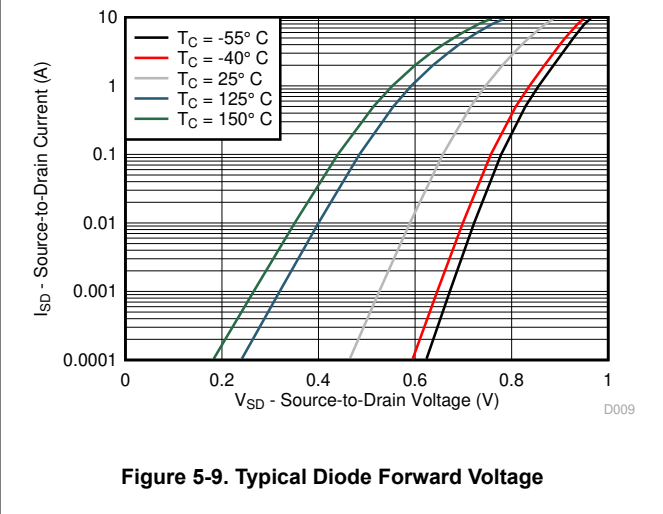
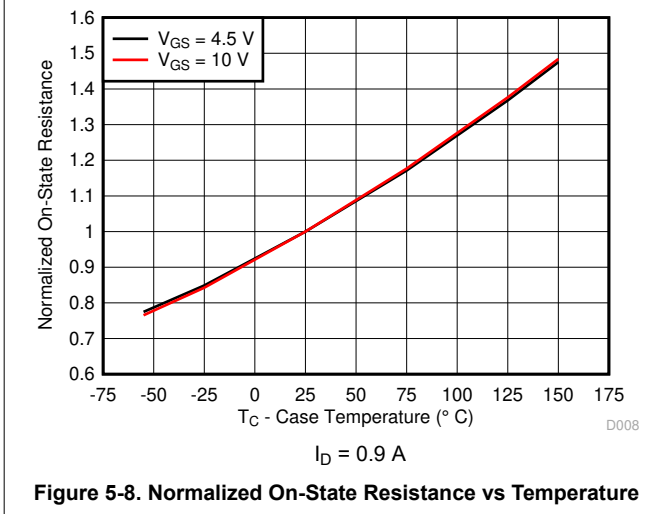
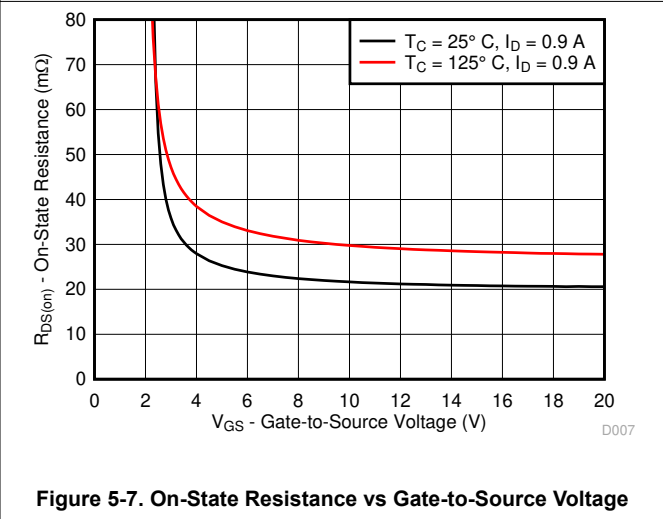
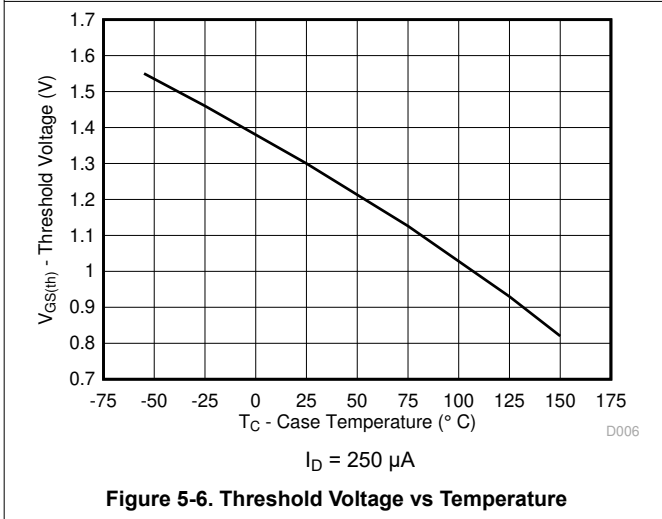
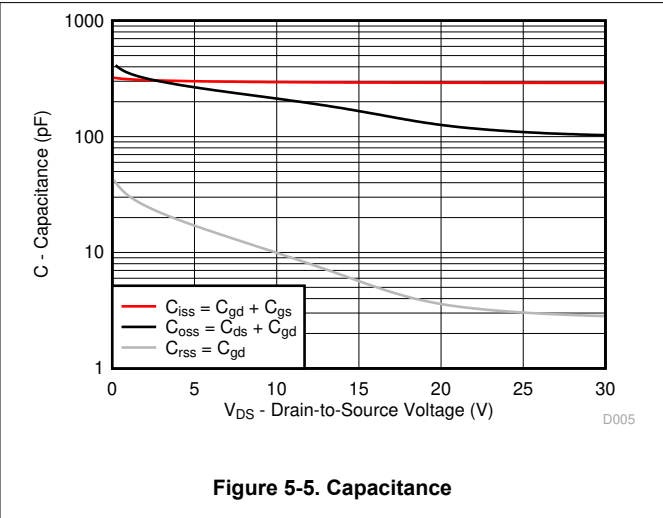
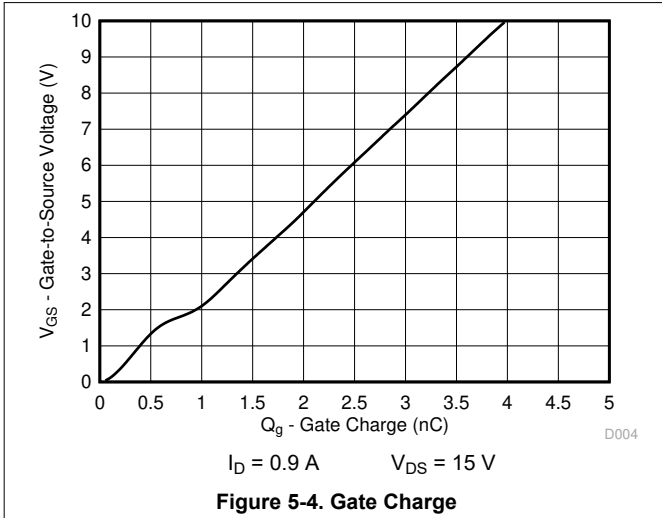
### 5.3 Typical MOSFET Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)



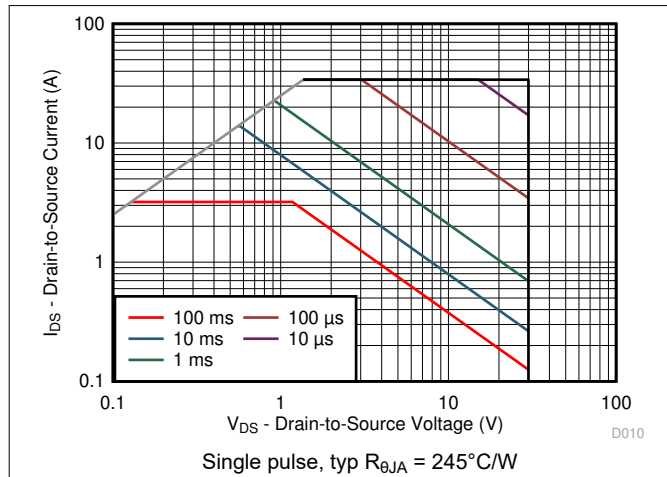
### 5.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

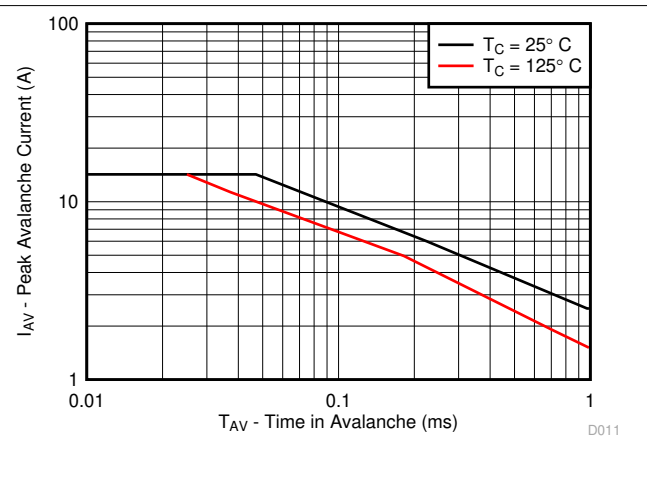


### 5.3 Typical MOSFET Characteristics (continued)

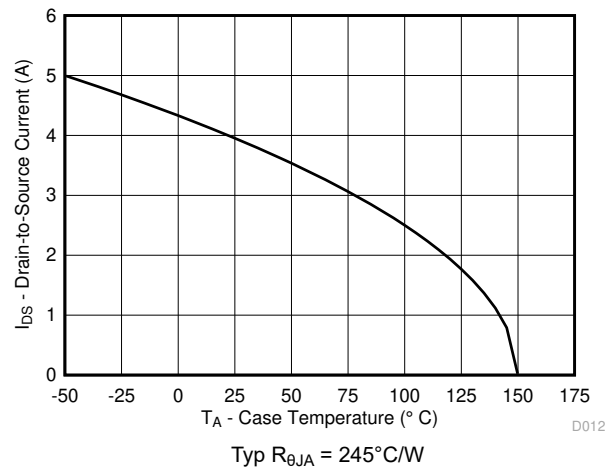
$T_A = 25^\circ\text{C}$  (unless otherwise stated)



**Figure 5-10. Maximum Safe Operating Area (SOA)**



**Figure 5-11. Single Pulse Unclamped Inductive Switching**



**Figure 5-12. Maximum Drain Current vs Temperature**

## **6 Device and Documentation Support**

### **6.1 Receiving Notification of Documentation Updates**

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

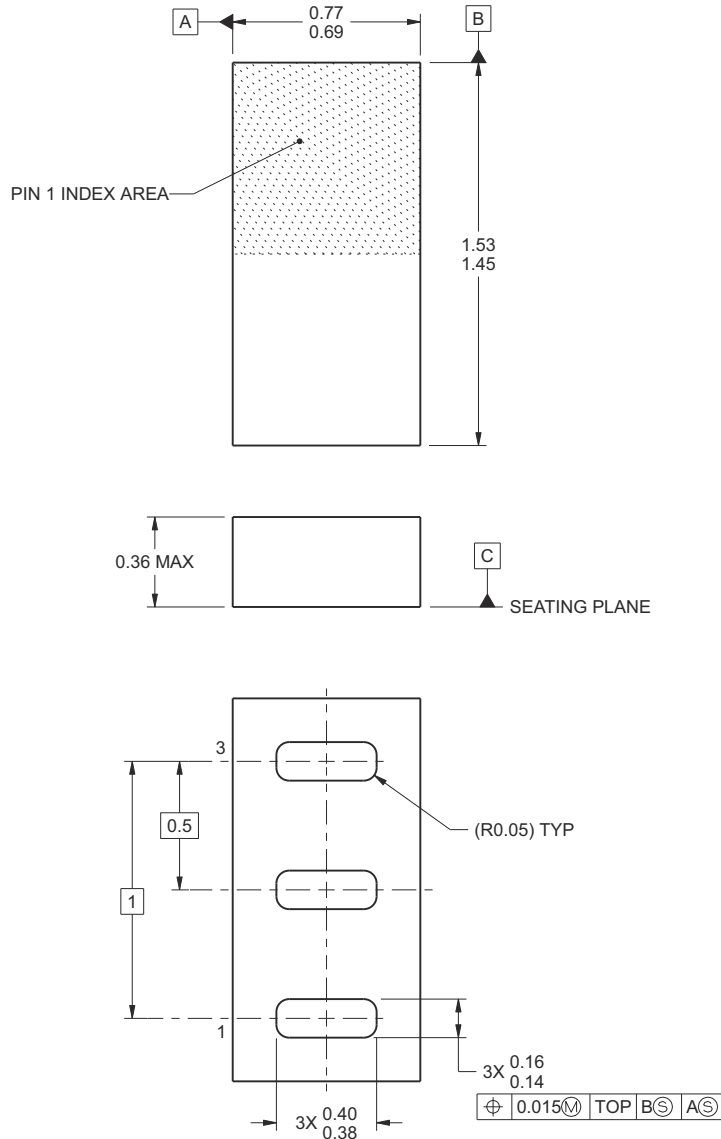
### **6.2 Trademarks**

FemtoFET™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions



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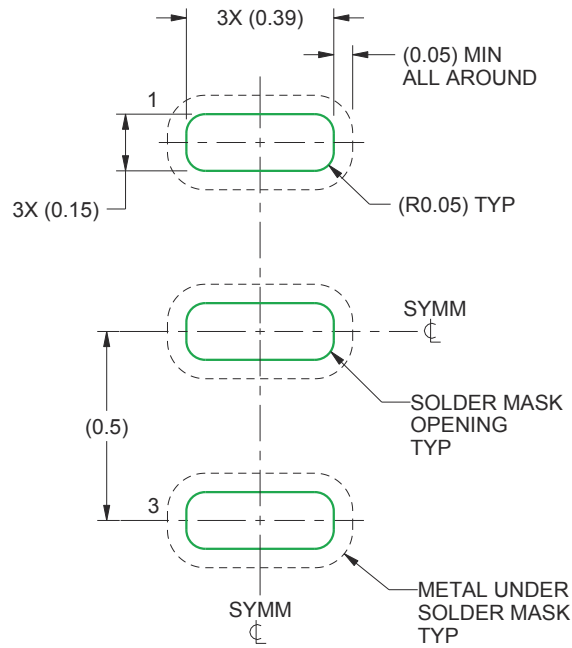
- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

**Table 7-1. Pin Configuration**

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

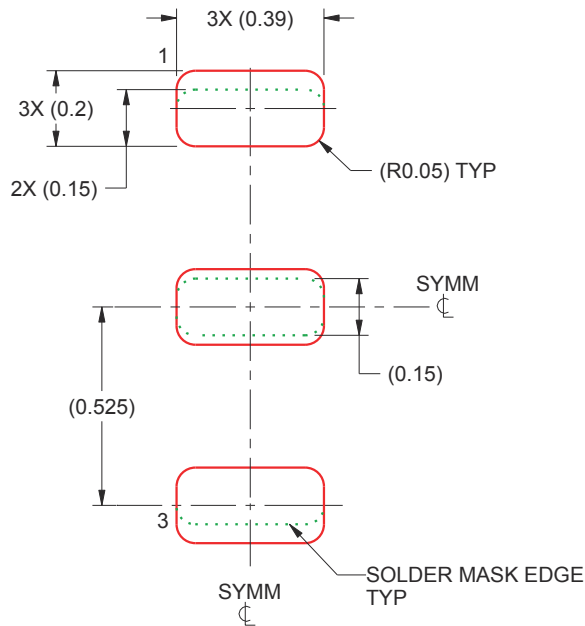


## 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17585F5	ACTIVE	PICOSTAR	YJK	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4U	<a href="#">Samples</a>
CSD17585F5T	ACTIVE	PICOSTAR	YJK	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17585F5	PICOST AR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD17585F5	PICOST AR	YJK	3	3000	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD17585F5T	PICOST AR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD17585F5T	PICOST AR	YJK	3	250	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17585F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD17585F5	PICOSTAR	YJK	3	3000	220.0	220.0	35.0
CSD17585F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0
CSD17585F5T	PICOSTAR	YJK	3	250	220.0	220.0	35.0

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