CSD18510KTT 40-V N-Channel NexFET™ Power MOSFET

1 Features

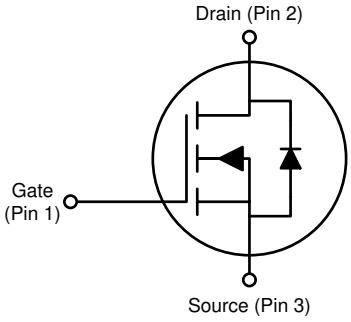
- Ultra-low Q_g and Q_{gd}
- Low-thermal resistance
- Avalanche rated
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- D^2PAK plastic package

2 Applications

- Secondary side synchronous rectifier
- Motor control

3 Description

This 40-V, 1.4-mΩ, D^2PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	40		V
Q_g	Gate Charge Total (10 V)	119		nC
Q_{gd}	Gate Charge Gate-to-Drain	21		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	2.0	mΩ
		V_{GS} = 10 V	1.4	
$V_{GS(th)}$	Threshold Voltage	1.7		V

Device Information(1)

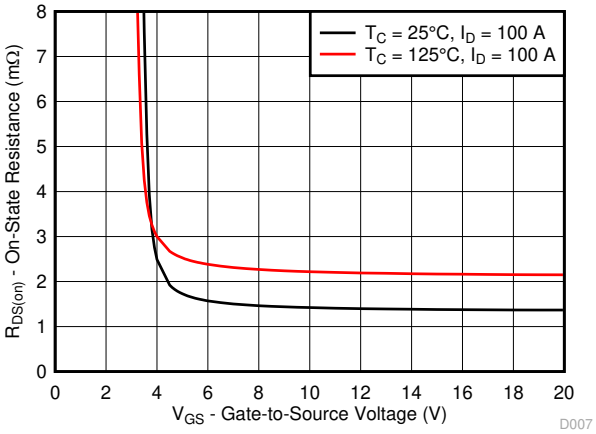
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18510KTT	500	13-Inch Reel	D^2PAK Plastic Package	Tape and Reel
CSD18510KTTT	50			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

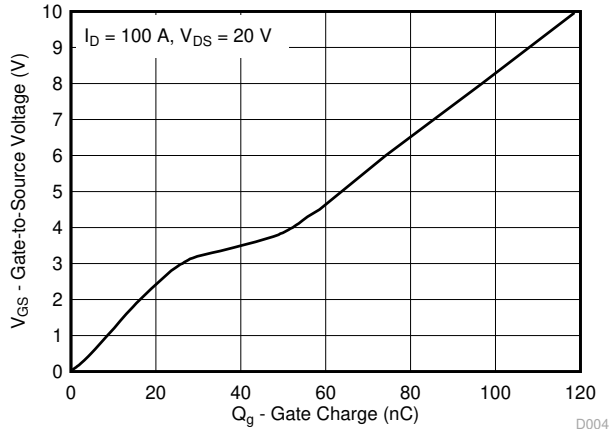
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	200	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	274	
	Continuous Drain Current (Silicon Limited), T_C = 100°C	193	
I_{DM}	Pulsed Drain Current(1)	400	A
P_D	Power Dissipation	250	W
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 175	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 81 A, L = 0.1 mH, R_G = 25 Ω	328	mJ

(1) Max $R_{\theta JC}$ = 0.6°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2017) to Revision B (November 2022)	Page
• Updated Figure 5-3	4

Changes from Revision * (November 2016) to Revision A (January 2017)	Page
• Changed silicon current limit, T_C = 25°C from 237 A : to 274 A in the *Absolute Maximum Ratings* table	1
• Changed silicon current limit, T_C = 100°C from 167 A : to 193 A in the *Absolute Maximum Ratings* table	1
• Changed max power dissipation from 188 W : to 250 W in the *Absolute Maximum Ratings* table	1
• Changed the charge values in the Dynamic Characteristics section of the *Electrical Characteristics* table	3
• Changed max $R_{\theta JC}$ from 0.8°C/W : to 0.6°C/W in the *Thermal Information* table	3
• Changed Figure 5-4 in the *Typical MOSFET Characteristics* section to reflect updated gate charges	4

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 32 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.4	1.7	2.3	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 4.5 V, I_D = 100 A		2.0	2.6	mΩ
		V_{GS} = 10 V, I_D = 100 A		1.4	1.7	
g_{fs}	Transconductance	V_{DS} = 4 V, I_D = 100 A		330		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz		8770	11400	pF
C_{oss}	Output capacitance			832	1080	pF
C_{rss}	Reverse transfer capacitance			424	551	pF
R_G	Series gate resistance			0.9	1.8	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 20 V, I_D = 100 A		58	75	nC
Q_g	Gate charge total (10 V)			118	153	nC
Q_{gd}	Gate charge gate-to-drain			21		nC
Q_{gs}	Gate charge gate-to-source			28		nC
$Q_{g(th)}$	Gate charge at V_{th}			15		nC
Q_{oss}	Output charge	V_{DS} = 20 V, V_{GS} = 0 V		35		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		10		ns
t_r	Rise time			8		ns
$t_{d(off)}$	Turnoff delay time			29		ns
t_f	Fall time			8		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.85	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 20 V, I_F = 100 A, di/dt = 300 A/µs		70		nC
t_{rr}	Reverse recovery time			41		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	°C/W

5.3 Typical MOSFET Characteristics

T_A =25°C (unless otherwise stated)

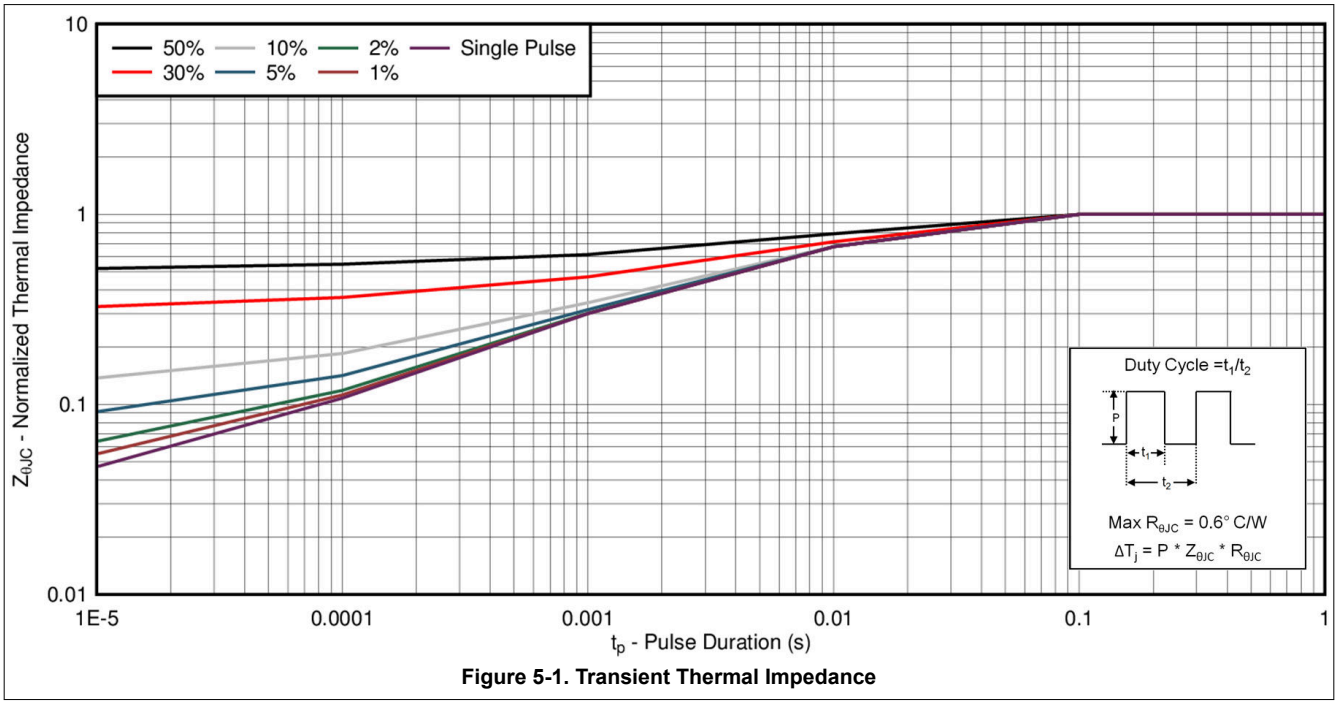


Figure 5-1. Transient Thermal Impedance

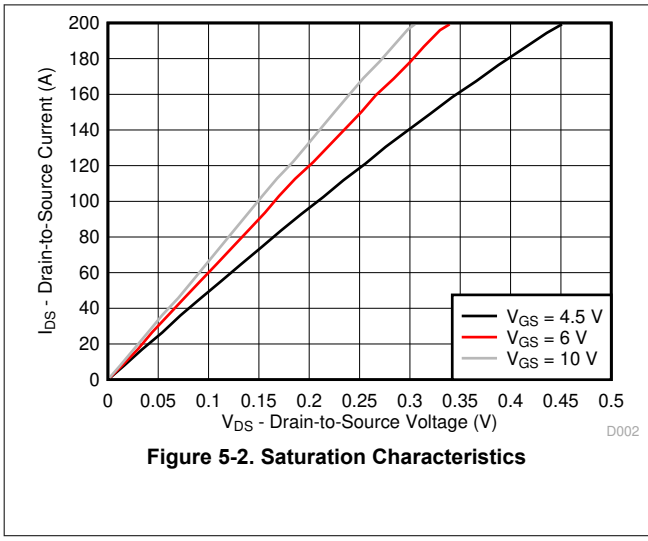
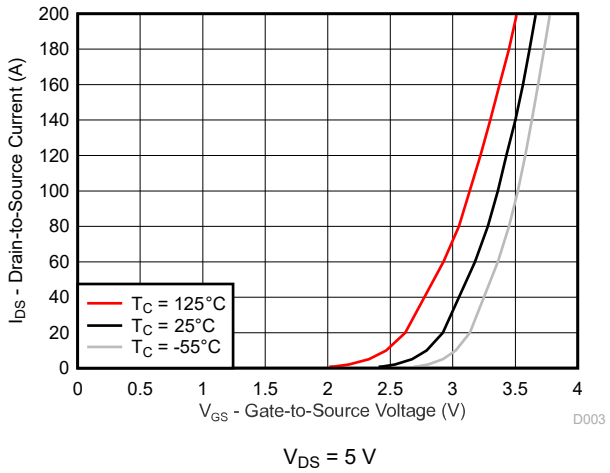


Figure 5-2. Saturation Characteristics

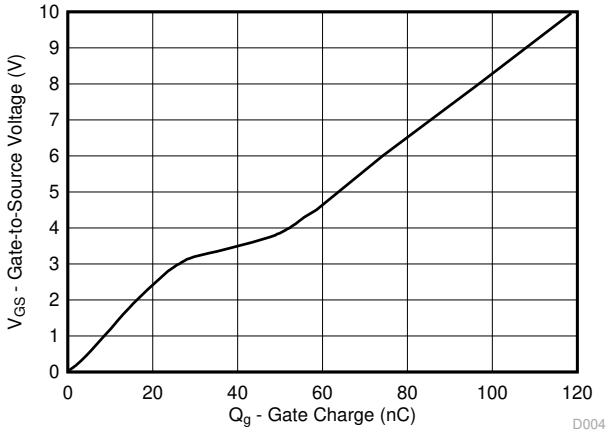


V_{DS} = 5 V

Figure 5-3. Transfer Characteristics

5.3 Typical MOSFET Characteristics (continued)

T_A =25°C (unless otherwise stated)



V_{DS} = 20 V I_D = 100 A

Figure 5-4. Gate Charge

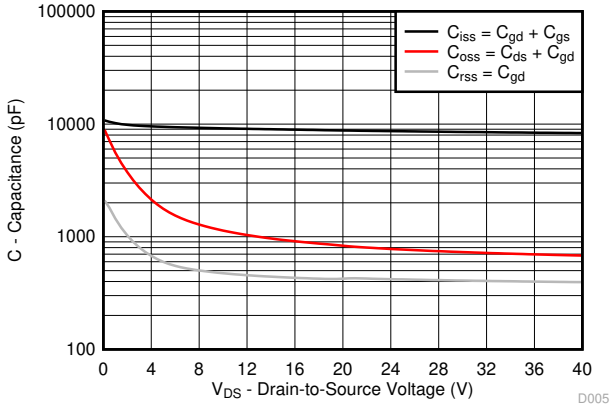
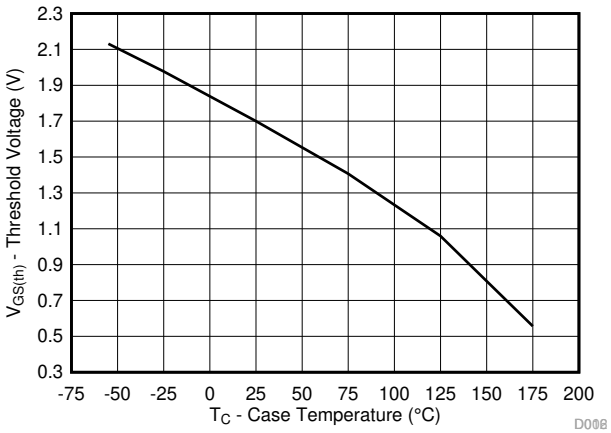


Figure 5-5. Capacitance



I_D = 250 µA

Figure 5-6. Threshold Voltage vs Temperature

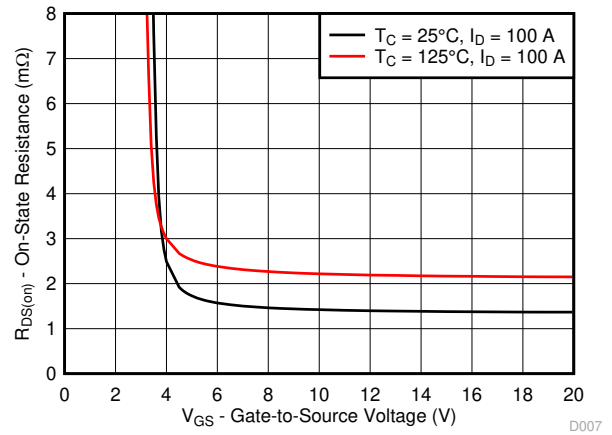
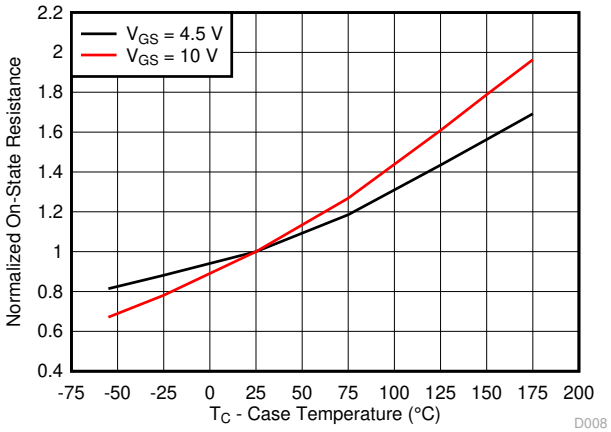


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 100 A

Figure 5-8. Normalized On-State Resistance vs Temperature

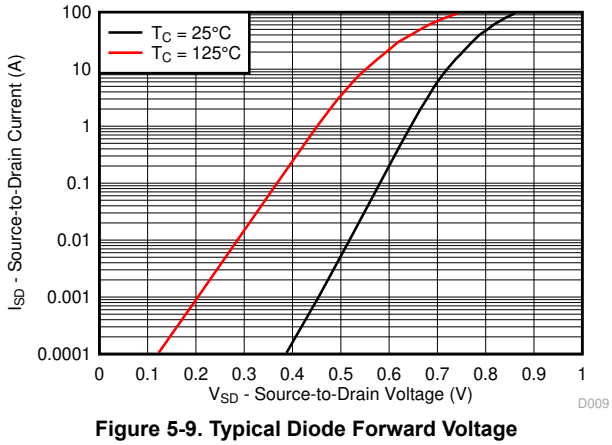
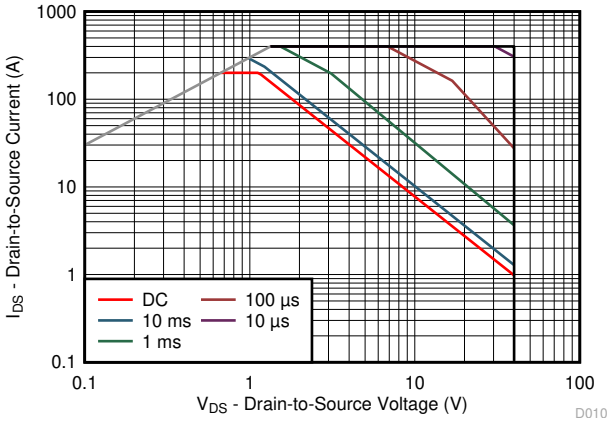


Figure 5-9. Typical Diode Forward Voltage

5.3 Typical MOSFET Characteristics (continued)

T_A =25°C (unless otherwise stated)



Single pulse, max $R_{\theta JC}$ = 0.6°C/W

Figure 5-10. Maximum Safe Operating Area

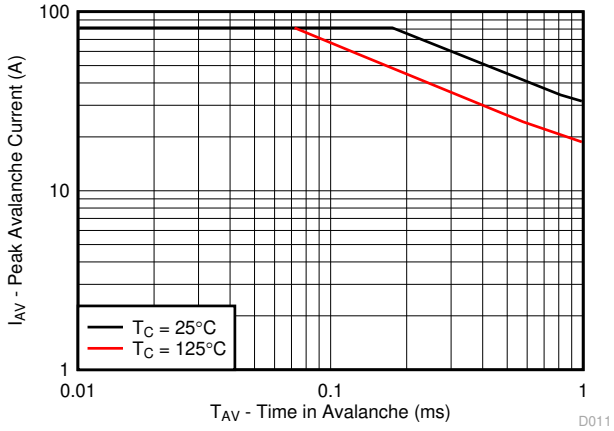
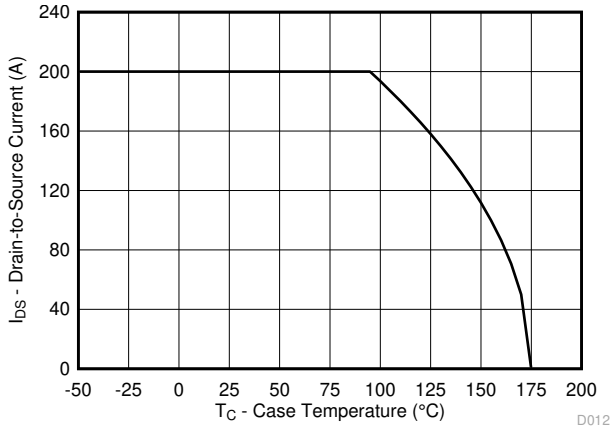


Figure 5-11. Single Pulse Unclamped Inductive Switching



Max $R_{\theta JC}$ = 0.6°C/W

Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.3 Trademarks

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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

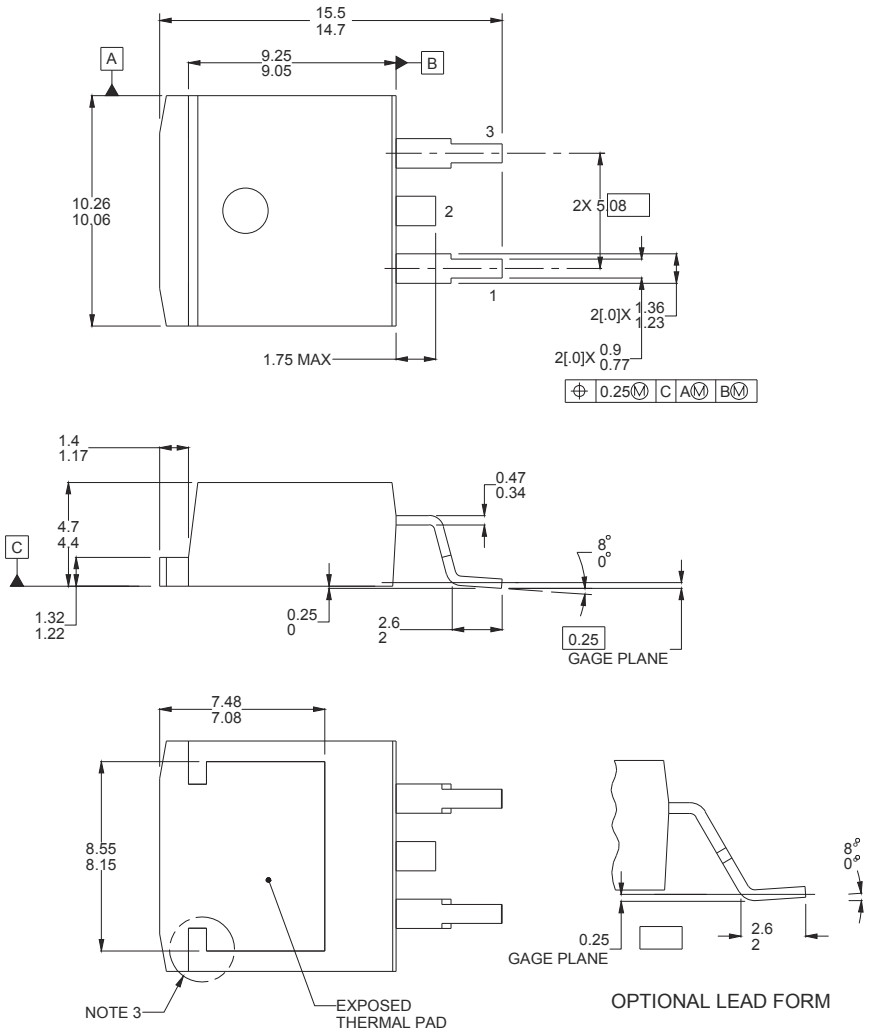
6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KTT Package Dimensions



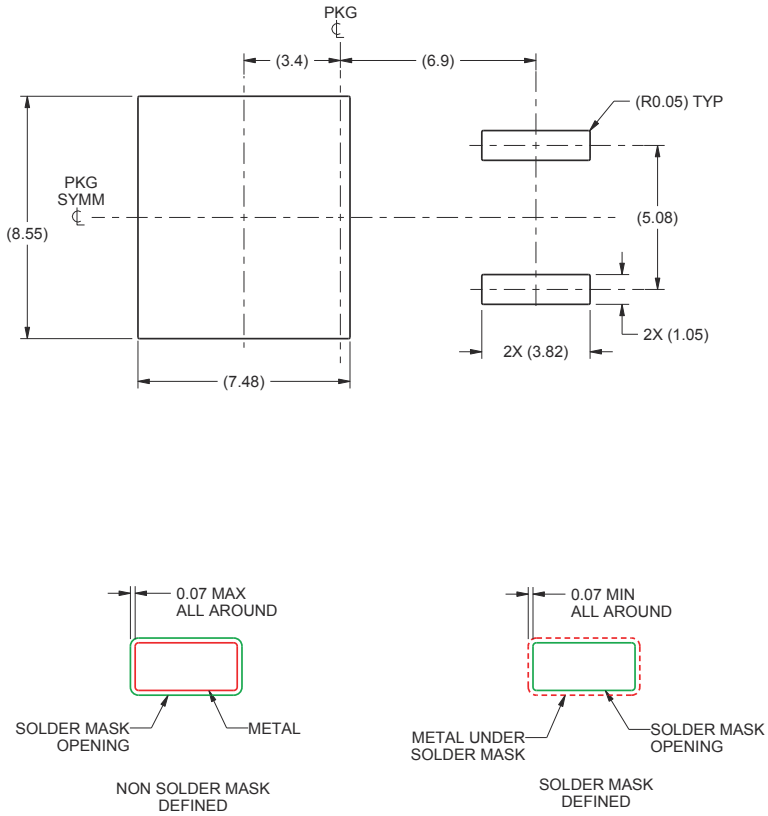
Notes:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.

Table 7-1. Pin Configuration

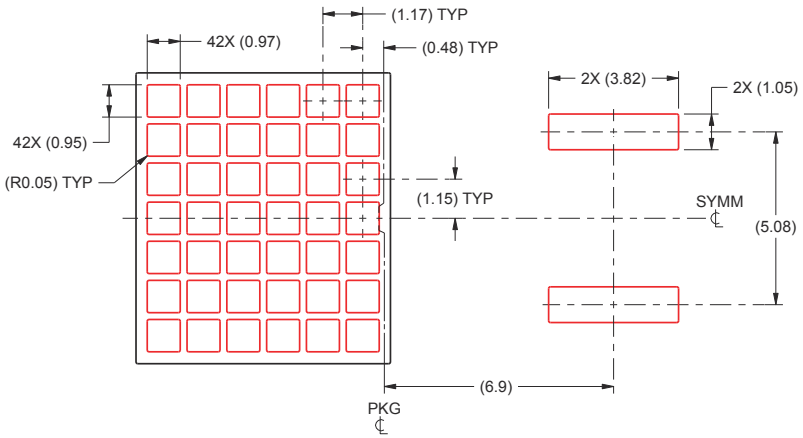
POSITION	DESIGNATION
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

7.2 Recommended PCB Pattern



For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Opening (0.125 mm Stencil Thickness)



Notes:

1. This package is designed to be soldered to a thermal pad on the board. See *PowerPAD™ Thermally Enhanced Package* (SLMA002) and *PowerPAD™ Made Easy* (SLMA004) for more information.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
3. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18510KTT	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18510KTT	Samples
CSD18510KTTT	ACTIVE	DDPAK/ TO-263	KTT	3	50	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18510KTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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