CSD93501-Q1 Synchronous Buck Monolothic Smart Power Stage

1 Features

- 30A TDC current, 60A peak operating current capability
- 91.2% peak system efficiency at 2MHz, 5Vin, 1Vo
- High-frequency operation (up to 2.2 MHz)
- Temperature compensated bi-directional current sense
- Analog temperature output
- 3.3-V and 5-V PWM signal compatible
- Tri-state PWM input
- Integrated bootstrap switch
- Optimized dead-time for shoot-through protection
- Fault Protection
  - Over temperature (OT)
  - Pulse-by-pulse over current limiting
  - Catatraphic Over Current Protection (OCP)
- Fault Detection
  - High-Side Short (HSS)
  - Pulse-by-pulse negative Over Current (negOC) detection
- Body Breaking (BB) mode and Diode Emulation Mode (DEM) operation
- 3.5 x 6.25 mm QFN package
- Ultra-low-inductance package
- System optimized PCB footprint
- AEC-Q100 Grade 1 qualified

2 Applications

- Multiphase synchronous buck converters
  - High-frequency applications
  - High-current, low-duty cycle applications

3 Description

CSD93501-Q1 is a highly optimized smart power stage for use in a high power, high density applications with 5V input, including automotive. This product integrates the driver IC and power MOSFETs in one silicon die to complete the power stage switching function. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. The monolithic design enables high switching frequency with high efficiency, lower noise, and high current- and temperature-sensing accuracy. This product has a small 3.5 x 6.25 mm QFN package. The PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

CSD93501-Q1 provides key differentiating features including cycle-by-cycle current limiting/protection based on high-side FET current sense, over temperature protection, negative over current detection, and open pin detection, which improve system reliability.

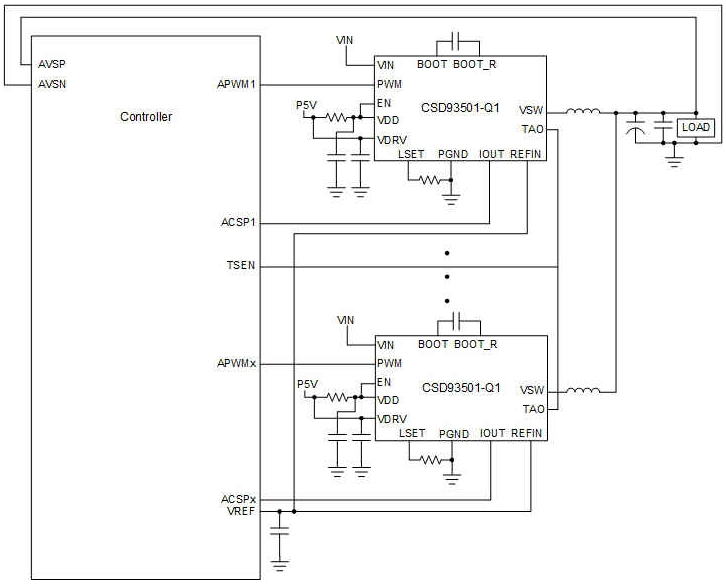
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CSD93501-Q1	WQFN	3.5 mm × 6.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Simplified Application



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4 Revision History

Changes from Revision * (October 2022) to Revision A (December 2022)	Page
• Max Peak Output Current updated to 60A (from 75A)	4
• Max Operating Junction Temperature updated to 125C (from 150C)	4

5 Pin Configuration and Functions

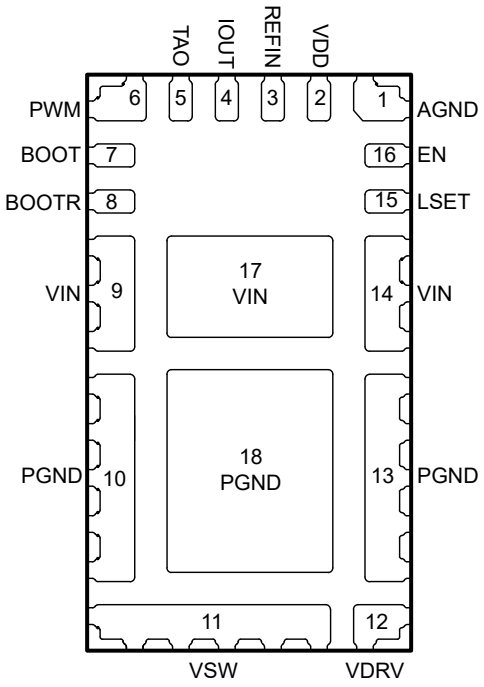

Figure 5-1. RYC Package, 18-PIn WQFN-FCRLF (Top View)

Table 5-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground.
VDD	2	Supply voltage for internal circuitry. This pin should be bypassed directly to AGND.
REFIN	3	External reference voltage input for current sensing amplifier.
IOUT	4	Output of current sensing amplifier. V(IOUT) - V(REFIN) is proportional to the phase current.
TAO/FLT	5	Temperature Amplifier Output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in multiphase applications, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3V if any one of the thermal shutdown, over current protection, or high-side short detection circuits is tripped.
PWM	6	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Either body break or DCM will be inabled if PWM stays in Hi-Z for greater than the tri-state shutdown hold-off time (t_{SHT}).
BOOT	7	Bootstrap capacitor connection. Connect a minimum 0.1 µF 10V X7R ceramic capacitor from BOOT to BOOTR pin. The bootstrap capacitor provides the charge to switch the HS FET. The bootstrap diode is integrated.
BOOTR	8	Bootstrap capacitor connectioin return path for the HS FET floating driver. Connected to VSW node internally. Connect a minimum 0.1 µF 10V X7R ceramic capacitor from BOOT to BOOTR pin. The bootstrap capacitor provides the charge to switch the HS FET. The bootstrap diode is integrated.
VIN	9, 14, 17	Input voltage ping. Connect input capacitors close to this pin.
PGND	10, 13, 18	Power ground.
VSW	11	Phase node connecting the HS FET source and LS FET drain; pin connection to the output inductor.
VDRV	12	Supply voltage for the gate drivers. This pin should be bypassed to PGND.
LSET	15	A resistor from this pin to PGND sets the inductor value for the internal current sensing circuitry.
EN	16	Enable input pin. The gate driver responds to PWM input when EN is logic high. When EN is logic low, both FET gates are actively driven off.

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6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN} to P_{GND}		-0.3	11	V
V_{IN} to V_{SW}		-0.3	11	V
V_{SW} to P_{GND}		-0.3	11	V
V_{DD} to A_{GND}		-0.3	6	V
V_{DDRV} to P_{GND}		-0.3	6	V
EN, TAO/FLT, LSET to A_{GND}		-0.3	V_{DD} + 0.3	V
IOUT, REFIN, VOS, PWM to P_{GND}		-0.3	6	V
BOOT to BOOTR(2)		-0.3	V_{DD} + 0.3	V
BOOT to P_{GND}		-0.3	17	V
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

PARAMETER			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q101-001, level H2, all pins	-2000	2000	V
		Charged device model (CDM), per AEC-Q100-011, level C4B, corner pins	-750	750	
		Charged device model (CDM), per AEC-Q100-011, level C4B, all other pins	-500	500	

6.3 Recommended Operating Conditions

T_A = 25 °C (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Driver Supply Voltage		4.5	5.5	V
V_{DRV}	Gate Drive Voltage		4.5	5.5	V
V_{IN}	Input Supply Voltage(2)		2.7	5.5	V
V_{OUT}	Output Voltage			2	V
	PWM to P_{GND}			5.5	V
I_{TDC}	Thermal Design Current	V_{IN} = 5V, V_{DD} = 5V, V_{DRV} = 5V, V_{OUT} = 1V, f_{SW} = 1000 kHz		30	A
I_{OUT-PK}	Peak Output Current			60	A
f_{SW}	Switching Frequency	C_{BST} = 0.1 µF (min) V_{IN} = 5V, V_{OUT} = 1V		2200	kHz
D_{MAX}	Max Duty Cycle	f_{SW} = 1 MHz, for transient response, not for steady state operation	90		%
	Minimum PWM On Time		20		ns

6.3 Recommended Operating Conditions (continued)

T_A = 25 °C (unless otherwise noted)(1)

			MIN	MAX	UNIT
T_J	Operating Junction Temperature		-40	125	°C

(1) Exposure to operating conditions beyond those specified in Recommended Operating Conditions may affect the long term reliability of the device.
(2) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the Absolute Maximum Ratings.

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7 Device and Documentation Support

7.1 Device Support

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7.2 Documentation Support

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7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Package Option Addendum

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4)(5)
PCSD93501QRYCTQ1	PRE_PROD	WQFN	RYC	16	500	PB-Free (RoHS Exempt)	CU NIPDAU	Level-3-260C-168 HR	–40 to 125	P501Q102

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

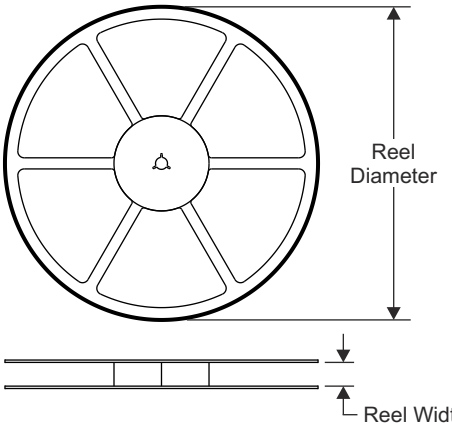
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

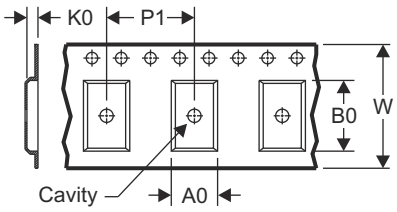
(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

8.2 Tape and Reel Information

REEL DIMENSIONS

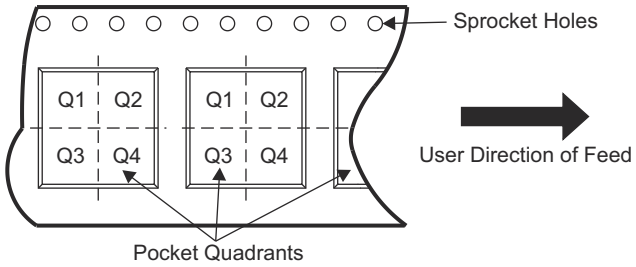


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCSD93501QRYCTQ1	WQFN	RYC	16	500	330	12.4	3.80	6.55	0.95	8.00	12.00	Q2

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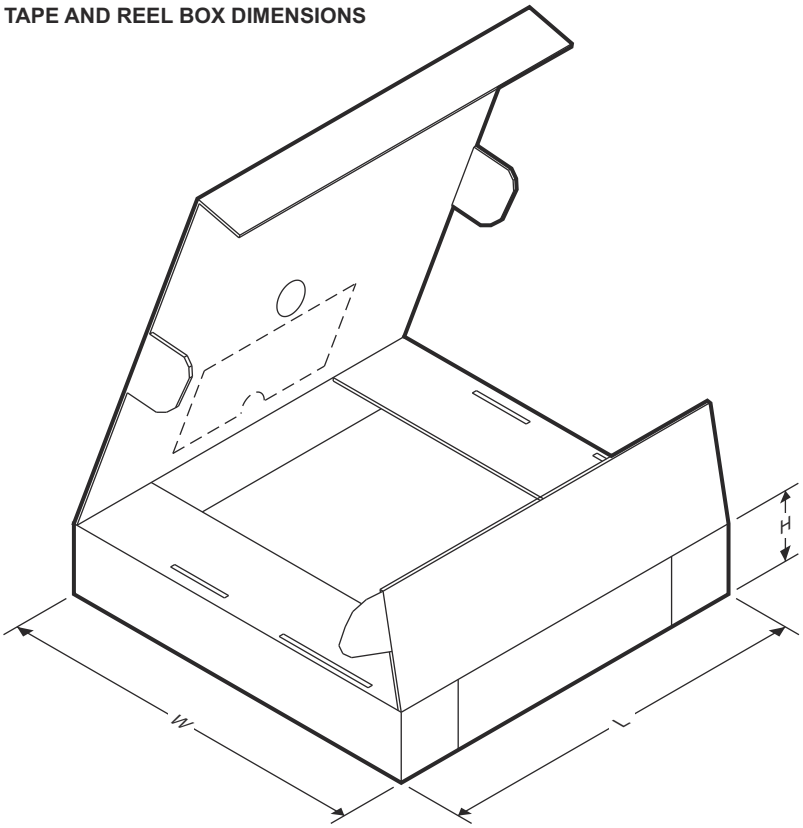
TAPE AND REEL BOX DIMENSIONS



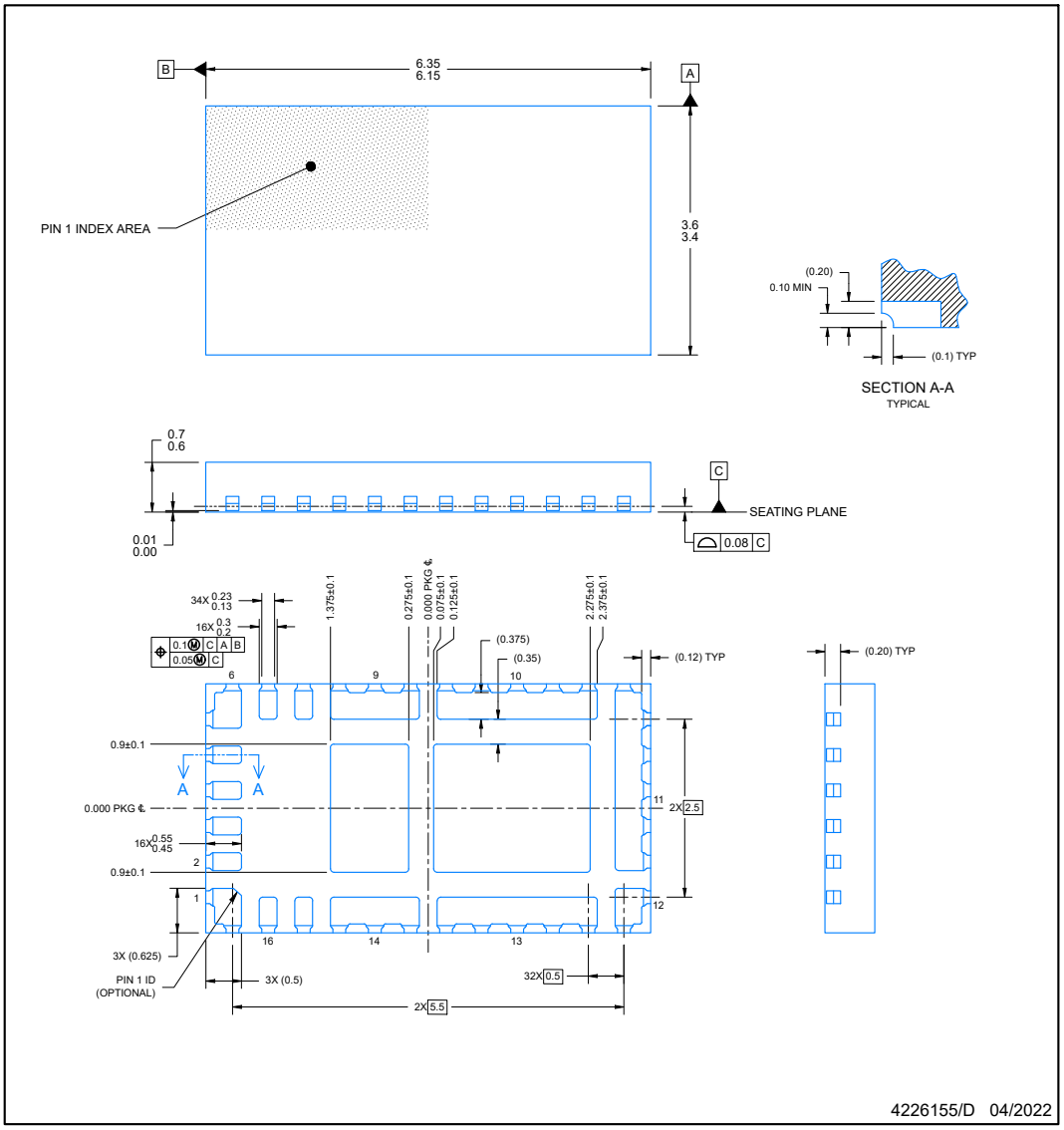
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCSD93501QRYCTQ1	WQFN	RYC	16	500	338	355	50

PACKAGE OUTLINE

RYC0016A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

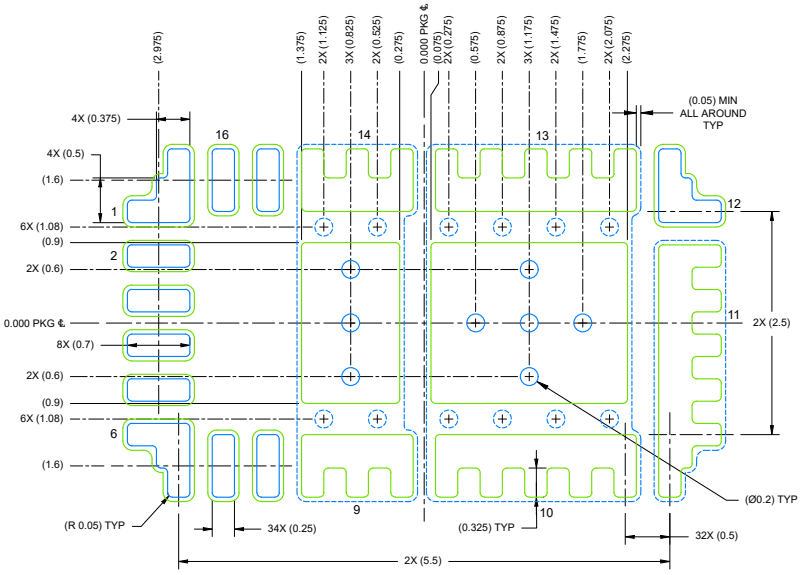
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

ADVANCE INFORMATION

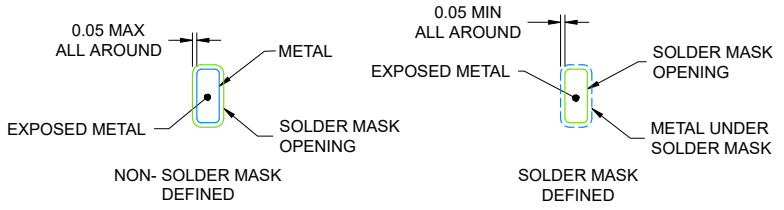
EXAMPLE BOARD LAYOUT

RYC0016A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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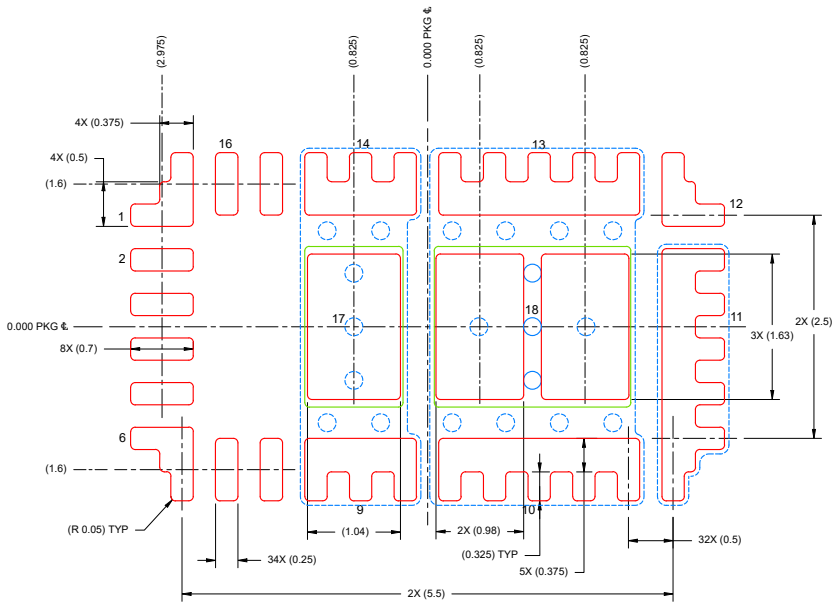
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RYC0016A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER PASTE COVERAGE:
PIN 17 : 86%
PIN 18 : 81%

SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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