SN65ALS1176 Differential Bus Transceiver

1 Features

- Meets or exceeds the requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU recommendations V.11 and X.27
- Operates at data rates up to 35 MBaud
- Operating temperature range: –25°C to 85°C
- Designed for multipoint transmission on long bus lines in noisy environments
- Low supply-current requirement: 30 mA max
- Wide positive and negative input/output bus-voltage ranges
- Thermal-shutdown protection
- Driver positive- and negative-current limiting
- Receiver input hysteresis
- Glitch-free power-up and power-down protection
- Receiver open-circuit fail-safe design
- Package options include plastic small-outline (D) package and (P) DIPs

2 Applications

- PROFIBUS

3 Description

The SN65ALS1176 differential bus transceiver is designed for bidirectional data communication on multipoint bus transmission lines. The device is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

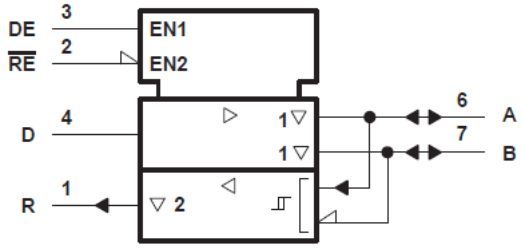
The SN65ALS1176 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device an excellent choice for party-line applications.

The SN65ALS1176 is characterized for operation from – 25°C to 85°C.

Package Information

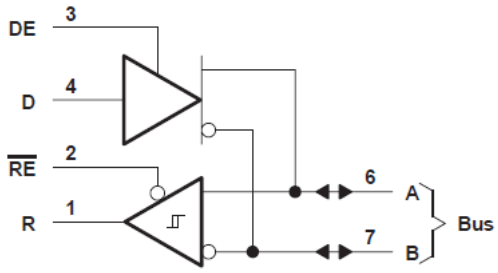
PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65ALS1176	D (SOIC)	4.9 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Symbol



Logic Diagram (Positive Logic)

Table of Contents

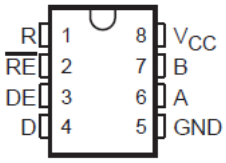
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 1999) to Revision B (January 2023)	Page
• Changed the document to the latest TI format	1
• Deleted the P package option	3
• Deleted the Package thermal impedance from the *Absolute Maximum Ratings*	4
• Added the *Thermal Information* table	4

Changes from Revision * (April 1998) to Revision A (December 1999)	Page
• Changed the document from Product Preview to *Production* data	1

5 Pin Configuration and Functions



A. The D package is available taped and reeled. Add the suffix R to the device type (for example, SN65ALS1176DR).

Figure 5-1. D Package (Top View)

Table 5-1. Pin Functions

NO	Name	Type	Description
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	I	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Local device ground
6	A	I/O	Driver output or receiver input (complementary to B)
7	B	I/O	Driver output or receiver input (complementary to A)
8	V_{CC}	SUPPLY	4.75-V to 5.25-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-7	12	V
V_I	Enable input voltage		5.5	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds)		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Input voltage at any bus terminal (separately or common mode)				12	V
					–7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				± 12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		–25		85	°C

(1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

6.3 Thermal Information

THERMAL METRIC(1)		D (SOIC) 8-Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = – 18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See Figure 7-1	½ V_{OD1} or 2[3]			V
		R_L = 54 Ω	See Figure 7-1	2.1	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = – 7 V to 12 V	See Figure 7-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage[4]	R_L = 54 Ω or 100 Ω	See Figure 7-1			± 0.2	V
V_{OC}	Common-mode output voltage					3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[4]					± 0.2	V
I_O	Output current	Outputs disabled[6]	V_O = 12 V			1	mA
			V_O = – 7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current[5]	V_O = – 4 V				–250	mA
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal

6.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω See Figure 7-3	C_L = 50 pF,			15	ns
$t_{sk(p)}$	Pulse skew[2]				0	2	ns
$t_{t(OD)}$	Differential output transition time				8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω See Figure 7-4	C_L = 50 pF,			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω See Figure 7-5	C_L = 50 pF,			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω See Figure 7-4	C_L = 50 pF,			50	ns

6.5 Switching Characteristics - Driver (continued)

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLZ}	Output disable time from low level	R_L = 110 Ω See Figure 7-5	C_L = 50 pF,			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.6 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$	None	V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	None
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

6.7 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = – 0.4 mA			0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = – 18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, SeeFigure 6	I_{OH} = – 400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = – 200 mV, See Figure 7-6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				± 20	µA
V_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = – 7 V			–0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	mµA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	–15		–85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

6.8 Switching Characteristics - Receiver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = – 1.5 V to 1.5 V, See Figure 7-7	C_L = 15 pF,			25	ns
$t_{sk(p)}$	Pulse skew(2)				0	2	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7-8		11	18	ns
t_{PZL}	Output enable time to low level				11	18	ns
t_{PHZ}	Output disable time from high level					50	ns
t_{PLZ}	Output disable time from low level					30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

7 Parameter Measurement Information

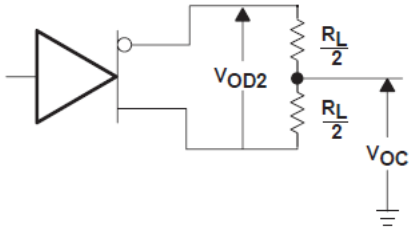


Figure 7-1. Driver V_{OD2} and V_{OC} Test Circuit

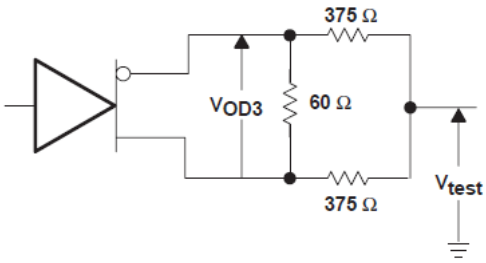
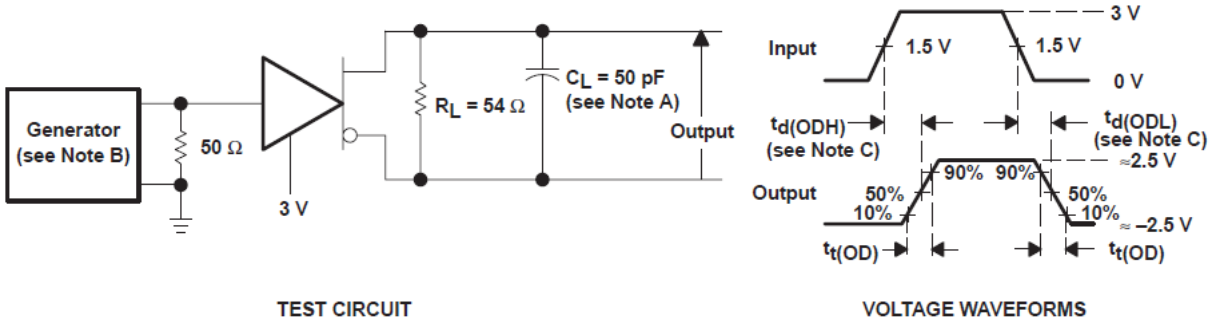
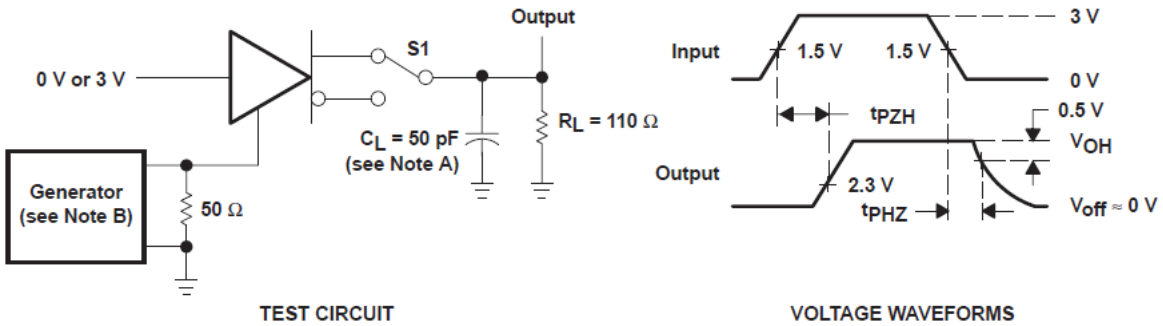


Figure 7-2. Driver V_{OD3} Test Circuit



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
C. $t_{d(OD)} = t_{d(ODH)}$ or $t_{d(ODL)}$.

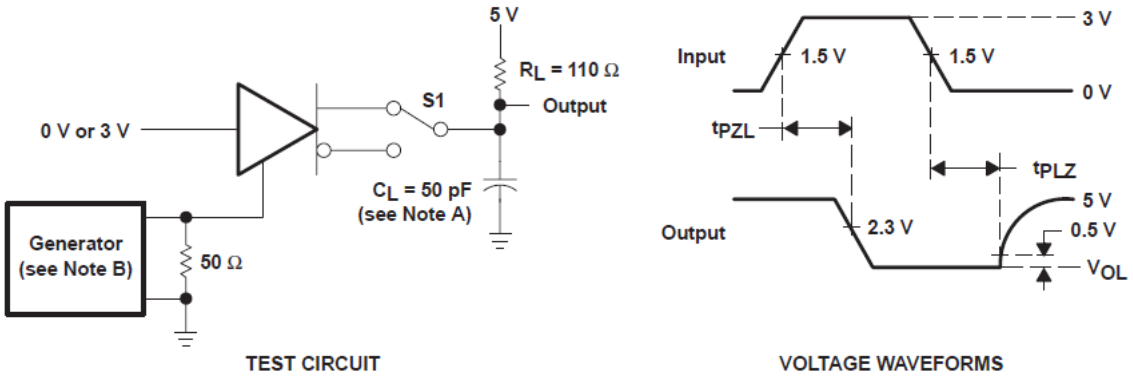
Figure 7-3. Driver Differential-Output Delay and Transition Times



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7-4. Driver Enable and Disable Times



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7-5. Driver Enable and Disable Times

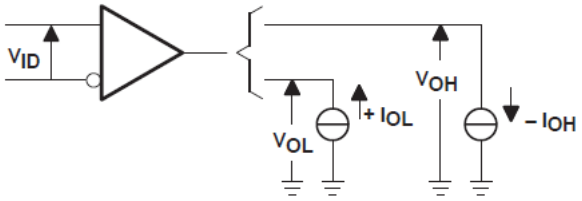
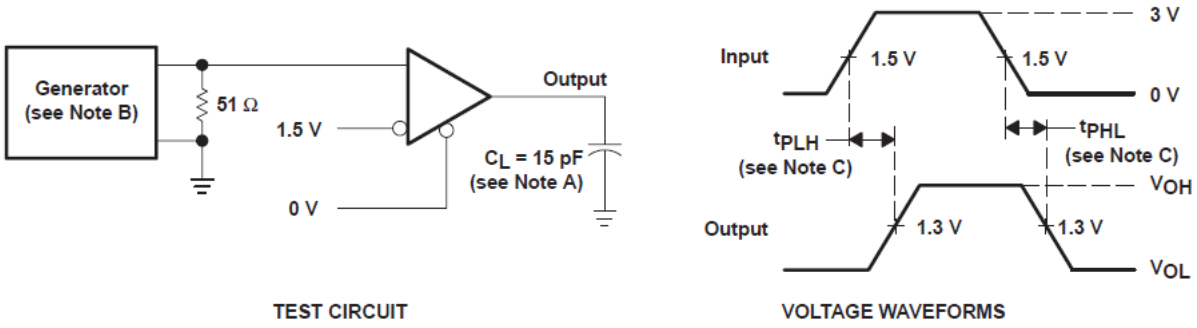


Figure 7-6. Receiver V_{OH} and V_{OL} Test Circuit

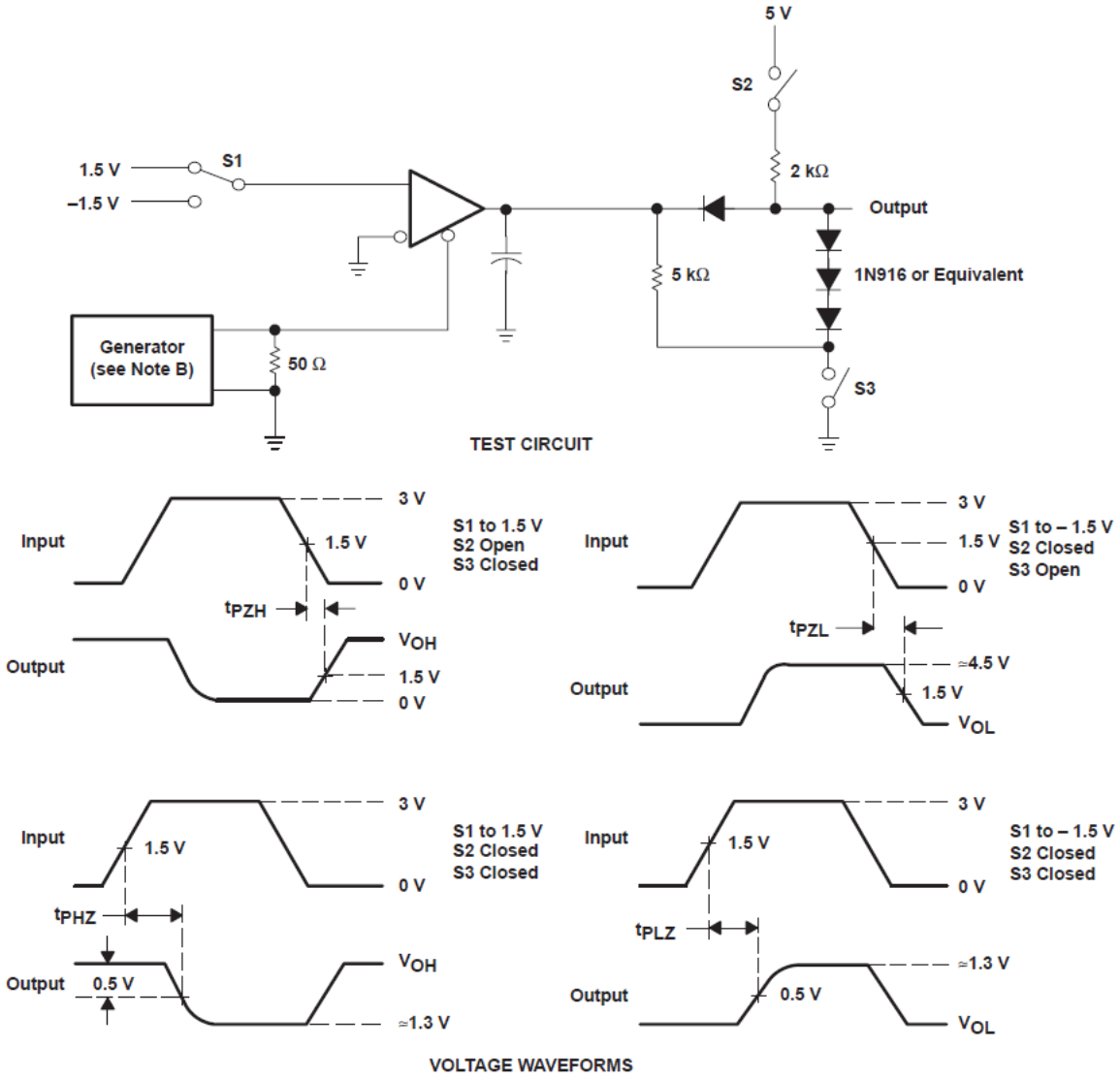


A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

C. $t_{pd} = t_{PLH}$ or t_{PHL}.

Figure 7-7. Receiver Propagation-Delay Times



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7-8. Receiver Output Enable and Disable Times

8 Detailed Description

8.1 Functional Block Diagram

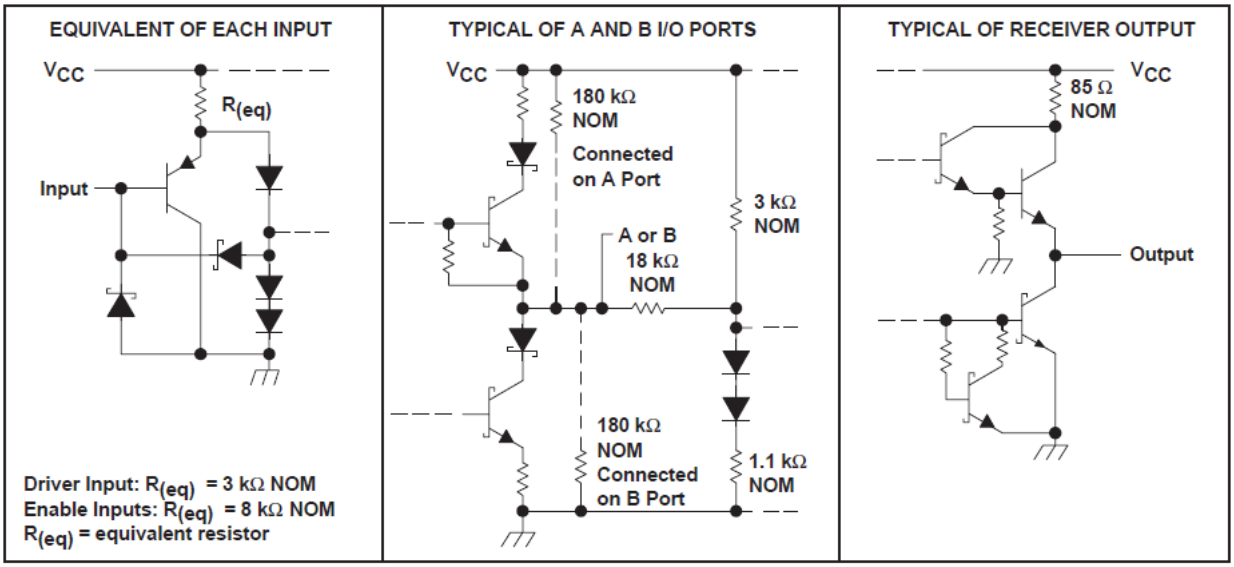


Figure 8-1. Schematics of Inputs and Outputs

8.2 Device Functional Modes

Function Tables

Table 8-1. Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off).

Table 8-2. Receiver(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off).

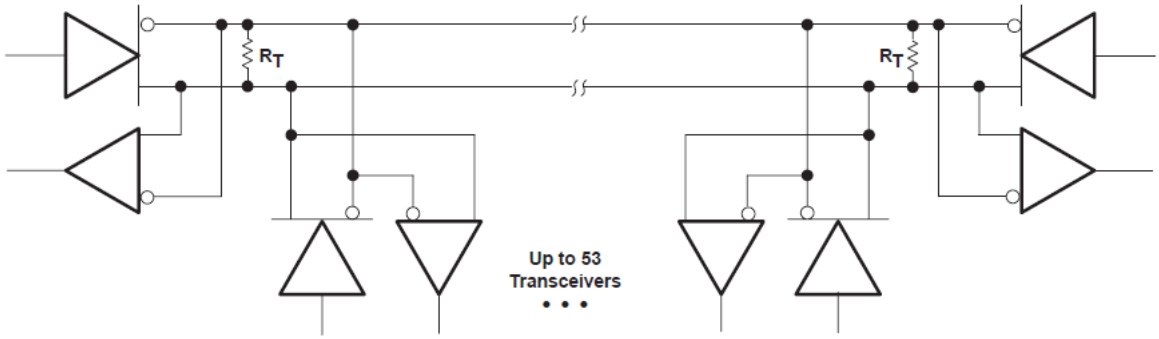
9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Typical Application



A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 9-1. Typical Application Circuit

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS1176D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	
SN65ALS1176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

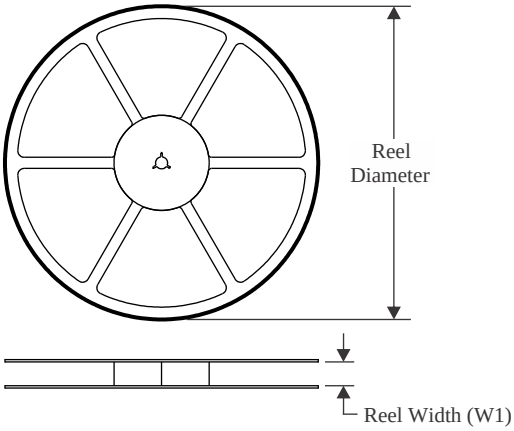
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

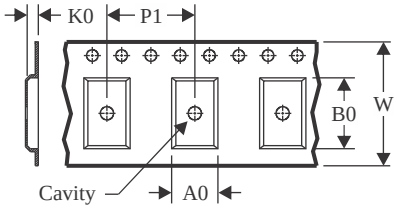
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

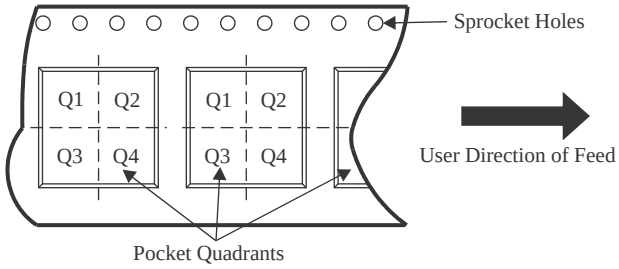


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

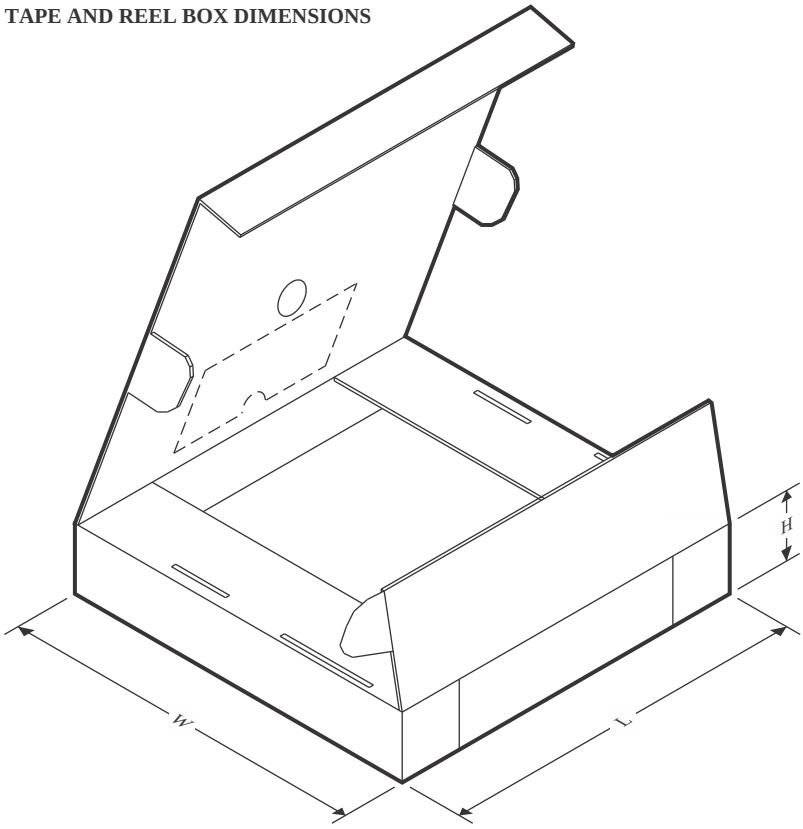
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

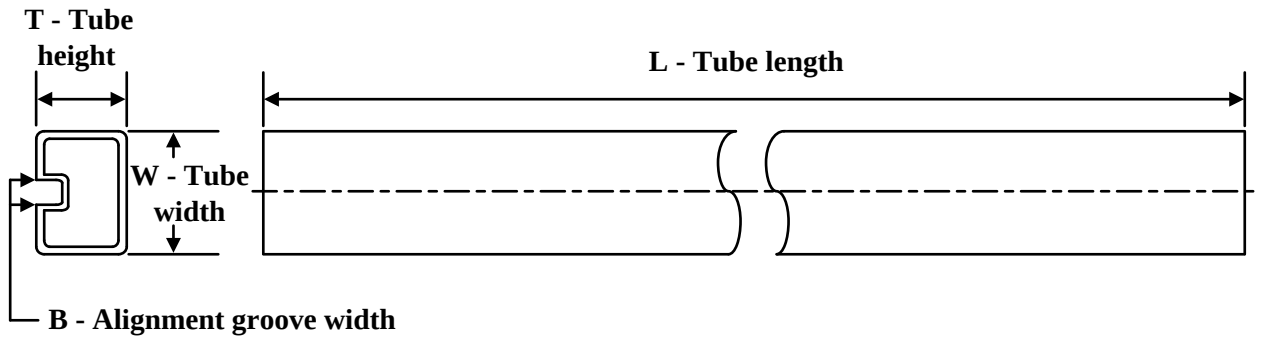
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

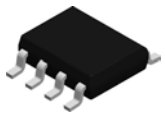
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS1176DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65ALS1176D	D	SOIC	8	75	507	8	3940	4.32

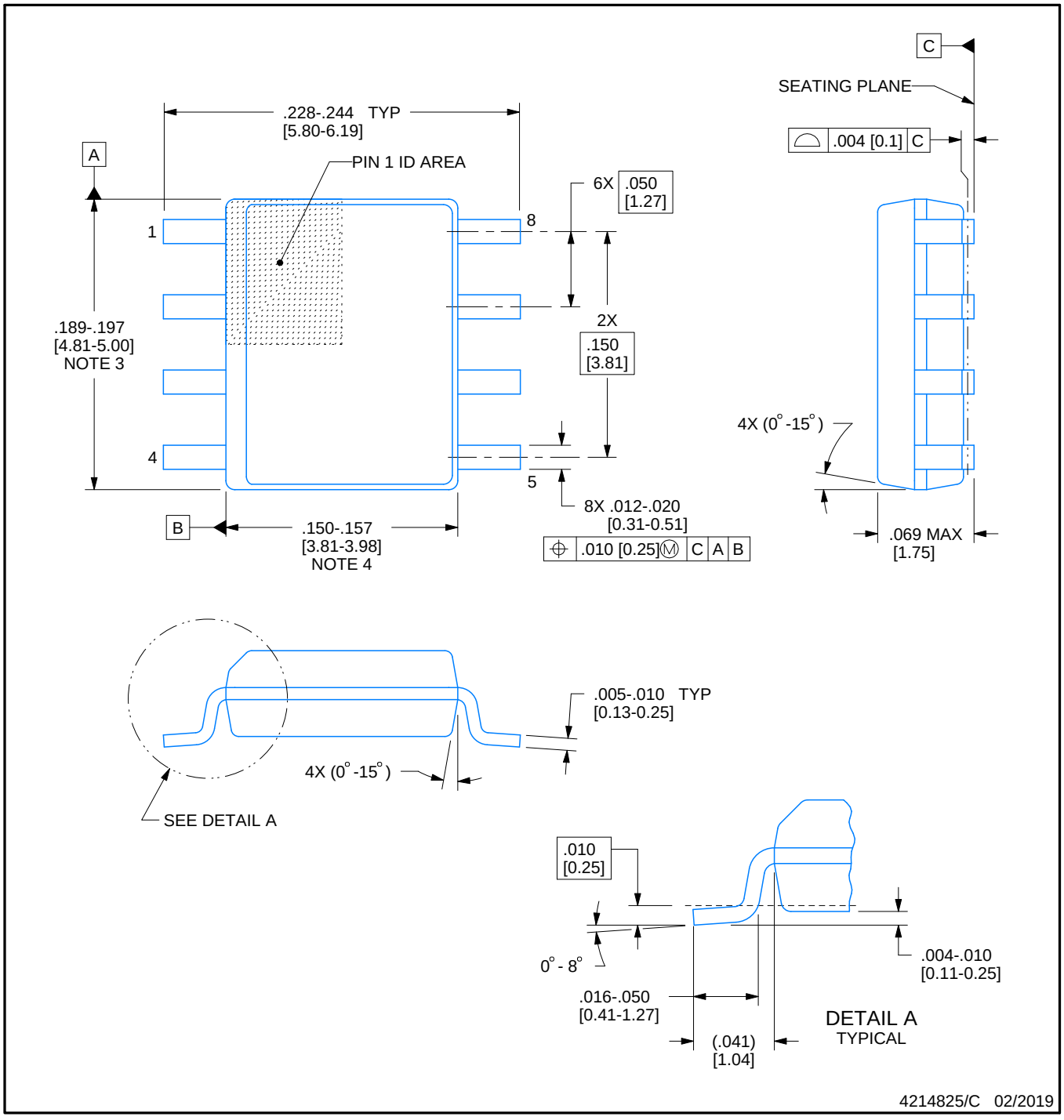


PACKAGE OUTLINE

D0008A

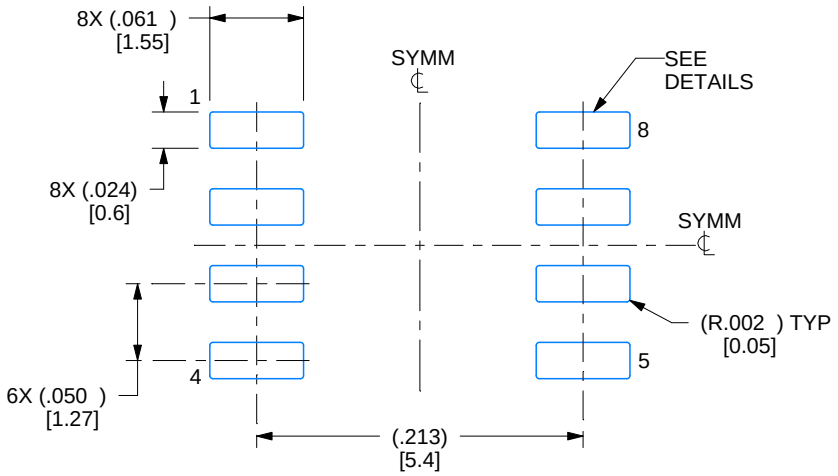
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

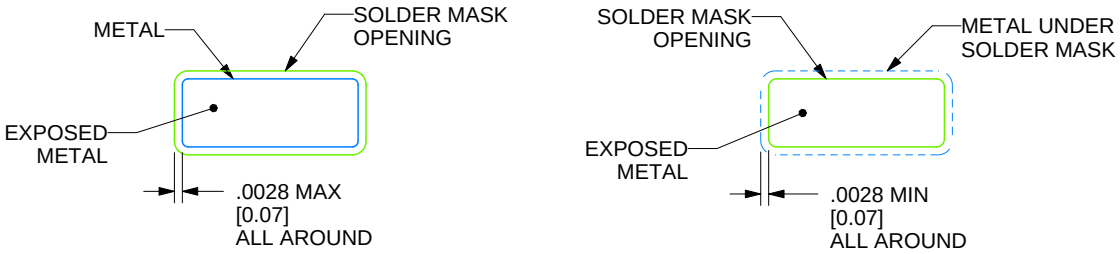


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

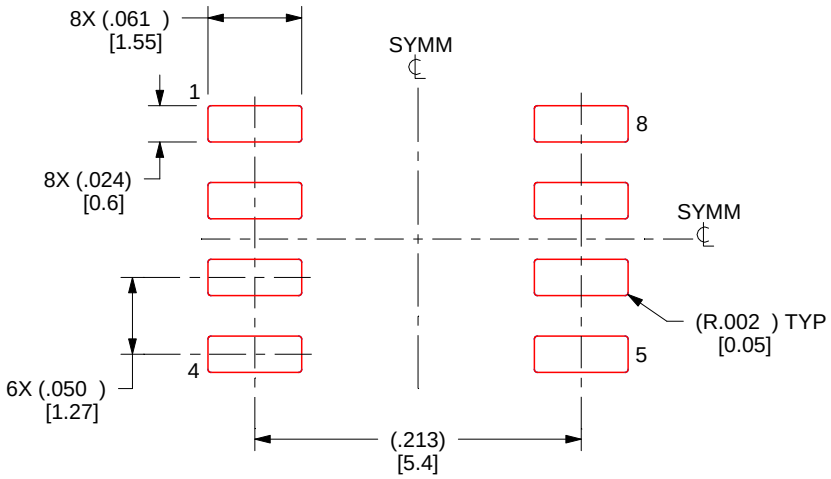
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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