

SN54F74, SN74F74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDFS046A – MARCH 1987 – REVISED OCTOBER 1993

- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

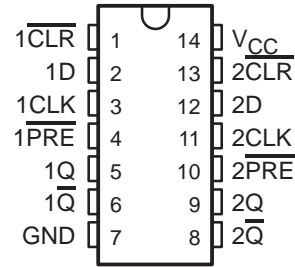
The SN54F74 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F74 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

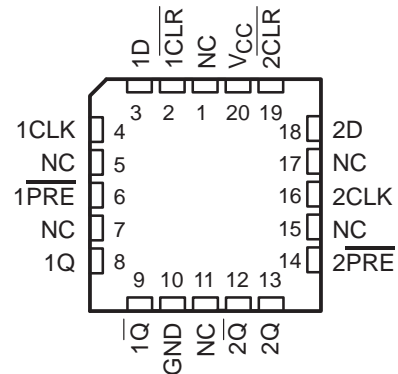
| INPUTS | | | | OUTPUTS | |
|-------------------------|-------------------------|-----|---|----------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H [†] | H [†] |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | $\overline{\text{Q}}_0$ |

† The output levels are not guaranteed to meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

**SN54F74 . . . J PACKAGE
SN74F74 . . . D OR N PACKAGE
(TOP VIEW)**



**SN54F74 . . . FK PACKAGE
(TOP VIEW)**

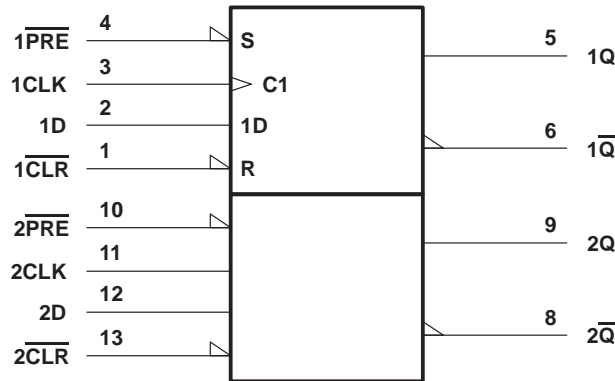


NC – No internal connection

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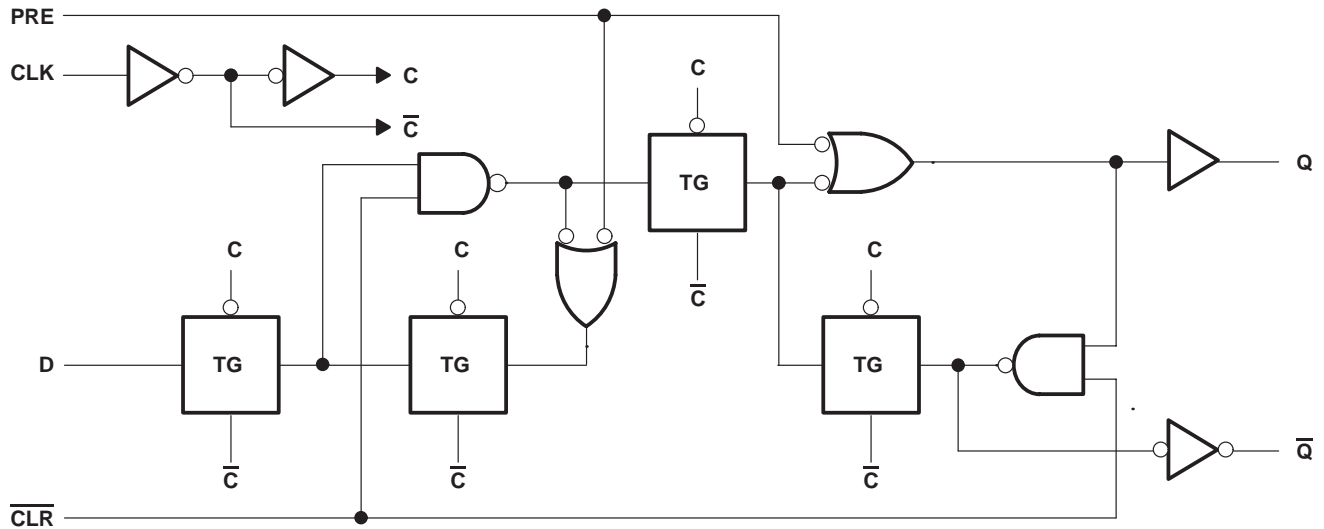
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|--------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -1.2 V to 7 V |
| Input current range | -30 mA to 5 mA |
| Voltage range applied to any output in the high state | -0.5 V to V_{CC} |
| Current into any output in the low state | 40 mA |
| Operating free-air temperature range: SN54F74 | -55°C to 125°C |
| SN74F74 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

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recommended operating conditions

| | | SN54F74 | | | SN74F74 | | | UNIT |
|----------|--------------------------------|---------|-----|-----|---------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{IK} | Input clamp current | | | -18 | | | -18 | mA |
| I_{OH} | High-level output current | | | -1 | | | -1 | mA |
| I_{OL} | Low-level output current | | | 20 | | | 20 | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F74 | | | SN74F74 | | | UNIT |
|-----------|--|----------------------------|-------------------------|---------|------|------|---------|------|------|------|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | | | -1.2 | V |
| V_{OH} | | $V_{CC} = 4.5\text{ V}$, | $I_{OH} = -1\text{ mA}$ | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $V_{CC} = 4.75\text{ V}$, | $I_{OH} = -1\text{ mA}$ | | | | 2.7 | | | |
| V_{OL} | | $V_{CC} = 4.5\text{ V}$, | $I_{OL} = 20\text{ mA}$ | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| I_I | | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} | | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 20 | | | 20 | μA |
| I_{IL} | Data, CLK | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.5\text{ V}$ | | | -0.6 | | | -0.6 | mA |
| | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | | | | | -1.8 | | | -1.8 | |
| $I_{OS}‡$ | | $V_{CC} = 5.5\text{ V}$, | $V_O = 0$ | -60 | | -150 | -60 | | -150 | mA |
| I_{CC} | | $V_{CC} = 5.5\text{ V}$, | See Note 2 | | 10.5 | 16 | | 10.5 | 16 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with D, CLK, and $\overline{\text{PRE}}$ grounded then with D, CLK, and $\overline{\text{CLR}}$ grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | | SN54F74 | | SN74F74 | | UNIT |
|--------------------|---|--|--|-----|---------|-----|---------|-----|------|
| | | | 'F74 | | | | | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | | 0 | 100 | 0 | 80 | 0 | 100 | MHz |
| t_w | Pulse duration | | CLK high, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low | | 4 | 4 | 4 | 4 | ns |
| | | | CLK low | | 5 | 6 | 5 | 5 | |
| t_{su} | Setup time, data before CLK↑ | | High | | 2 | 3 | 2 | 2 | ns |
| | | | Low | | 3 | 4 | 3 | 3 | |
| | Setup time, inactive-state before CLK↑§ | | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK | | 2 | 3 | 2 | 2 | |
| t_h | Hold time, data after CLK↑ | | High | | 1 | 2 | 1 | 1 | ns |
| | | | Low | | 1 | 2 | 1 | 1 | |

§ Inactive-state setup time is also referred to as recovery time.



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switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C | | | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX† | | | UNIT | |
|------------------|--|----------------|---|-----|-----|---|------|---------|------|-----|
| | | | 'F74 | | | SN54F74 | | SN74F74 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| f _{max} | | | 100 | 145 | | 80 | | 100 | MHz | |
| t _{PLH} | CLK | Q or \bar{Q} | 3 | 4.9 | 6.8 | 3.8 | 8.5 | 3 | 7.8 | ns |
| t _{PHL} | | | 3.6 | 5.8 | 8 | 4.4 | 10.5 | 3.6 | 9.2 | |
| t _{PLH} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or \bar{Q} | 2.4 | 4.2 | 6.1 | 3.2 | 8 | 2.4 | 7.1 | ns |
| t _{PHL} | | | 2.7 | 6.6 | 9 | 3.5 | 11.5 | 2.7 | 10.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------|-------------------------|
| 5962-9759201Q2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9759201Q2A SNJ54F74FK | Samples |
| 5962-9759201QCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9759201QCA SNJ54F74J | Samples |
| 5962-9759201QDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9759201QDA SNJ54F74W | Samples |
| JM38510/34101B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/34101B2A | Samples |
| JM38510/34101BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/34101BCA | Samples |
| JM38510/34101BDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/34101BDA | Samples |
| M38510/34101B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | M38510/34101B2A | Samples |
| M38510/34101BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | M38510/34101BCA | Samples |
| M38510/34101BDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | M38510/34101BDA | Samples |
| SN54F74J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54F74J | Samples |
| SN74F74D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F74 | Samples |
| SN74F74DG4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F74 | Samples |
| SN74F74DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F74 | Samples |
| SN74F74DRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F74 | Samples |
| SN74F74N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74F74N | Samples |
| SN74F74NE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74F74N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|----------------------------------|-------------------------|
| SN74F74NSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74F74 | Samples |
| SNJ54F74FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9759201Q2A SNJ54F74FK | Samples |
| SNJ54F74J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9759201QC A SNJ54F74J | Samples |
| SNJ54F74W | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9759201QD A SNJ54F74W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54F74, SN74F74 :

- Catalog : [SN74F74](#)
- Military : [SN54F74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74F74DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74F74NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74F74DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74F74NSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9759201Q2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 5962-9759201QDA | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/34101B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/34101BDA | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/34101B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/34101BDA | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74F74D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74F74DG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74F74N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F74N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F74NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74F74NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54F74FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54F74W | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

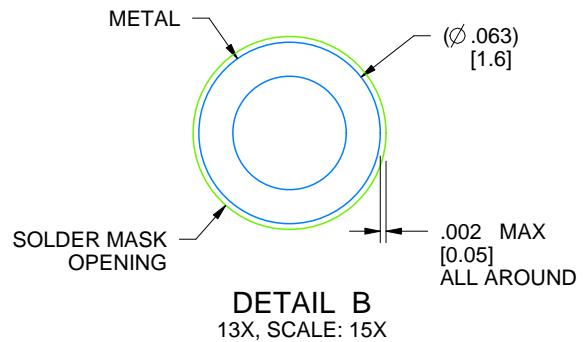
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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