SN74LV240A Octal Inverting Buffers/Drivers With 3-State Outputs

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA per JESD 17
- I_{off} Supports Live Insertion, Partial Power-Down Mode, and Back Drive Protection

2 Applications

- Handset: Smartphone
- Network Switch
- Health and Fitness / Wearables

3 Description

These octal buffers/drivers with inverted outputs are designed for 2 V to 5.5 V V_{CC} operation.

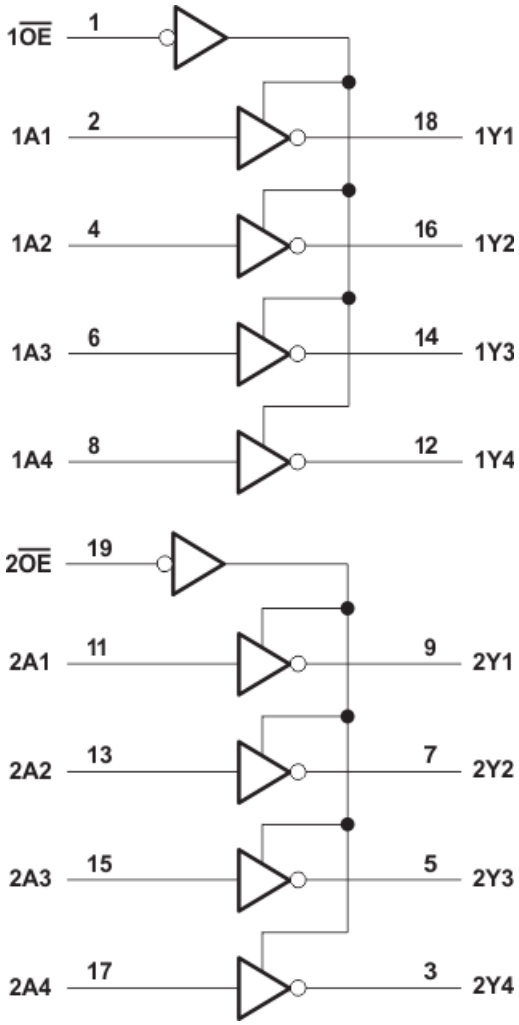
The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV240A	TVSOP (14)	3.60 mm × 4.40 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SO (14)	10.30 mm × 5.30 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

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4 Revision History

Changes from Revision I (February 2015) to Revision J (December 2022)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision H (April 2005) to Revision I (Feruary 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated operating free-air temperature maximum from 85°C to 125°C for SN74LV240A	6

5 Pin Configuration and Functions

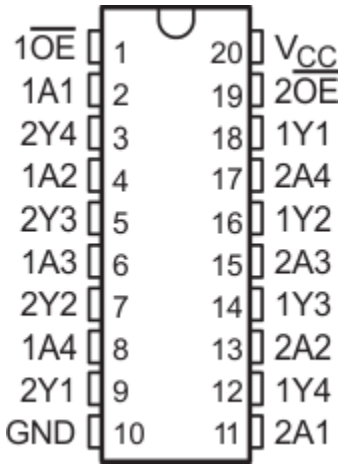


Figure 5-1. SN74LV240A: DB, DGV, DW, NS, or PW Package Top View

Table 5-1. Pin Functions

NAME[1]	PIN	TYPE	DESCRIPTION
1OE	1	I	Output enable 1
1A1	2	I	1A1 input
2Y4	3	O	2Y4 output
1A2	4	I	1A2 input
2Y3	5	O	2Y3 output
1A3	6	I	1A3 input
2Y2	7	O	2Y2 output
1A4	8	I	1A4 input
2Y1	9	O	2Y1 output
GND	10	—	Ground pin
2A1	11	I	2A1 input
1Y4	12	O	1Y4 output
2A2	13	I	2A2 input
1Y3	14	O	1Y3 output
2A3	15	I	2A3 input
1Y2	16	O	1Y2 output
2A4	17	I	2A4 input
1Y1	18	O	1Y1 output
2OE	19	I	Output enable 2
VCC	20	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	–35	35	mA
	Continuous current through V_{CC} or GND		–70	70	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction Temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 2.3 to 2.7 V		–2	mA
		V_{CC} = 3 to 3.6 V		–8	
		V_{CC} = 4.5 to 5.5 V		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 to 2.7 V		2	mA
		V_{CC} = 3 to 3.6 V		8	
		V_{CC} = 4.5 to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 to 2.7 V		200	ns/V
		V_{CC} = 3 to 3.6 V		100	
		V_{CC} = 4.5 to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		DW	DB	DGV	NS	PW	UNIT
		20 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	79.2	94.5	116.2	76.7	102.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.7	56.4	31.2	43.2	36.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.0	49.7	57.7	44.2	53.6	
ψ_{JT}	Junction-to-top characterization parameter	18.6	18.5	0.9	16.8	2.4	
ψ_{JB}	Junction-to-board characterization parameter	46.5	49.3	57.0	43.8	52.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –50 µA	2 to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			
		I_{OH} = –8 mA	3 V	2.48			
		I_{OH} = –16 mA	4.5 V	3.8			
V_{OL}	Low level output voltage	I_{OL} = 50 µA	2 to 5.5 V			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4	
		I_{OL} = 8 mA	3 V			0.44	
		I_{OL} = 16 mA	4.5 V			0.55	
I_I	Input leakage current	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{OZ}	Off-State (High-Impedance State) Output Current (of a 3-State Output)	V_O = V_{CC} or GND	5.5 V			±5	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
I_{off}	Input/Output Power-Off Leakage Current	V_I or V_O = 0 to 5.5 V	0			5	µA
C_i	Input Capacitance	V_I = V_{CC} or GND	3.3 V		2.3		pF

6.6 Switching Characteristics, V_{CC} = 2.5 V ±0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Section 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	C_L = 15 pF		6.3(1)	11.6(1)	1(2)	14(2)	ns
t_{en}	$\overline{OE}$				8.5(1)	14.6(1)	1(2)	17(2)	
t_{dis}	$\overline{OE}$				9.7(1)	14.1(1)	1(2)	16(2)	
t_{pd}	A	Y	C_L = 50 pF		8.2	14.4	1	17	ns
t_{en}	$\overline{OE}$				10.3	17.8	1	21	
t_{dis}	$\overline{OE}$				14.2	19.2	1	21	
$t_{sk(o)}$						2		2(3)	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) Value applies for SN74LV240A only

6.7 Switching Characteristics, V_{CC} = 3.3 V ±0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Section 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	C_L = 15 pF		4.6(1)	7.5(1)	1(2)	9(2)	ns
t_{en}	$\overline{OE}$				6.2(1)	10.6(1)	1(2)	12.5(2)	
t_{dis}	$\overline{OE}$				8.3(1)	12.5(1)	1(2)	13.5(2)	
t_{pd}	A	Y	C_L = 50 pF		5.9	11	1	12.5	ns
t_{en}	$\overline{OE}$				7.5	14.1	1	16	
t_{dis}	$\overline{OE}$				11.8	15	1	17	
$t_{sk(o)}$						1.5		1.5(3)	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) Value applies for SN74LV240A only

6.8 Switching Characteristics, V_{CC} = 5 V ±0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Section 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	C_L = 15 pF		3.4(1)	5.5(1)	1(2)	6.5(2)	ns
t_{en}	$\overline{OE}$				4.6(1)	7.3(1)	1(2)	8.5(2)	
t_{dis}	$\overline{OE}$				7.4(1)	12.2(1)	1(2)	13.5(2)	
t_{pd}	A	Y	C_L = 50 pF		4.4	7.5	1	8.5	ns
t_{en}	$\overline{OE}$				5.6	9.3	1	10.5	
t_{dis}	$\overline{OE}$				9.7	14.2	1	15.5	
$t_{sk(o)}$						1		1(3)	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) This values applies for SN74LV240A only

6.9 Noise Characteristics for SN74LV240A

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see (1))

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.56		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.49		
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.82		
$V_{IH(D)}$	High-level dynamic input voltage	2.31			
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	

(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF f = 10 MHz	3.3 V	14	pF
			5 V	16.4	

6.11 Typical Characteristics

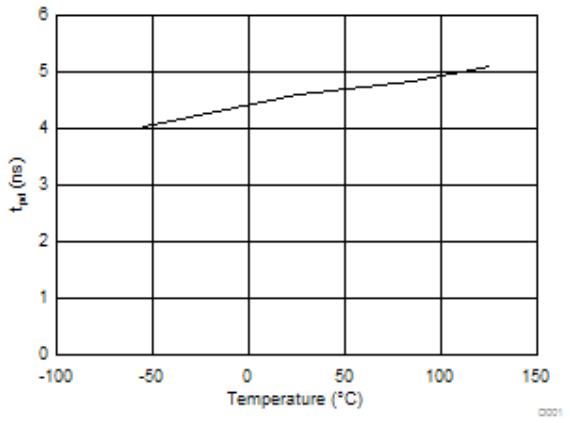


Figure 6-1. t_{pd} vs Temperature at 3.3-V V_{CC}

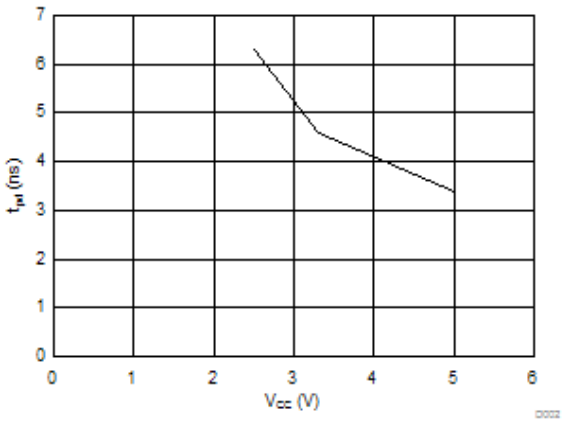
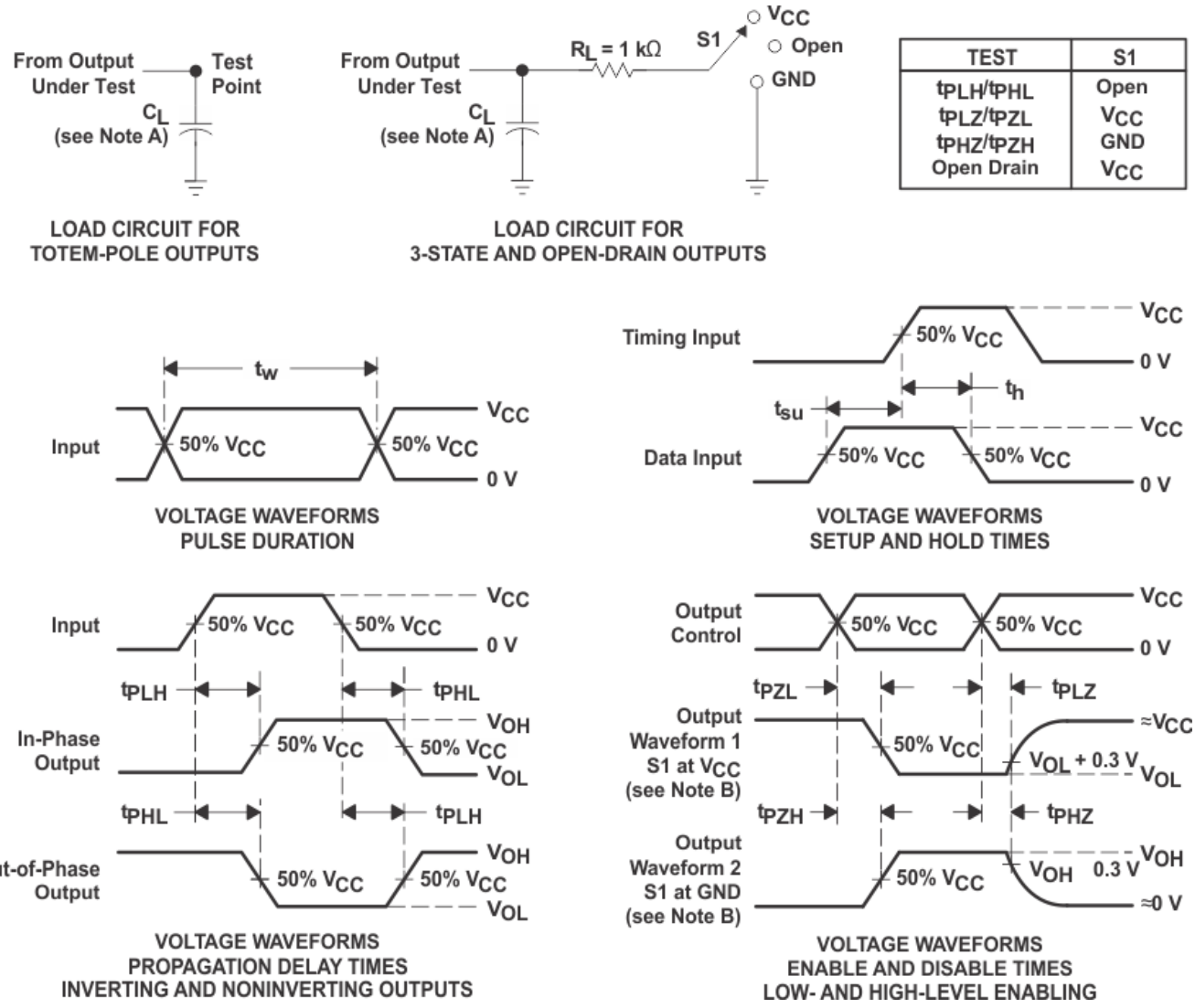


Figure 6-2. t_{pd} vs V_{CC} at 25°C

7 Parameter Measurement Information

7.1



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and tPZH are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These octal buffers/drivers with inverted outputs are designed for 2 V to 5.5 V V_{CC} operation.

The ’LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

8.2 Functional Block Diagram

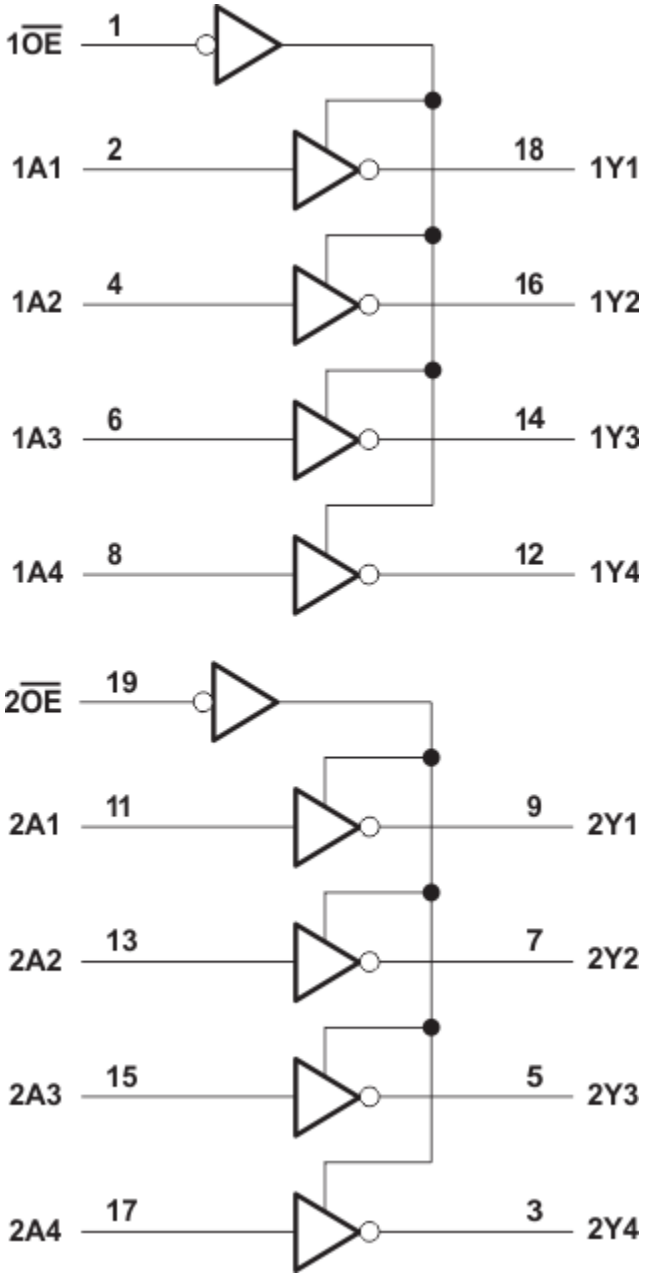


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

- Wide operating voltage range operates from 2 V to 5.5 V operation
- Allow down voltage translation inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V

8.4 Device Functional Modes

Table 8-1. Function Table (Each Buffer)

INPUTS(1)		OUTPUT (2)
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV240A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. It can produce 8 mA of drive current at 3.3 V making it ideal for driving multiple outputs and low-noise applications. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC}.

9.2 Typical Application

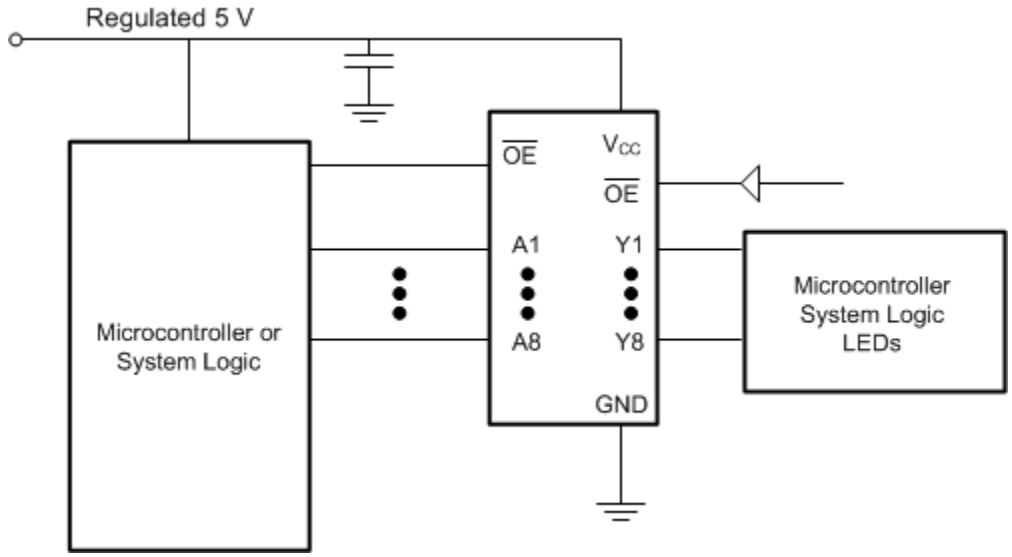


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specifications see (Δt/ΔV) in *Section 6.3*.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Section 6.3*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
   - Load currents should not exceed 35 mA per output and 70 mA total for the part
   - Outputs should not be pulled above V_{CC}

9.2.3 Application Curve

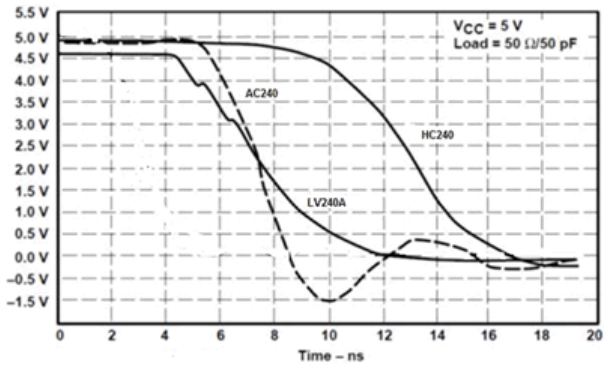


Figure 9-2. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *Section 6.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 µF and if there are multiple V_{CC} terminals, then TI recommends .01 µF or .022 µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

11.2 Layout Example

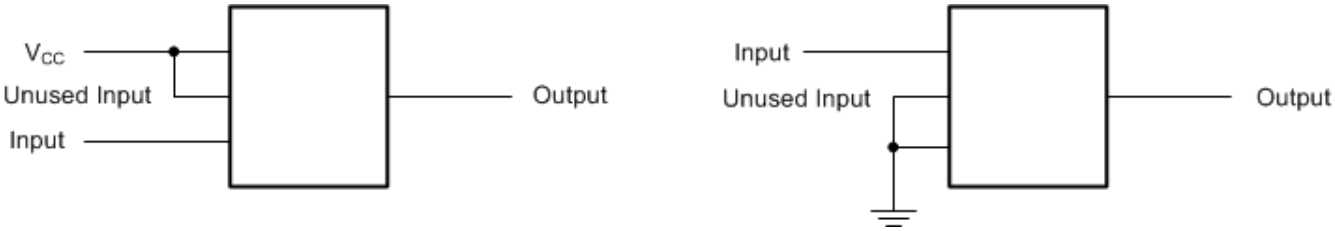


Figure 11-1. Layout Recommendation

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LV240A	Click here	Click here	Click here	Click here	Click here
SN74LV240A	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV240ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240ADBRE4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV240A	Samples
SN74LV240APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240APWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples
SN74LV240APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

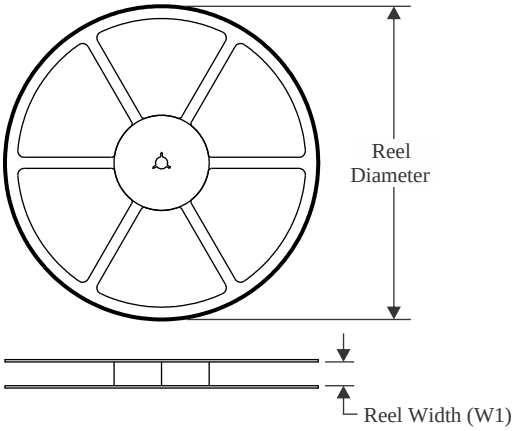
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

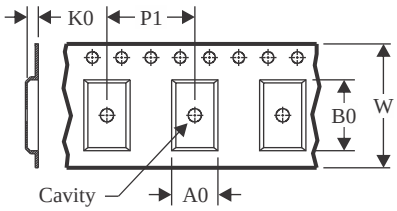
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

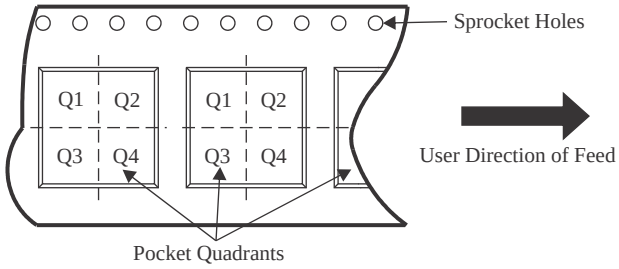


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

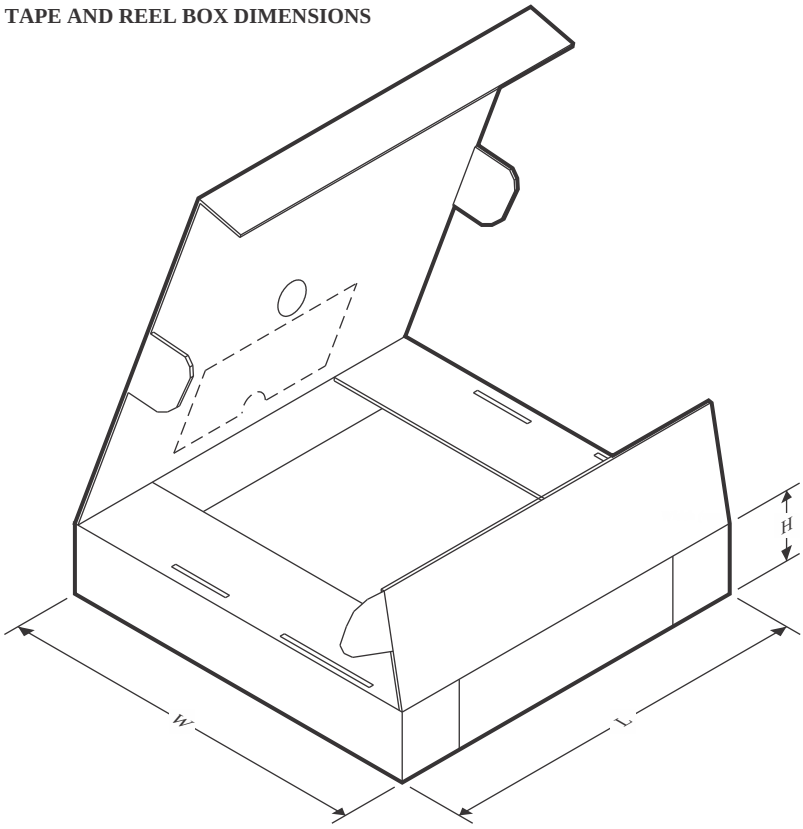
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV240ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV240ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV240ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV240ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV240APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV240APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV240APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV240APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

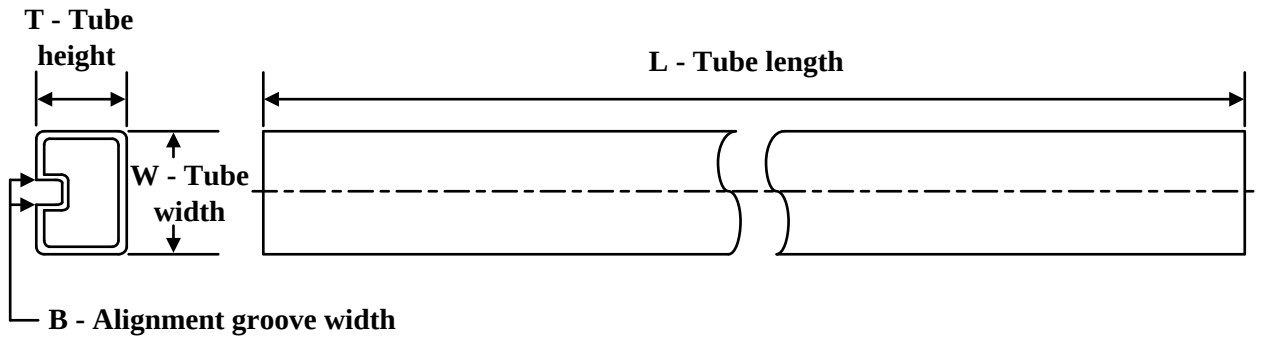
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV240ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV240ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV240ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV240ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV240APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV240APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LV240APWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV240APWT	TSSOP	PW	20	250	356.0	356.0	35.0

TUBE



*All dimensions are nominal

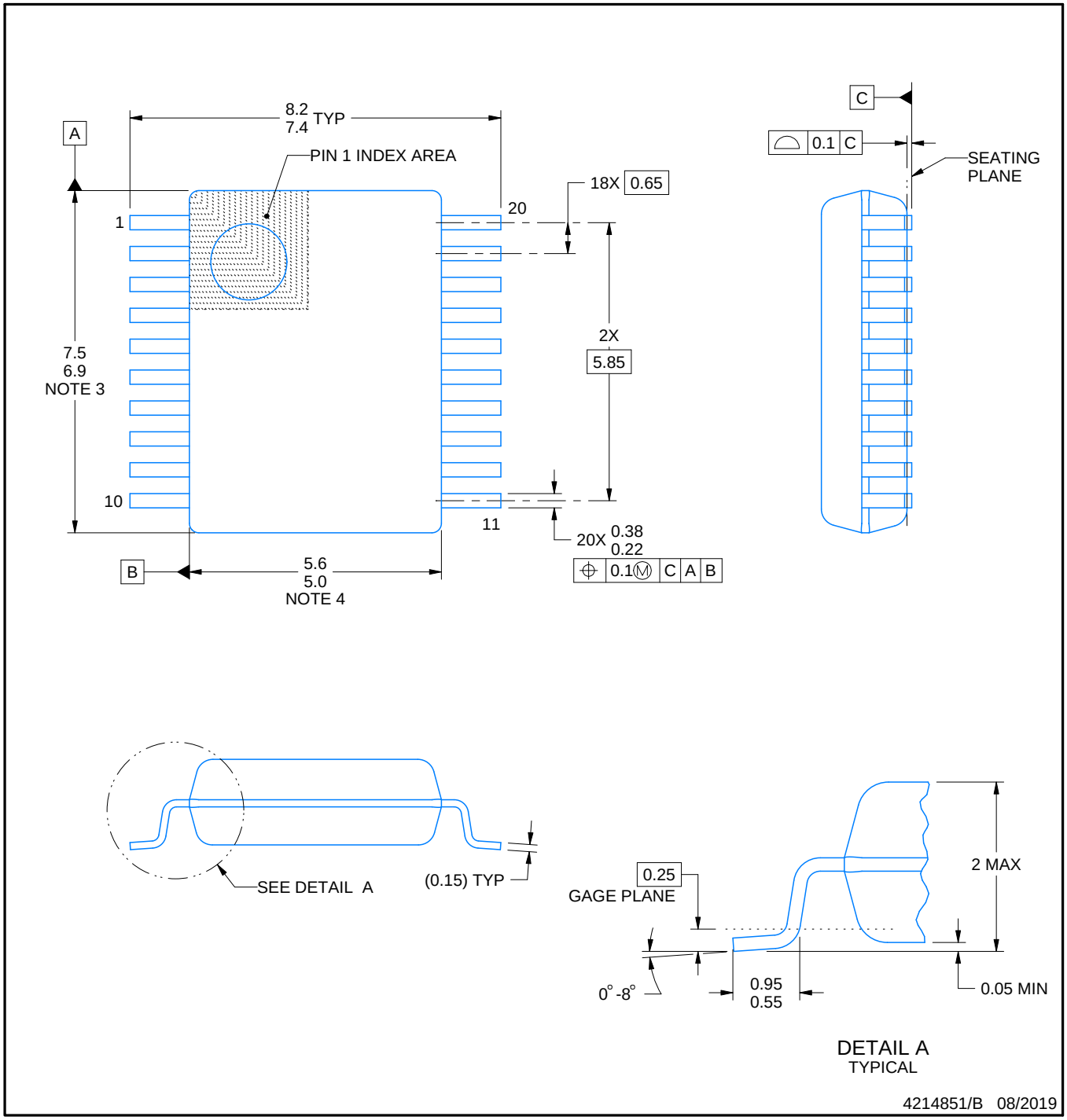
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV240ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LV240APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LV240APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

DB0020A

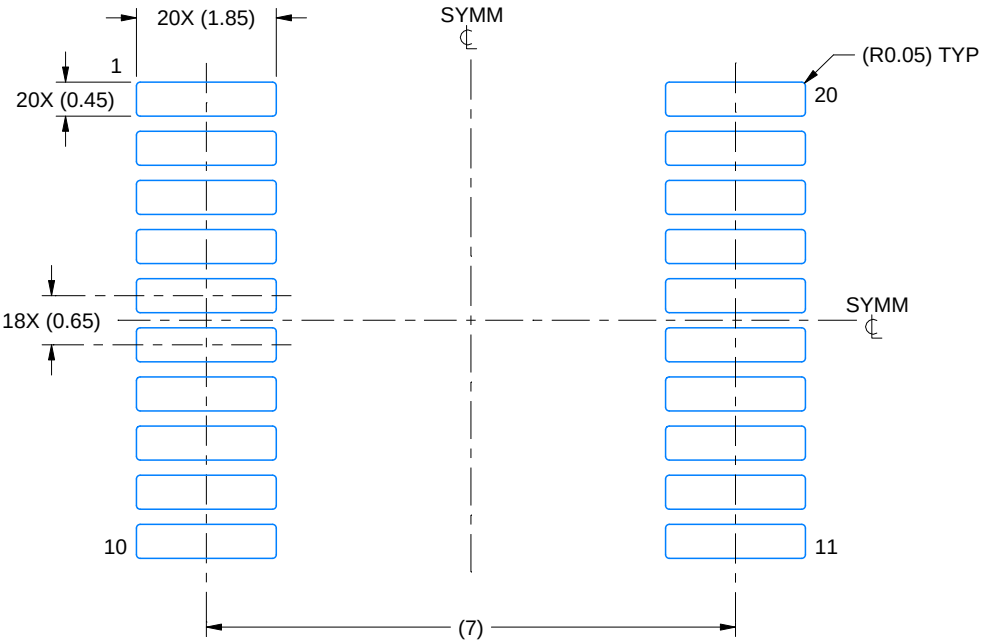
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

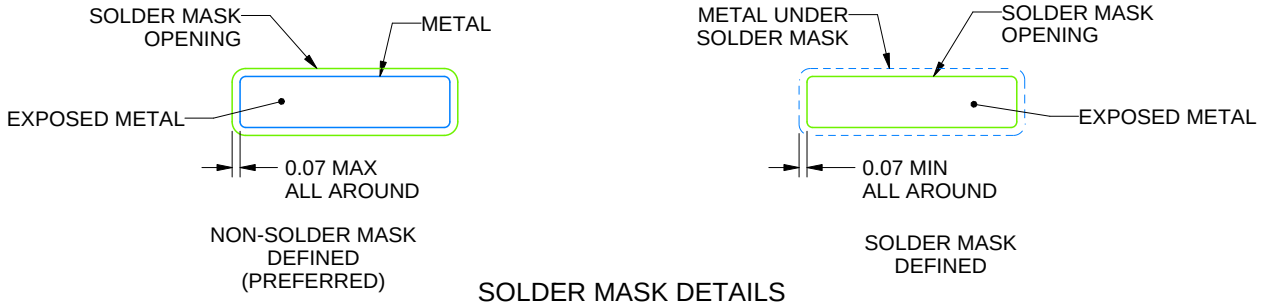


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

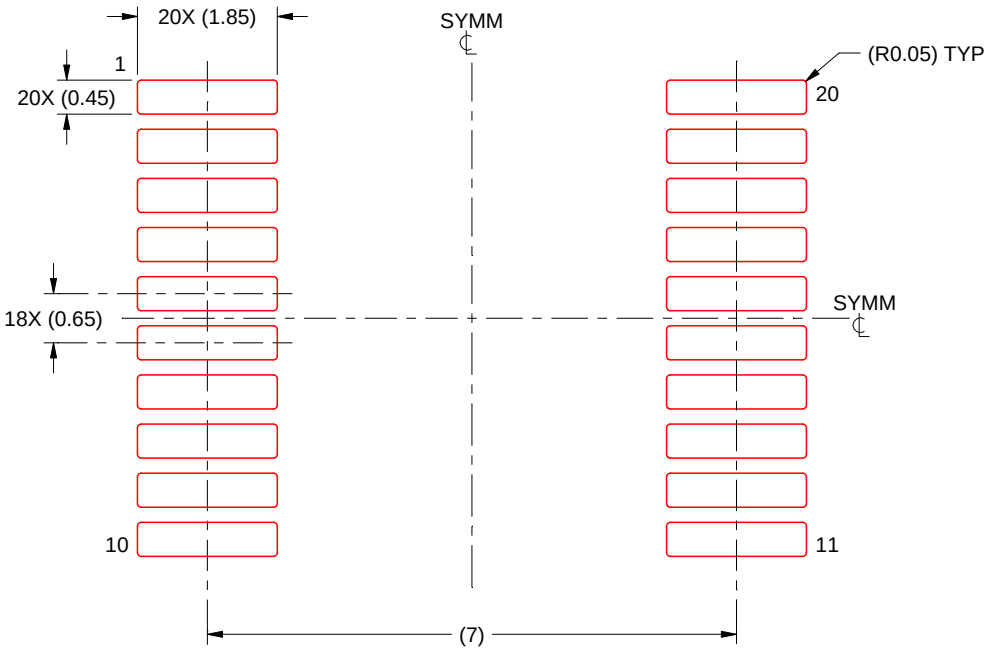
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

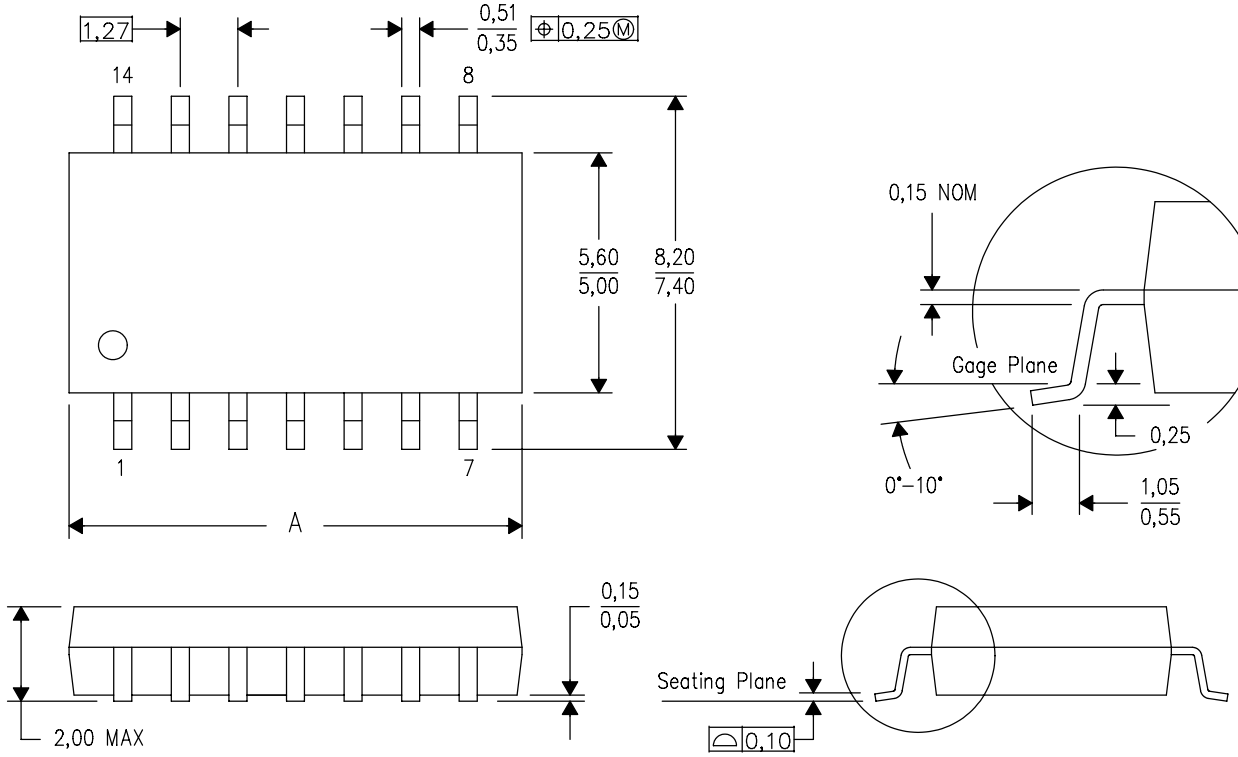
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



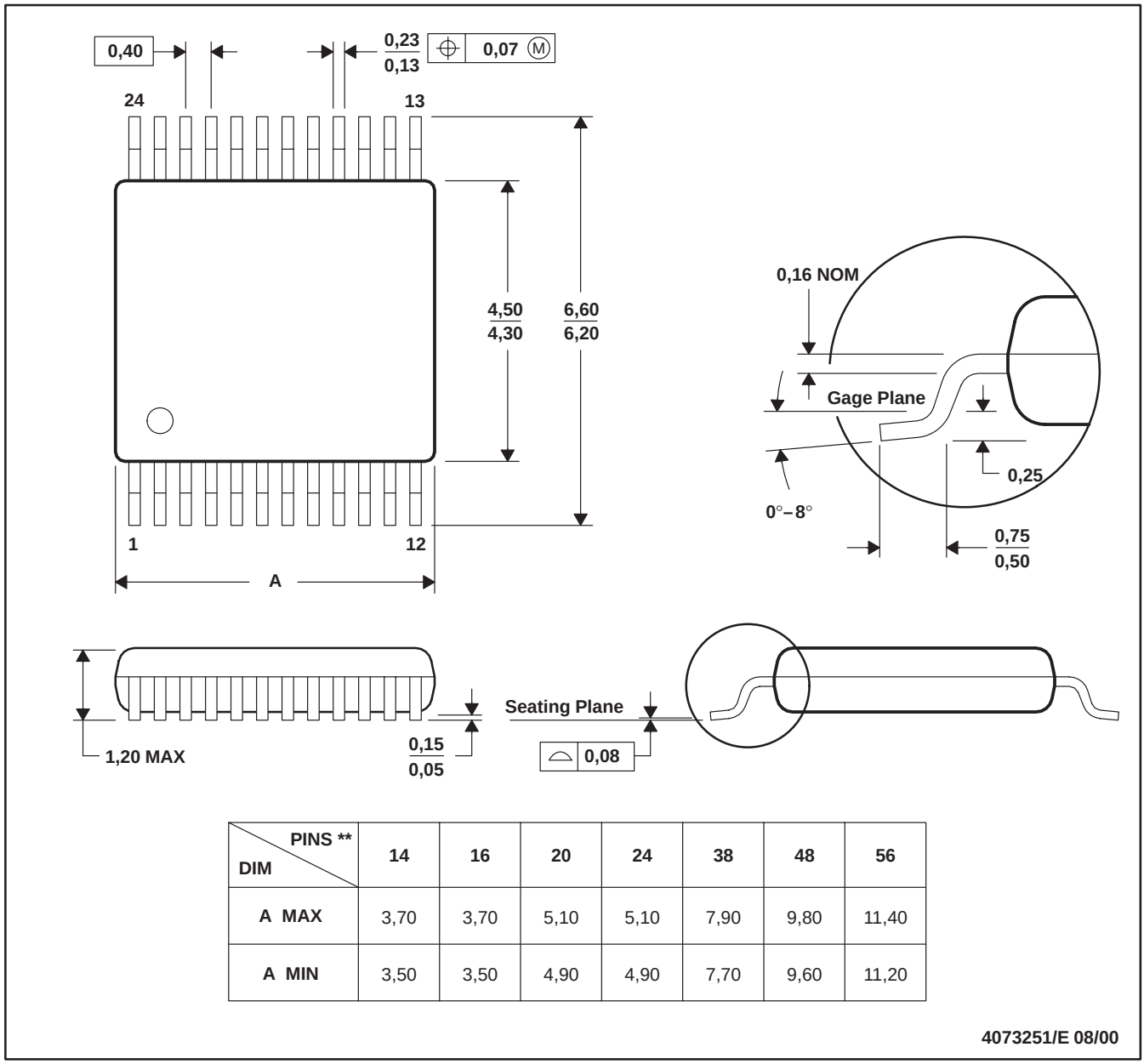
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

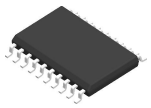
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

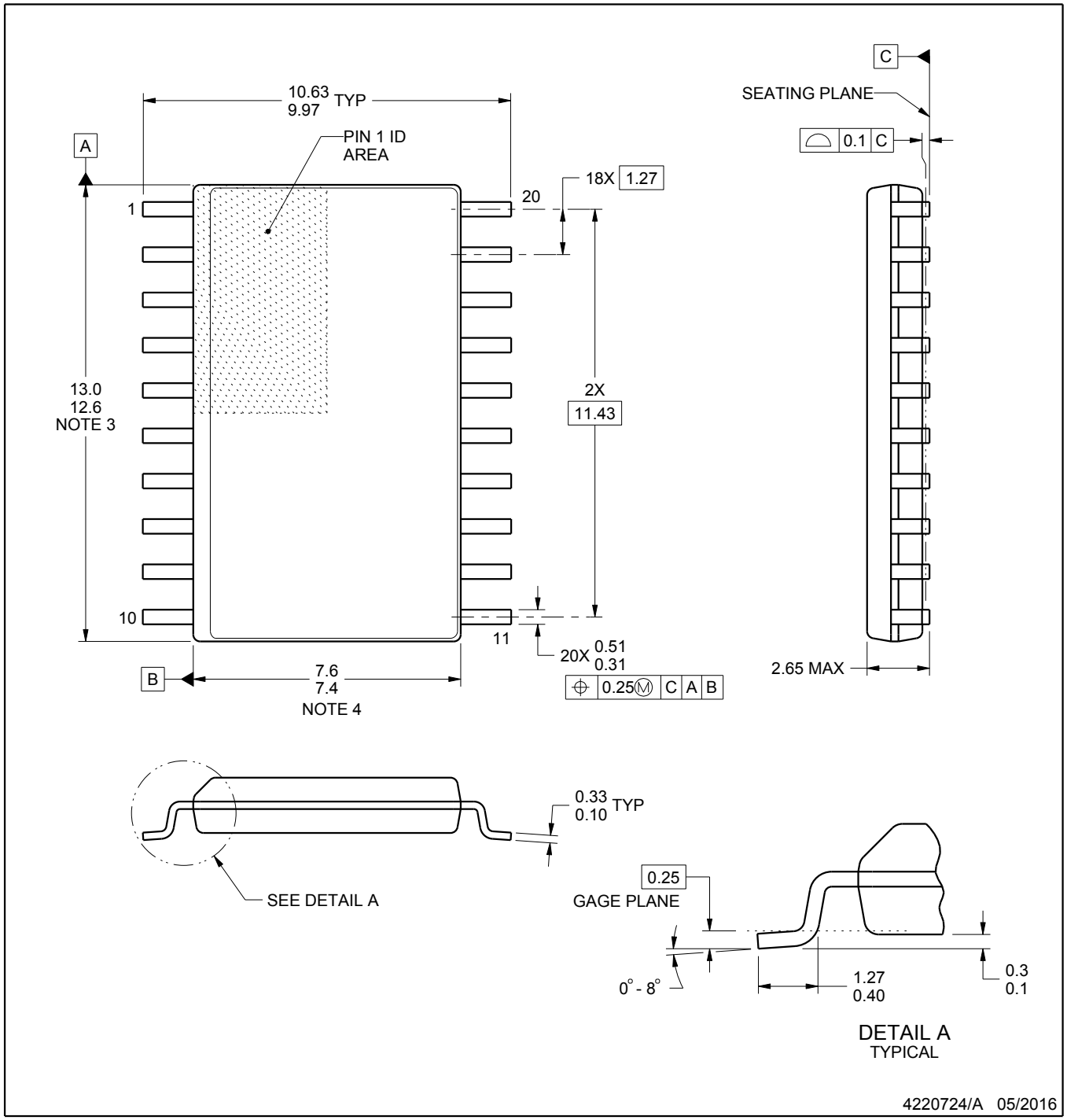


PACKAGE OUTLINE

DW0020A

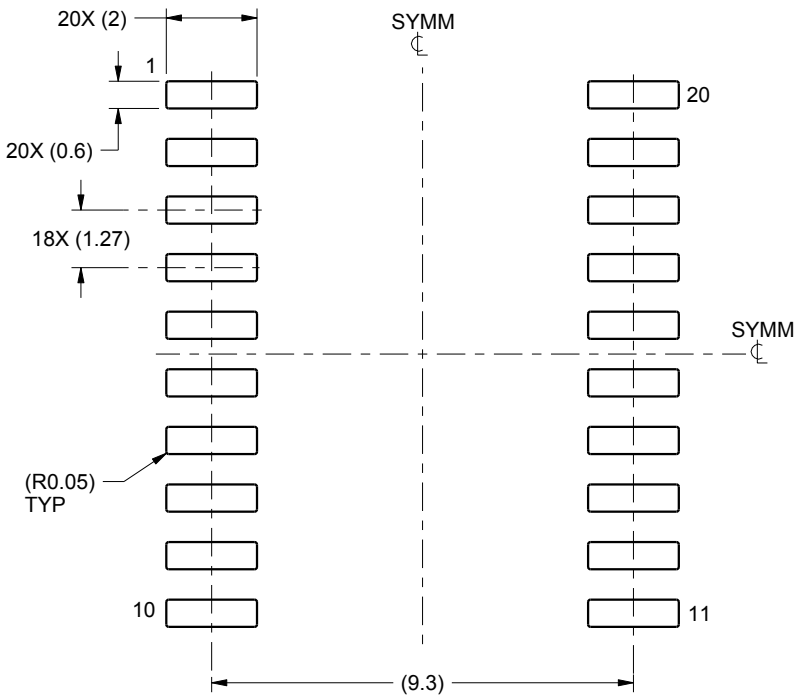
SOIC - 2.65 mm max height

SOIC

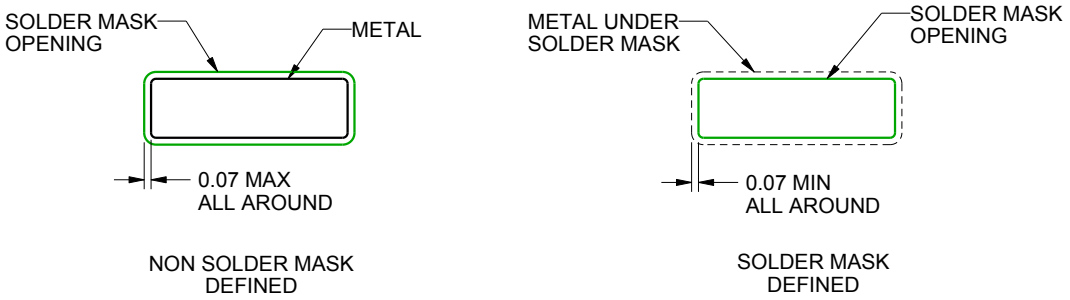


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

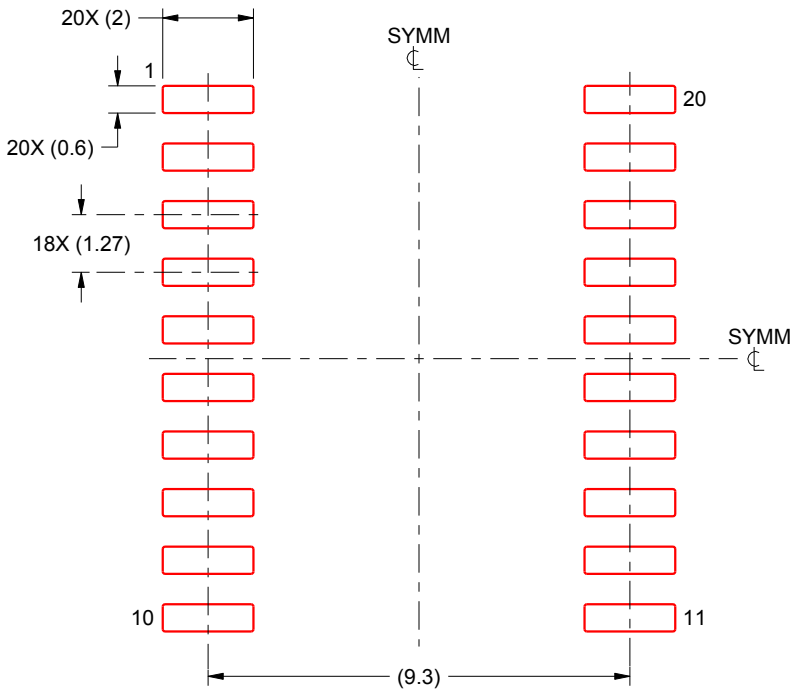


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

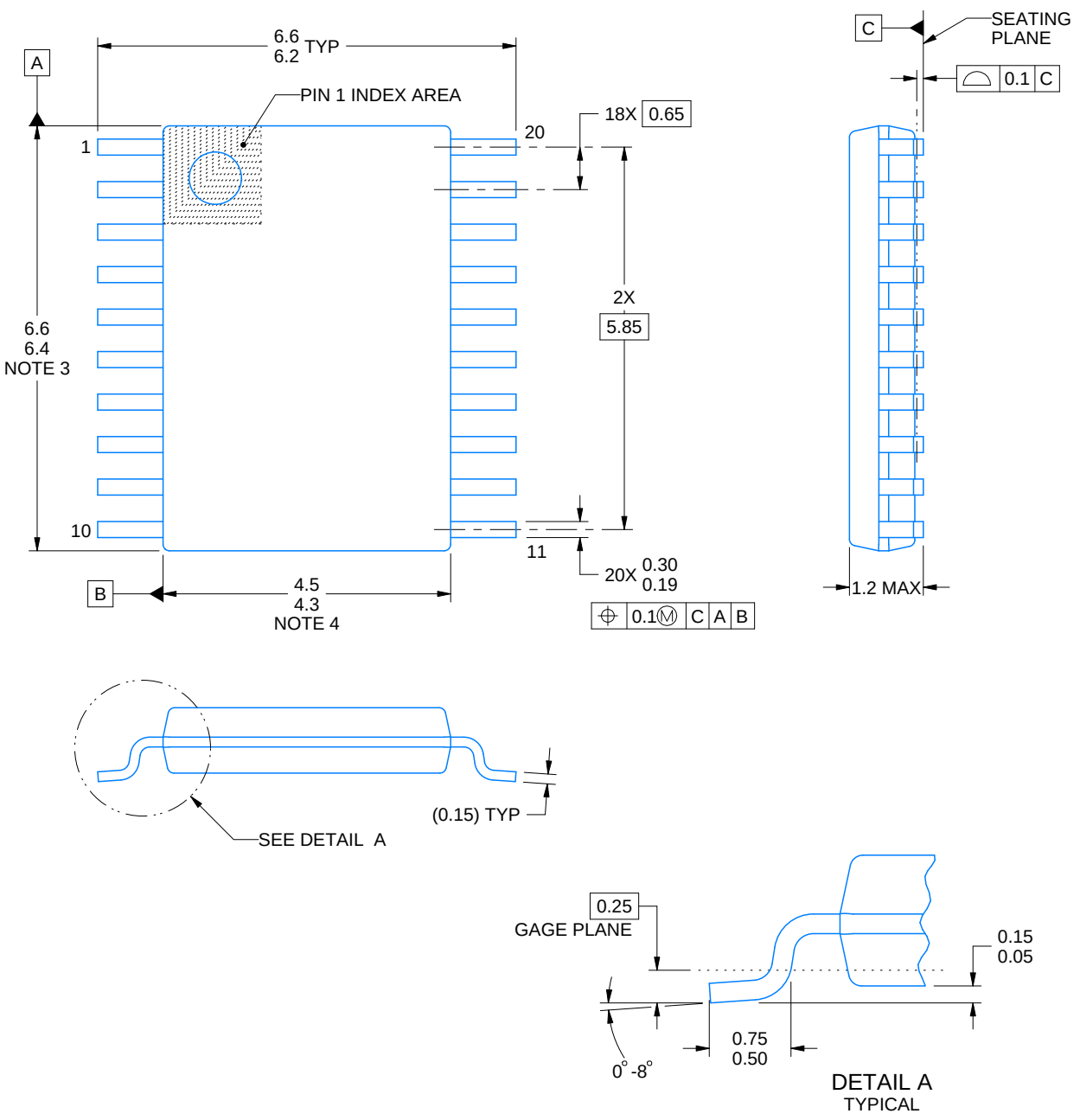
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

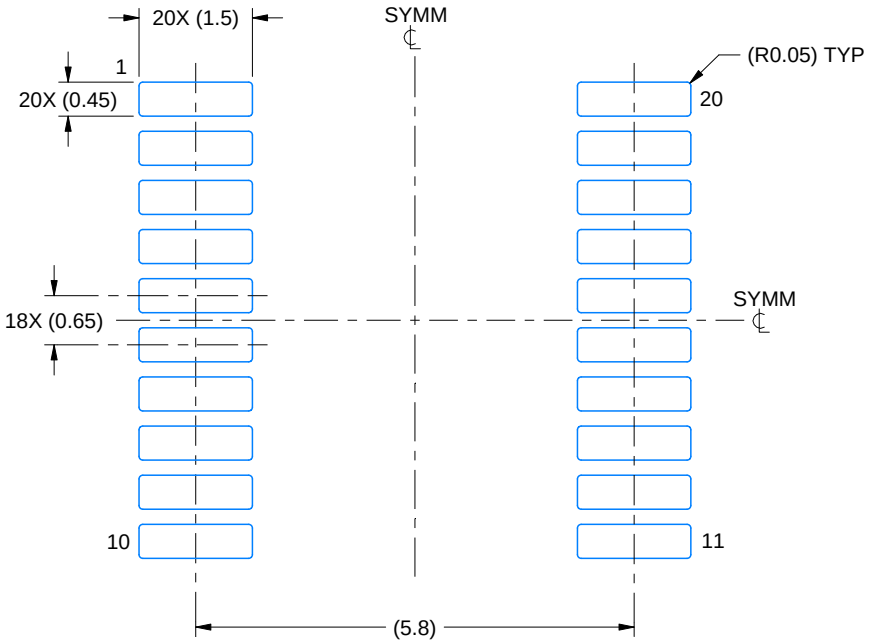
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



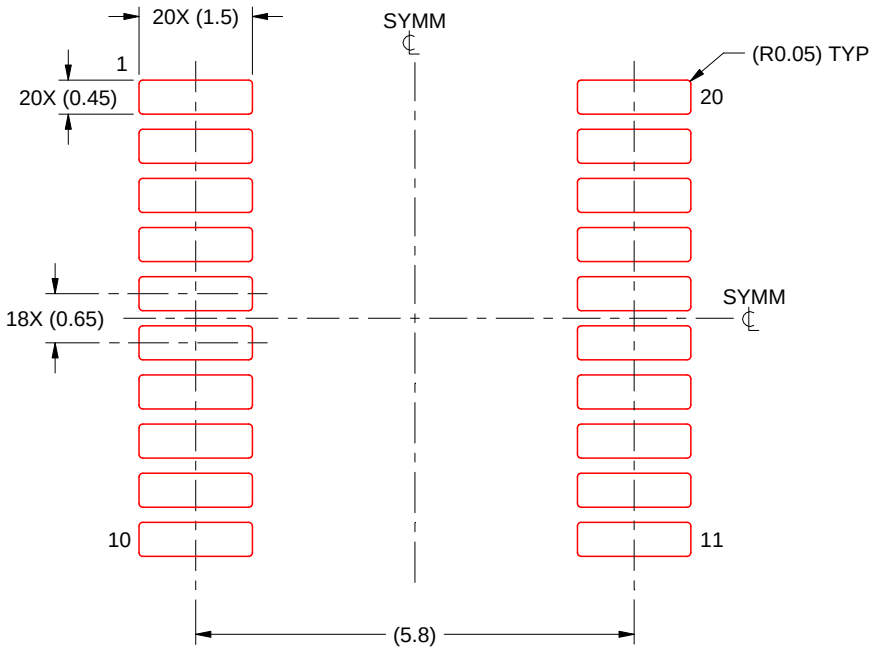
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



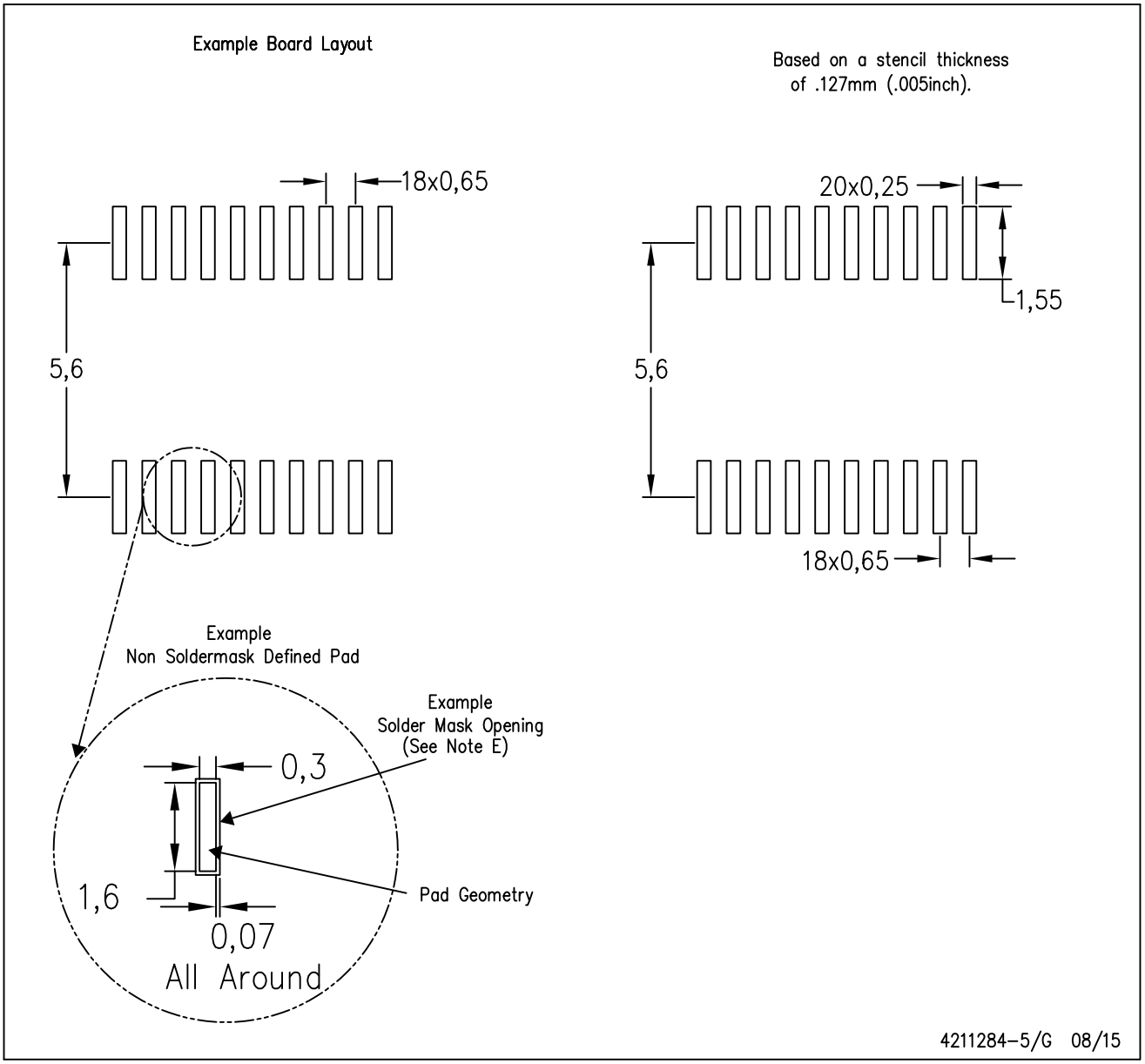
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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