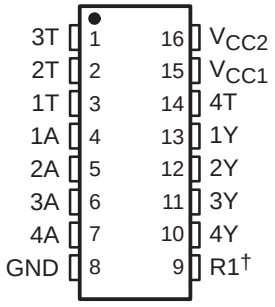
SLLS083B – NOVEMBER 1970 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28**
- **Input Resistance . . . 3 kΩ to 7 kΩ Over Full EIA/TIA-232-E Voltage Range**
- **Input Threshold Adjustable to Meet Fail-Safe Requirements Without Using External Components**
- **Built-In Hysteresis for Increased Noise Immunity**
- **Inverting Output Compatible With TTL**
- **Output With Active Pullup for Symmetrical Switching Speeds**
- **Standard Supply Voltages . . . 5 V or 12 V**

D OR N PACKAGE
(TOP VIEW)



† For function of R1, see schematic

description

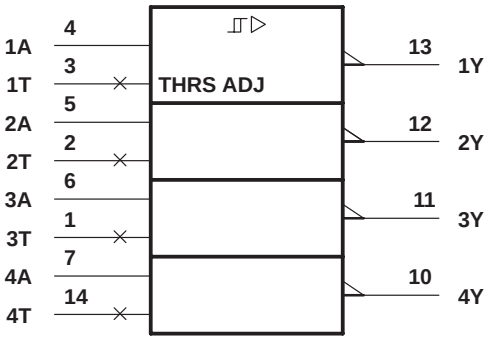
The SN75154 is a monolithic low-power Schottky line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI Standard EIA/TIA-232-E. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5-V supply; however, a built-in option allows operation from a 12-V supply without the use of additional components. The output is compatible with most TTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, even if power is being supplied via the alternate V_{CC2} terminal. This provides a wide hysteresis loop, which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

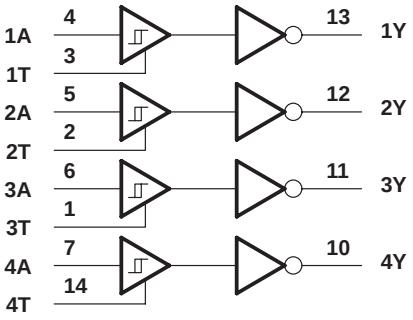
The SN75154 is characterized for operation from 0°C to 70°C.

logic symbol†

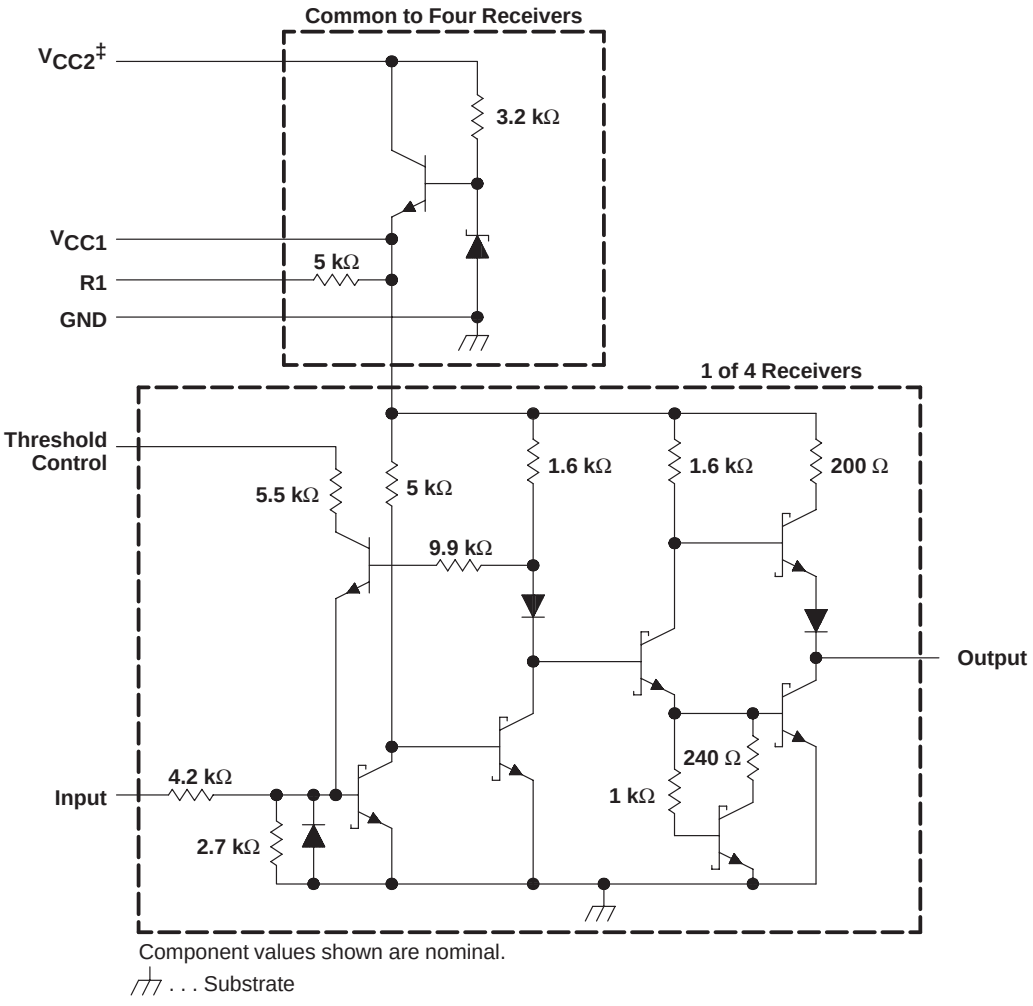


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic



Component values shown are nominal.

⏚ . . . Substrate

‡ When V_{CC1} is used, V_{CC2} may be left open or shorted to V_{CC1}. When V_{CC2} is used, V_{CC1} must be left open or connected to the threshold control pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Normal supply voltage, V_{CC1} (see Note 1) . . . . . 7 V
Alternate supply voltage, V_{CC2} . . . . . 14 V
Input voltage, V_I . . . . . ±25 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage, V_{CC1}	4.5	5	5.5	V
Alternate supply voltage, V_{CC2}	10.8	12	13.2	V
High-level input voltage, V_{IH} (see Note 2)	3		15	V
Low-level input voltage, V_{IL} (see Note 2)	–15		–3	V
High-level output current, I_{OH}			–400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

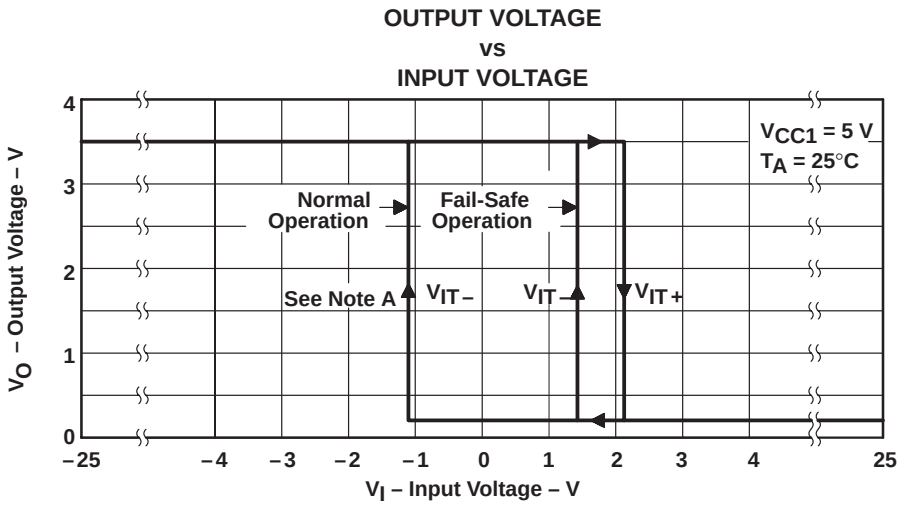
PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{IT-}	Negative-going input threshold voltage	Normal operation	1		–3	–1.1	0	V
		Fail-safe operation			0.8	1.4	3	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = –400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.29	0.4	V
r_i	Input resistance		2	ΔV_I = –25 V to –14 V	3	5	7	kΩ
				ΔV_I = –14 V to –3 V	3	5	7	
				ΔV_I = –3 V to 3 V	3	6	8	
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current‡		4	V_{CC1} = 5.5 V, V_I = –5 V	–10	–20	–40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

† All typical values are at V_{CC1} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	6	C_L = 50 pF, R_L = 390 Ω		11		ns
t_{PHL}	Propagation delay time, high- to low-level output				8		ns
t_{TLH}	Transition time, low- to high-level output				7		ns
t_{THL}	Transition time, high- to low-level output				2.2		ns

TYPICAL CHARACTERISTICS



NOTE A: For normal operation, the threshold controls are connected to V_{CC1}. For fail-safe operation, the threshold controls are open.

Figure 1

PARAMETER MEASUREMENT INFORMATION

dc test circuits†

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1}	V_{CC2}
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{IT+} min, V_{IT-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{IT+} min (normal)	V_{OH}	Note A	V_{CC1}	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	V_{CC1}	I_{OH}	T	13.2 V
V_{IL} max, V_{IT+} min (normal)	V_{OH}	–3 V	V_{CC1}	I_{OH}	5.5 V and T	Open
	V_{OH}	–3 V	V_{CC1}	I_{OH}	T	13.2 V
V_{IH} min, V_{IT+} max, V_{IT-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{IT+} max (normal)	V_{OL}	3 V	V_{CC1}	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	V_{CC1}	I_{OL}	T	10.8 V
V_{IT-} max (normal)	V_{OL}	Note B	V_{CC1}	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	V_{CC1}	I_{OL}	T	13.2 V

NOTES: A. Momentarily apply –5 V, then 0.8 V.
B. Momentarily apply 5 V, then GND.

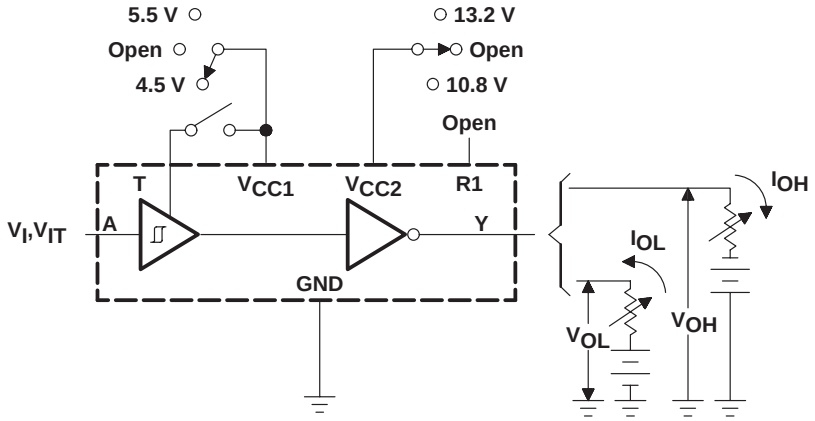
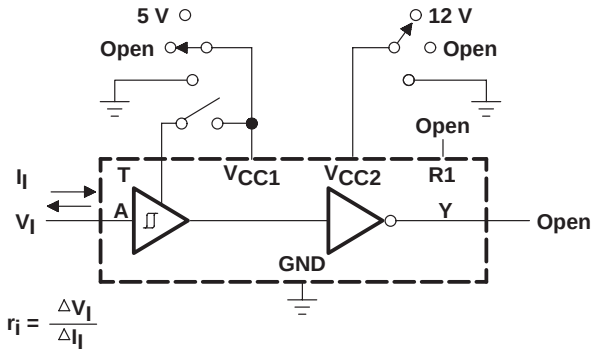


Figure 2. V_{IH}, V_{IL}, V_{IT+}, V_{IT-}, V_{OH}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

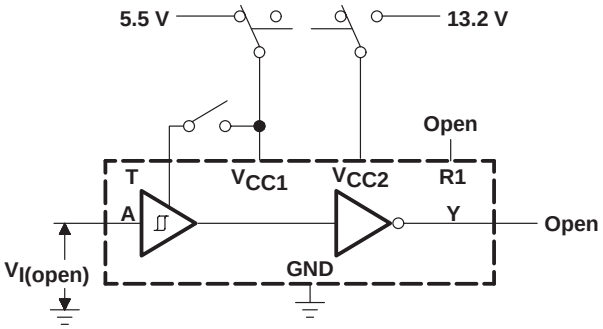
dc test circuits† (continued)



TEST TABLE

T	V_{CC1}	V_{CC2}
Open	5 V	Open
Open	GND	Open
Open	Open	Open
V_{CC1}	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
V_{CC1}	T	12 V
V_{CC1}	T	GND
V_{CC1}	T	Open

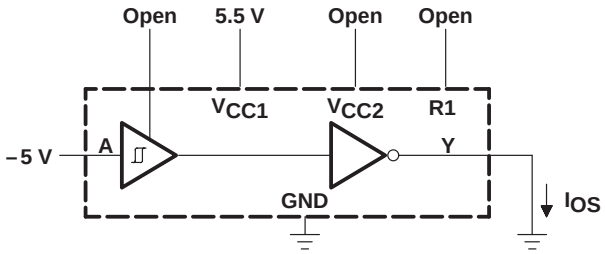
Figure 3. Input Resistance



TEST TABLE

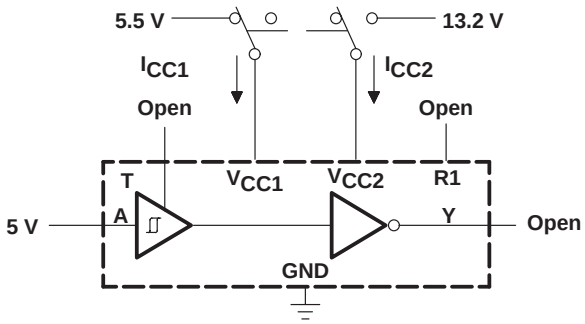
T	V_{CC1}	V_{CC2}
Open	5.5 V	Open
V_{CC1}	5.5 V	Open
Open	Open	13.2 V
V_{CC1}	T	13.2 V

Figure 4. Input Voltage (Open)



Each output is tested separately.

Figure 5. Output Short-Circuit Current

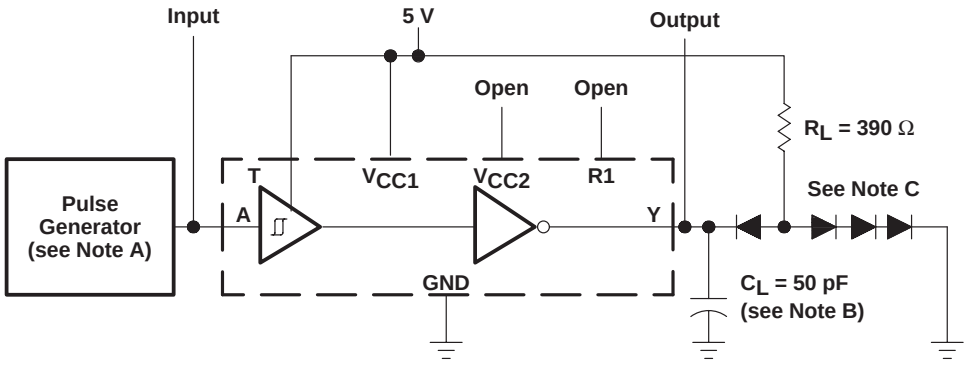


All four line receivers are tested simultaneously.

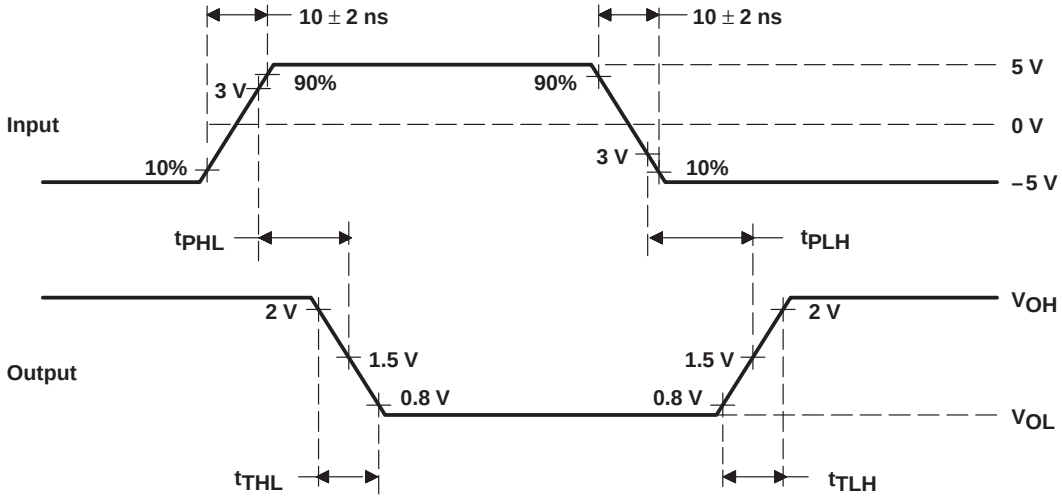
Figure 6. Supply Current

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, $t_W \leq$ 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

Figure 6. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75154D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples
SN75154DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples
SN75154N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75154N	Samples
SN75154NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

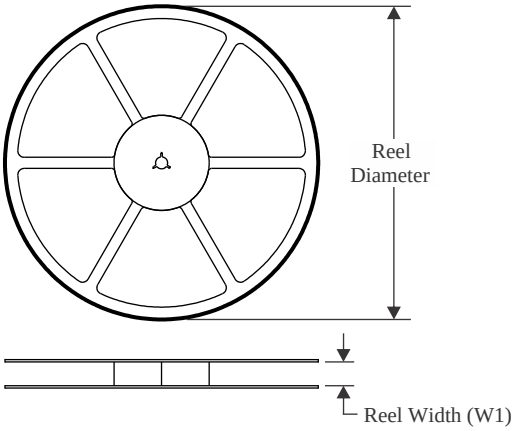
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

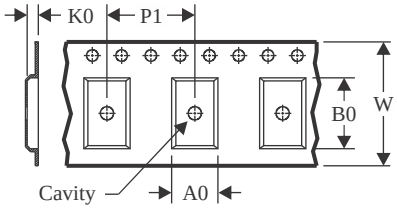
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

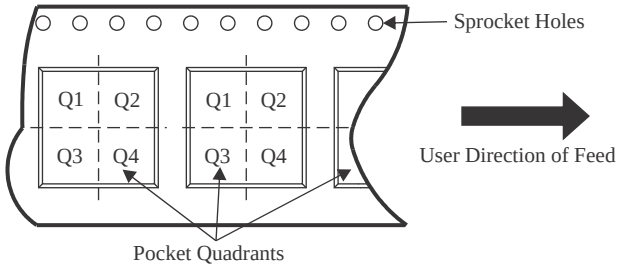


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

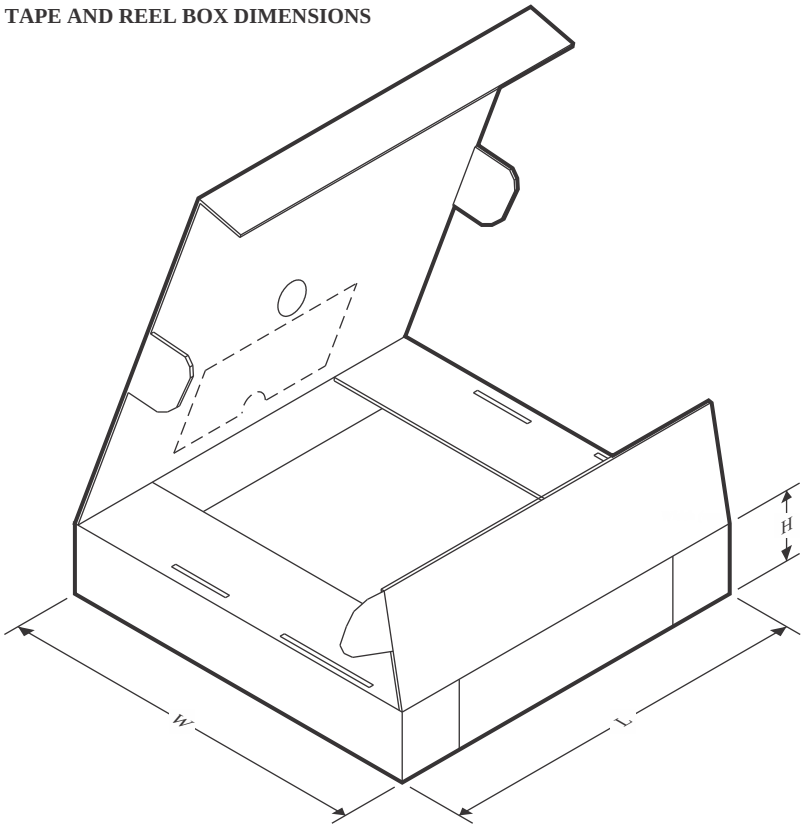
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75154DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75154NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

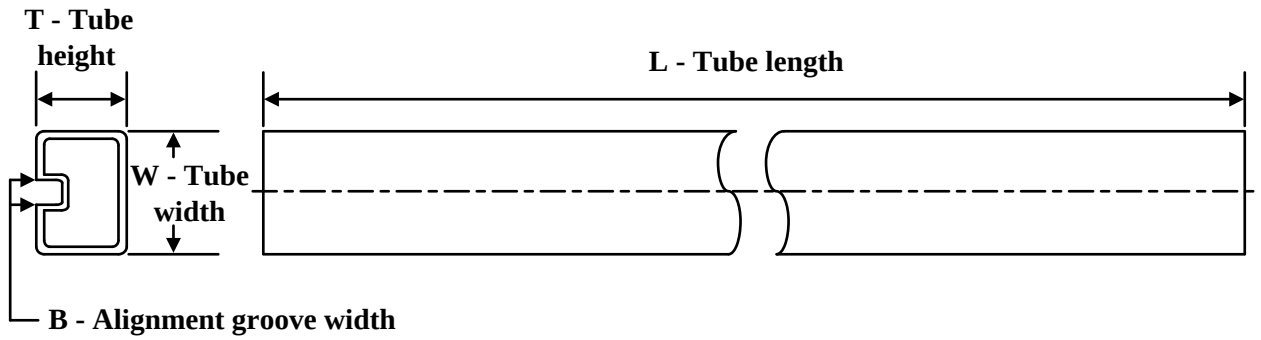
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

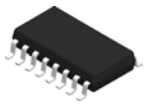
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75154DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75154NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75154D	D	SOIC	16	40	507	8	3940	4.32
SN75154N	N	PDIP	16	25	506	13.97	11230	4.32

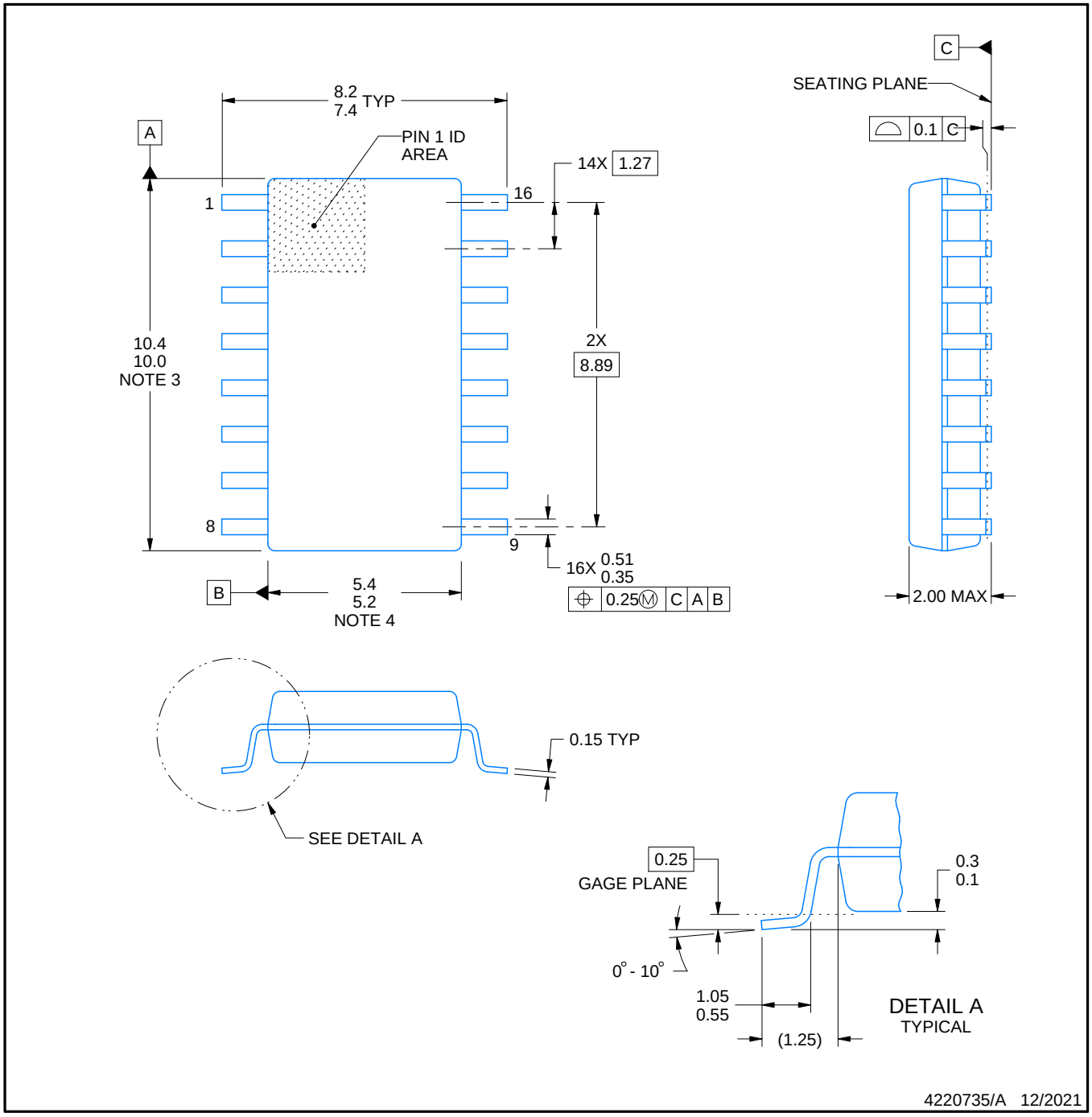


PACKAGE OUTLINE

NS0016A

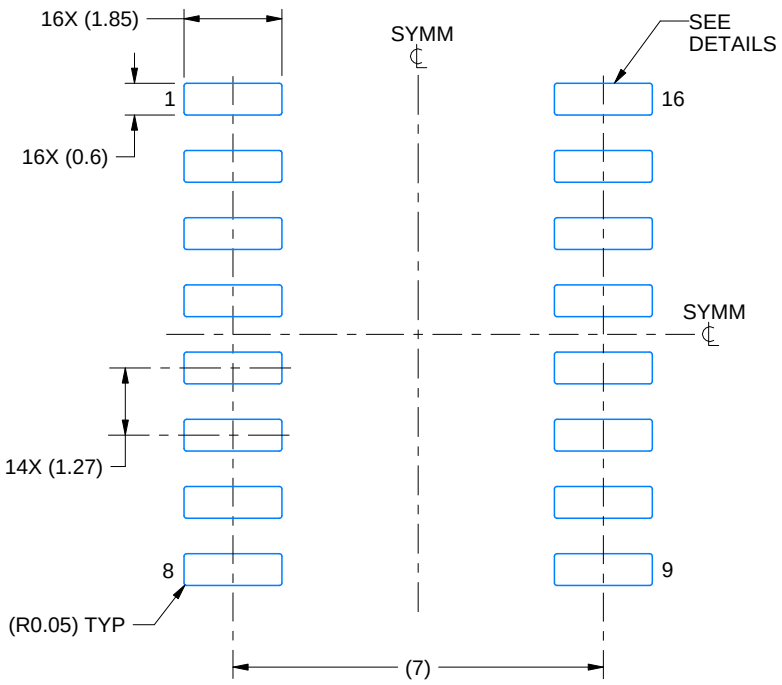
SOP - 2.00 mm max height

SOP

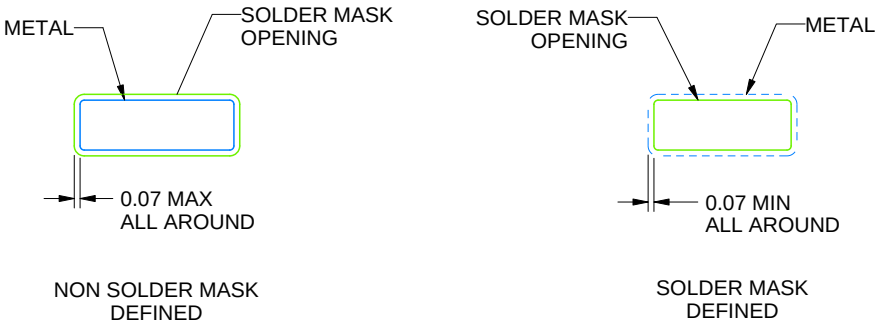


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

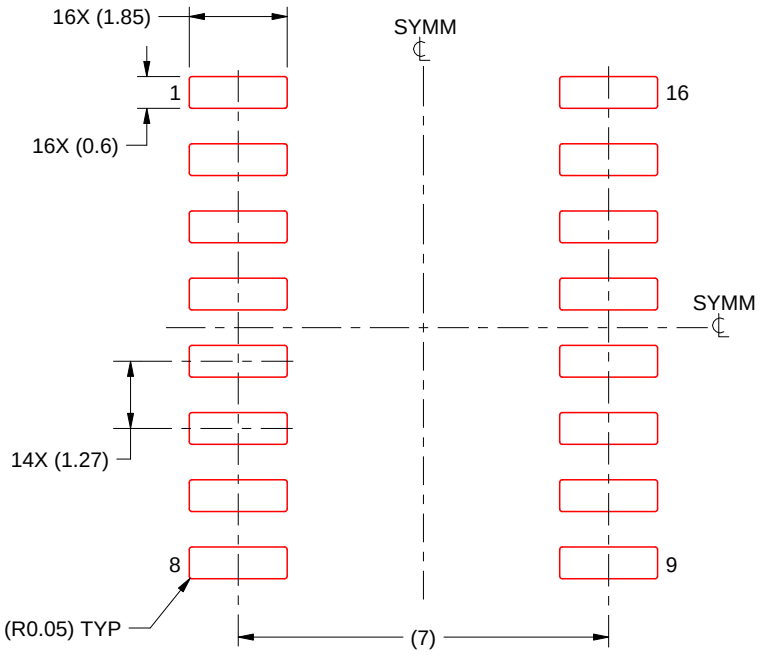
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



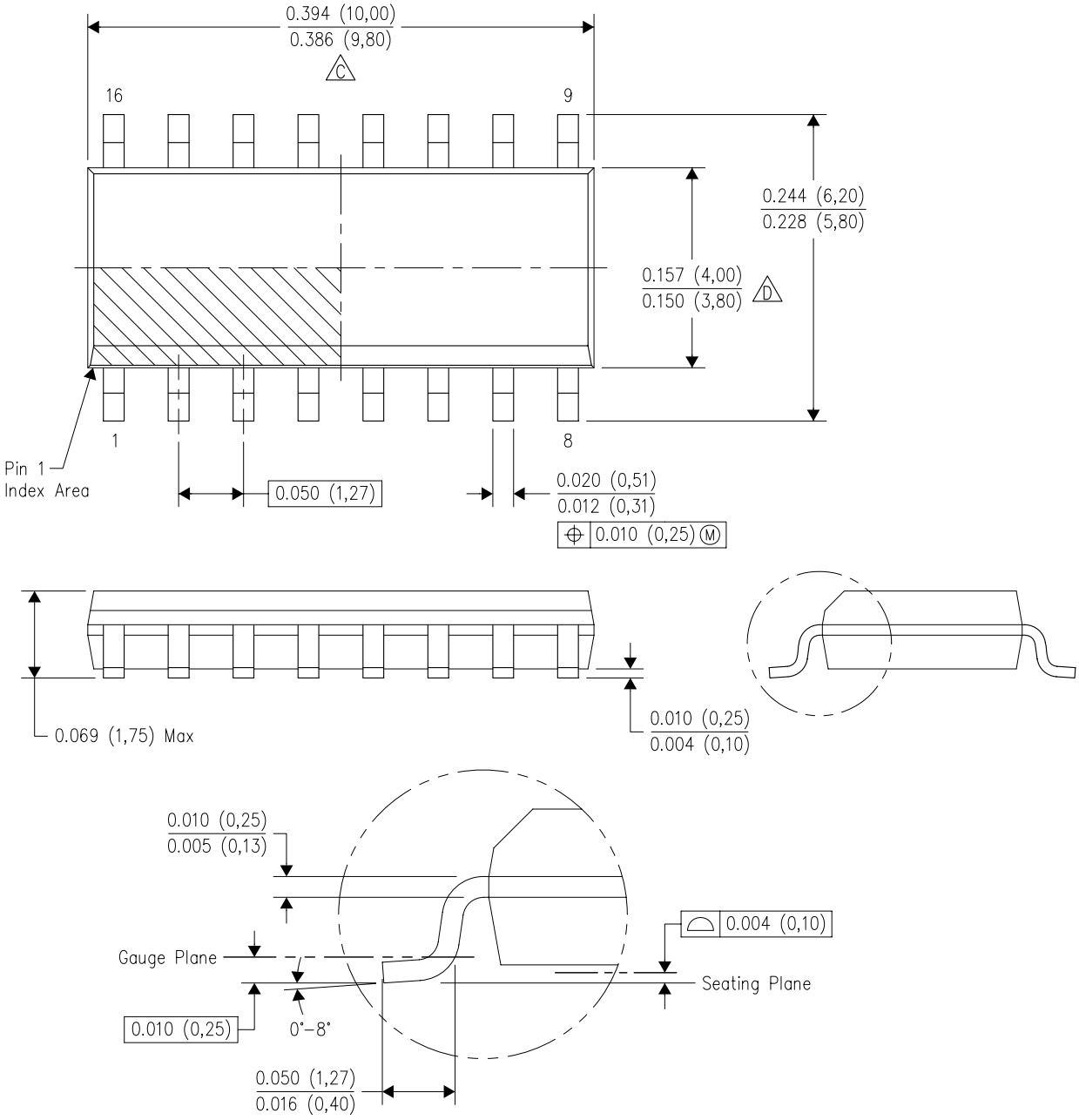
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

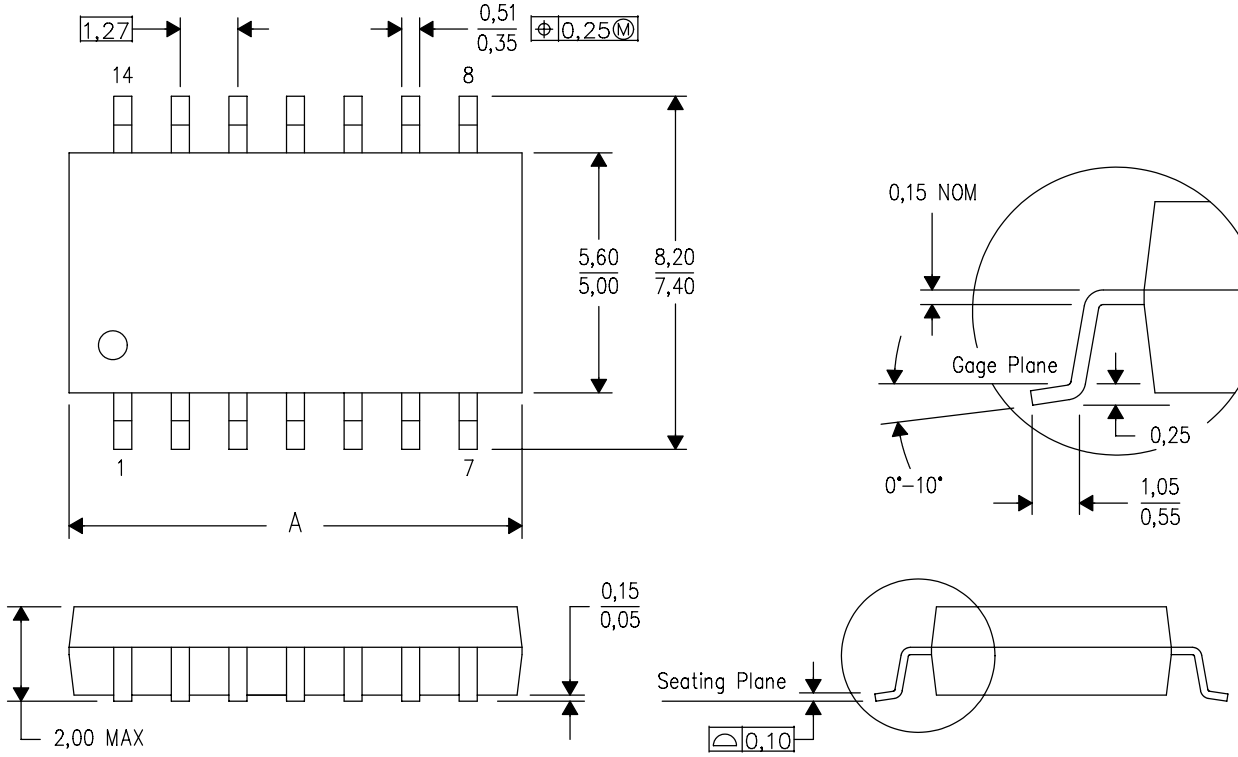


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

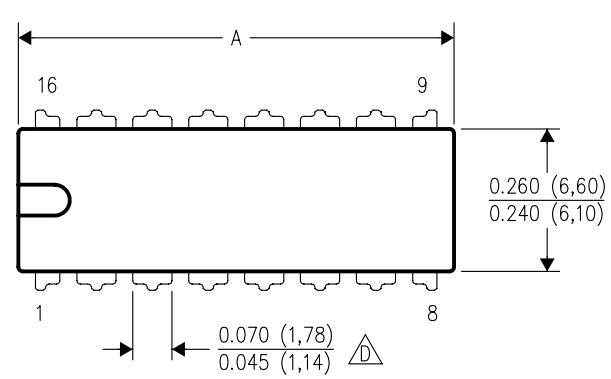
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

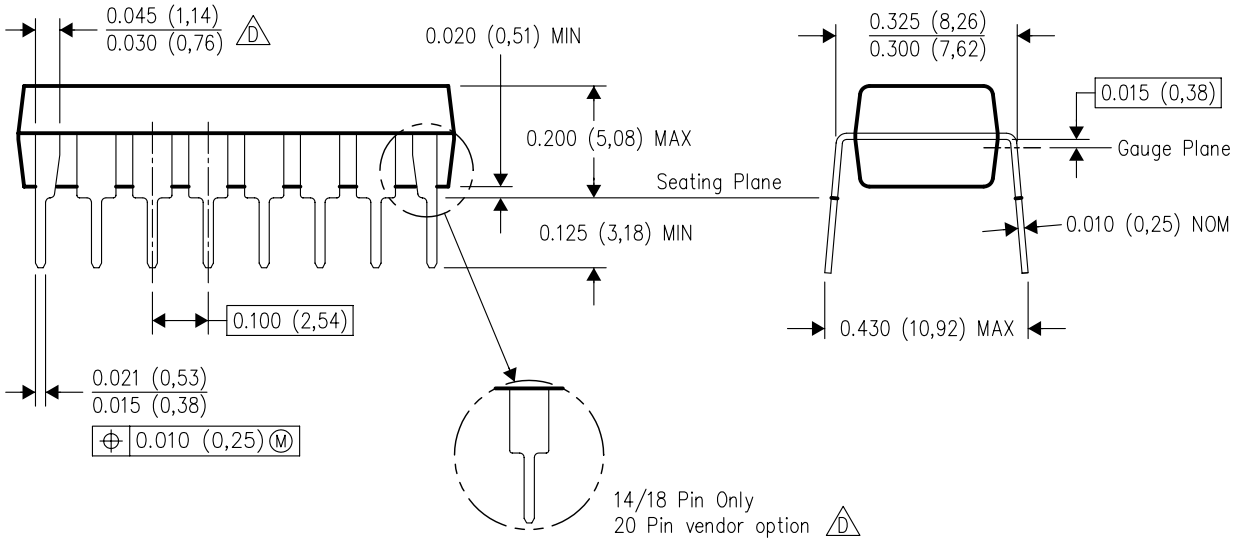
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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