

# TMAG5170D-Q1 Dual-Die High-Precision 3D Linear Hall-Effect Sensor With SPI

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 0:  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$
- High-precision linear 3D Hall-effect sensor to optimize position sensing speed and accuracy:
  - Conversion rate for single axis: 20 kSPS
- **Functional Safety-Compliant targeted:**
  - Developed for functional safety applications
  - [Documentation available to aid ISO 26262 system design up to ASIL D will be available upon production release](#)
- 10-MHz serial peripheral interface (SPI) with cyclic redundancy check (CRC)
- Built-in temperature sensor with  $< \pm 3^{\circ}\text{C}$  error
- Independently selectable X, Y, and Z ranges:
  - TMAG5170DA1-Q1:  $\pm 25, \pm 50, \pm 100$  mT
  - TMAG5170DA2-Q1:  $\pm 75, \pm 150, \pm 300$  mT
- Autonomous wake-up and sleep mode for threshold detection consuming only  $1.5 \mu\text{A}$
- $\overline{\text{ALERT}}$  function to initiate sensor conversion or indicate conversion complete
- Integrated temperature compensation for multiple magnet types
- Integrated angle CORDIC calculation with gain and offset adjustment
- Supply voltage range: 2.3 V to 5.5 V

## 2 Applications

- [Steering column control](#)
- [Steering wheel control](#)
- [Shifter systems](#)
- [Wiper modules](#)
- [Actuators](#)

## 3 Description

The TMAG5170D-Q1 is a dual-die high-precision linear 3D Hall-effect sensor designed for a wide range of automotive and industrial applications. The high level of integration offers flexibility and accuracy in a variety of position sensing systems. This device features 3 independent Hall sensors at X, Y, and Z axes.

A precision signal-chain along with an integrated 12-bit ADC enables high accuracy and low drift magnetic field measurements while supporting a sampling of up to 20 kSPS. On-chip temperature sensor data is available for system-level drift compensation.

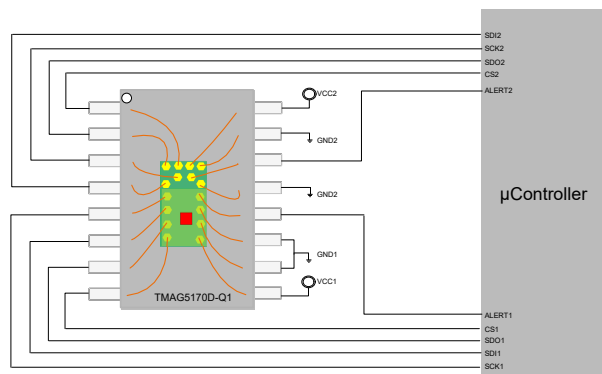
Integrated angle calculation engine (CORDIC) provides full  $360^{\circ}$  angular position information for both on-axis and off-axis angle measurement topologies. The angle calculation is performed using two user-selected magnetic axes. The device features magnetic gain and offset correction to mitigate the impact of system mechanical error sources.

The TMAG5170D-Q1 can be configured through the SPI to enable any combination of magnetic axes and temperature measurements. Multiple sensor conversion schemes and SPI read frames help optimize throughput and accuracy. A dedicated  $\overline{\text{ALERT}}$  pin can act as a system interrupt during low power wake-up and sleep mode, and can also be used by a microcontroller to trigger a new sensor conversion.

### Package Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMAG5170D-Q1	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Application Block Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2023	*	Initial Release

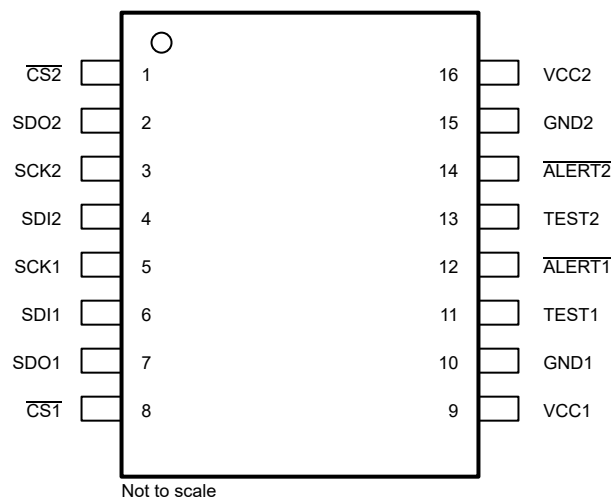
## 5 Description (continued)

The TMAG5170D-Q1 offers multiple diagnostics features to detect and report both system and device-level failures. The SPI communication features a user-enabled cyclic redundancy check to enhance the data integrity.

The device is offered in two different orderables to support wide magnetic fields ranges from  $\pm 25$  mT to  $\pm 300$  mT.

The device performs consistently across a wide ambient temperature range of  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ .

## 6 Pin Configuration and Functions



**Figure 6-1. PW Package 16-Pin TSSOP Top View**

**Table 6-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CS}}2$	I	Chip select, bottom die
2	SDO2	O	Serial data out, bottom die
3	SCK2	I	Serial clock, bottom die
4	SDI2	I	Serial data in, bottom die
5	SCK1	I	Serial clock, top die
6	SDI1	I	Serial data in, top die
7	SDO1	O	Serial data out, top die
8	$\overline{\text{CS}}1$	I	Chip select, top die
9	VCC1	P	Main power supply, top die. Handles 2.3-V to 5.5-V power supply input
10	GND1	G	Ground, top die
11	TEST1	I/O	Test input, top die, connect to ground
12	$\overline{\text{ALERT}}1$	I/O	Status output/Trigger, top die
13	TEST2	I/O	Test input, bottom die, connect to ground
14	$\overline{\text{ALERT}}2$	I/O	Status output/Trigger, bottom die
15	GND2	G	Ground, bottom die
16	VCC2	P	Main power supply, bottom die. Handles 2.3-V to 5.5-V power supply input

(1) I = input, O = output, I/O = input and output, G = ground, P = power

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Main supply voltage, VCC1, VCC2	-0.3	7	V
I <sub>OUT</sub>	Output current, SDO1, SDO2, $\overline{\text{ALERT1}}$ , $\overline{\text{ALERT2}}$	-10	10	mA
V <sub>OUT</sub>	Output voltage, SDO1, SDO2, $\overline{\text{ALERT1}}$ , $\overline{\text{ALERT2}}$	-0.3	7	V
V <sub>IN</sub>	Input voltage, SDI1, $\overline{\text{CS1}}$ , SCK1, SDI2, $\overline{\text{CS2}}$ , SCK2	-0.3	V <sub>VCC</sub> + 0.3	V
B <sub>MAX</sub>	Magnetic flux density		Unlimited	T
T <sub>J</sub>	Junction temperature	-40	170	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	
		CDM ESD classification level C4B	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMAG5170D-Q1	UNIT
		PW (16-TSSOP)	
		PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	106.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	33.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	63.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>VCC</sub>	Main supply voltage	2.3		5.5	V
I <sub>OUT</sub>	Output current, SDO1, SDO2	-2		2	mA
I <sub>OUT</sub>	Output current, $\overline{\text{ALERT1}}$ , $\overline{\text{ALERT2}}$	0		2	mA
V <sub>IH</sub>	Input HIGH voltage, SDI1, $\overline{\text{CS1}}$ , SCK1, SDI2, $\overline{\text{CS2}}$ , SCK2	0.75			V <sub>VCC</sub>
V <sub>IL</sub>	Input LOW voltage, SDI1, $\overline{\text{CS1}}$ , SCK1, $\overline{\text{ALERT1}}$ , SDI2, $\overline{\text{CS2}}$ , SCK2, $\overline{\text{ALERT2}}$			0.25	V <sub>VCC</sub>
t <sub>w_trigger</sub>	Pulse width for conversion trigger input signal	1		25	μs

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T <sub>A</sub>	Operating free air temperature	-40		150	C

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SDO, ALERT</b>						
V <sub>OH</sub>	Output HIGH voltage, SDOx pins	I <sub>OUT</sub> = -2 mA	V <sub>CC</sub> - 0.4		V <sub>CC</sub>	V
V <sub>OL</sub>	Output LOW voltage, SDOx pins	I <sub>OUT</sub> = -2 mA	0		0.4	V
V <sub>OL</sub>	Output LOW voltage, $\overline{\text{ALERTx}}$ pins	I <sub>OUT</sub> = -2 mA	0		0.4	V
t <sub>FALL_ALERT</sub>	$\overline{\text{ALERTx}}$ output fall time	R <sub>PU</sub> = 10 kΩ C <sub>L</sub> = 20 pF V <sub>CC</sub> = 2.3 V to 5.5 V		50		ns
t <sub>ALERT</sub>	$\overline{\text{ALERTx}}$ output pulse width with conversion complete or threshold cross interrupt event	ALERT_MODE = 0b Interrupt & Trigger Mode		5		μs
t <sub>ALERT</sub>	$\overline{\text{ALERTx}}$ output pulse width with other interrupt events	ALERT_MODE = 0b Interrupt & Trigger Mode		31		μs
I <sub>OZ</sub>	Output Leakage current, $\overline{\text{ALERTx}}$ pins	ALERT pin disabled V <sub>OZ</sub> = 5.5V	0	30		nA
<b>DC Power</b>						
V <sub>CC_PORRise</sub>	Power on reset voltage at VCCx ramping up			1.4		V
V <sub>CC_PORFall</sub>	Power off reset voltage at VCCx ramping down			1.2		V
V <sub>CC_UV</sub>	Under voltage threshold at VCCx			2.1		V
V <sub>CC_OV</sub>	Over voltage threshold at VCCx			5.9		V
I <sub>ACTIVE</sub>	Active mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high V <sub>CC</sub> = 2.3 V to 5.5 V		3.4		mA
I <sub>STDBY</sub>	Stand-by mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high V <sub>CC</sub> = 2.3 V to 5.5 V		0.8		mA
I <sub>CFG</sub>	Configuration mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high		0.06		mA
I <sub>SLP</sub>	Sleep mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high V <sub>CC</sub> = 2.3 V to 5.5 V T <sub>A</sub> = -40°C to 125°C		1.3		μA
I <sub>SLP</sub>	Sleep mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high V <sub>CC</sub> = 2.3 V to 5.5 V T <sub>A</sub> = -40°C to 125°C		1.3		μA
I <sub>DEEP_SLP</sub>	Deep sleep mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high V <sub>CC</sub> = 2.3 V to 5.5 V T <sub>A</sub> = -40°C to 125°C		5		nA

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Average Power</b>						
I <sub>CC_DCM</sub>	Duty-cycle mode current consumption for each die One channel enabled CONV_AVG = 000b	V <sub>CC</sub> = 5 V Data active rate 1000 Hz		245		μA
		V <sub>CC</sub> = 5 V Data active rate 100 Hz		32		μA
		V <sub>CC</sub> = 5 V Data active rate 10 Hz		4.5		μA
		V <sub>CC</sub> = 5 V Data active rate 1 Hz		1.5		μA
	Duty-cycle mode current consumption for each die Two channels enabled CONV_AVG = 000b	V <sub>CC</sub> = 5 V Data active rate 1000 Hz		292		μA
		V <sub>CC</sub> = 5 V Data active rate 100 Hz		39		μA
		V <sub>CC</sub> = 5 V Data active rate 10 Hz		5		μA
		V <sub>CC</sub> = 5 V Data active rate 1 Hz		1.6		μA
<b>Operating Speed</b>						
t <sub>ini_active</sub>	Initialization time during Active mode	OPERATING_MODE = 010b Time between trigger and conversion start		10		μs
t <sub>measure</sub>	Conversion time <sup>(1)</sup>	CONV_AVG = 000b OPERATING_MODE = 010b One channel enabled <sup>(2)</sup>		45		μs
t <sub>measure</sub>	Conversion time <sup>(1)</sup>	CONV_AVG = 101b OPERATING_MODE = 010b One channel enabled <sup>(2)</sup>		820		μs
t <sub>measure</sub>	Conversion time <sup>(1)</sup>	CONV_AVG = 000b OPERATING_MODE = 010b One channel enabled <sup>(2)</sup>		50		μs
		CONV_AVG = 101b OPERATING_MODE = 010b One channel enabled <sup>(3)</sup>		825		μs
f <sub>HFOSC</sub>	Internal high-frequency oscillator speed			3.2		MHz
f <sub>LFOSC</sub>	Internal low-frequency oscillator speed			16		KHz
<b>Temperature Sensing</b>						
T <sub>SENS_RANGE</sub>	Temperature sensing range		-40		170	°C
T <sub>SENS_T0</sub>	Reference temperature for TADC <sub>T0</sub>		23	25	27	°C
TADC <sub>T0</sub>	TEMP_RESULT decimal value @ T <sub>SENS_T0</sub>			17522		
TADC <sub>RES</sub>	Temp sensing resolution			60.0		LSB/°C
NRMS (T)	RMS (1 Sigma) temperature noise	CONV_AVG = 101b		0.06		°C
NRMS (T)	RMS (1 Sigma) temperature noise	CONV_AVG = 000b		0.35		°C
<b>Sensor Location</b>						
d <sub>s1_s2</sub>	Sensor displacement in the X and Y plane			25		μm
A <sub>s1_s2</sub>	Relative angular rotation between top and bottom sensor in degree			1		o

- (1) To calculate the time between conversion request and the availability of the conversion result, add the initialization time to the t<sub>measure</sub> as explained in Comparing Operating Modes Table. For continuous conversion, the initialization time is applicable only for the first conversion.
- (2) Add 25μs for each additional channel enabled for conversion with CONV\_AVG =000.

- (3) For conversion with CONV\_AVG = 101, each axis data is collected 32 times. If an additional channel is enabled with CONV\_AVG = 101, add  $32 \times 25\mu\text{s} = 800\mu\text{s}$  to the  $t_{\text{measure}}$  to calculate the conversion time for two axes.

## 7.6 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>TMAG5170A1</b>							
B <sub>RANGE</sub>	Linear magnetic range	x_RANGE <sup>(1)</sup> = 00b			±50		mT
		x_RANGE <sup>(1)</sup> = 01b			±25		mT
		x_RANGE <sup>(1)</sup> = 10b			±100		mT
SENS	Sensitivity	x_RANGE <sup>(1)</sup> = 00b			654		LSB/mT
		x_RANGE <sup>(1)</sup> = 01b			1308		LSB/mT
		x_RANGE <sup>(1)</sup> = 10b			326		LSB/mT
SENS <sub>ERR</sub>	Sensitivity error	X, Y, or Z axis T <sub>A</sub> = 25°C	B <sub>RANGE</sub> = 25 mT, 50 mT		±0.5%		
			B <sub>RANGE</sub> = 100 mT		±0.5%		
SENS <sub>ERR_DRI</sub> FT	Sensitivity Drift from T <sub>A</sub> = 25°C value	X, Y, or Z axis B <sub>RANGE</sub> = 25 mT, 50 mT	MAG_TEMP <sub>CO</sub> = 00b T <sub>A</sub> = 25°C to 125°C		±0.9%		
			MAG_TEMP <sub>CO</sub> = 00b T <sub>A</sub> = -40°C to 25°C		±1.2%		
			MAG_TEMP <sub>CO</sub> = 01b, 10b, 11b T <sub>A</sub> = -40°C to 125°C		±1.2%		
	Sensitivity Drift from T <sub>A</sub> = 25°C value	X, Y, or Z axis B <sub>RANGE</sub> = 100 mT	T <sub>A</sub> = 25°C to 125°C		±1.0%		
			T <sub>A</sub> = -40°C to 25°C		±1.2%		
SENS <sub>LT_DRIFT</sub>	Sensitivity Lifetime drift	X, Y, Z axes			±0.5%		
SENS <sub>LE</sub>	Sensitivity Linearity Error	T <sub>A</sub> = 25°C	X, Y axes		±0.1%		
			Z axis		±0.05%		
SENS <sub>MIS</sub>	Sensitivity mismatch	T <sub>A</sub> = 25°C	X-Y axes		±0.02%		
			Y-Z axes		±0.17%		
			X-Z axes		±0.15%		
SENS <sub>MIS_DRIF</sub> T	Sensitivity mismatch drift from 25°C value	X-Y axes	T <sub>A</sub> = 25°C to 125°C		±0.8%		
			T <sub>A</sub> = -40°C to 25°C		±0.5%		
		Y-Z axes	T <sub>A</sub> = 25°C to 125°C		±0.7%		
			T <sub>A</sub> = -40°C to 25°C		±0.5%		
X-Z axes	T <sub>A</sub> = 25°C to 125°C		±1.4%				
	T <sub>A</sub> = -40°C to 25°C		±0.1%				
B <sub>OFFSET</sub>	Magnetic Offset	X, Y, or Z axis B <sub>RANGE</sub> = 25 mT, 50 mT	T <sub>A</sub> = 25°C		±10		μT
		X, Y, or Z axis B <sub>RANGE</sub> = 100 mT	T <sub>A</sub> = 25°C		±150		μT
B <sub>OFFSET_DRIFT</sub>	Offset drift from T <sub>A</sub> = 25°C value	X or Y axis	T <sub>A</sub> = 25°C to 125°C		±1.0		μT/°C
		Z axis	T <sub>A</sub> = 25°C to 125°C		±0.50		μT/°C
		X or Y axis	T <sub>A</sub> = -40°C to 25°C		±1.5		μT/°C
		Z axis	T <sub>A</sub> = -40°C to 25°C		±1.0		μT/°C
B <sub>OFFSET_LT_D</sub> RIFT	Offset Lifetime drift				±50		μT
					±50		μT

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
B <sub>N,RMS</sub>	RMS (1 Sigma) magnetic noise	X or Y axis	x_RANGE <sup>(1)</sup> = 00b CONV_AVG = 000b T <sub>A</sub> = 25°C		140		μT
			x_RANGE <sup>(1)</sup> = 00b CONV_AVG = 000b T <sub>A</sub> = 125°C		170		μT
			x_RANGE <sup>(1)</sup> = 00b CONV_AVG = 101b T <sub>A</sub> = 25°C		24		μT
			x_RANGE <sup>(1)</sup> = 00b CONV_AVG = 101b T <sub>A</sub> = 125°C		30		μT
		Z axis	Z_RANGE <sup>(1)</sup> = 00b CONV_AVG = 000b T <sub>A</sub> = 25°C		61		μT
			Z_RANGE <sup>(1)</sup> = 00b CONV_AVG = 000b T <sub>A</sub> = 125°C		70		μT
			Z_RANGE <sup>(1)</sup> = 00b CONV_AVG = 101b T <sub>A</sub> = 25°C		11		μT
			Z_RANGE <sup>(1)</sup> = 00b CONV_AVG = 101b T <sub>A</sub> = 125°C		13		μT
ANG <sub>ERR</sub>	Angle drift from T <sub>A</sub> = 25°C value in full 360 degree rotation	Y-Z axes			±0.5		°
	Angle drift from T <sub>A</sub> = 25°C value in full 360 degree rotation	X-Z axes	RANGE - 10 CONV_AVG = 101b		±0.5		°
	Angle drift from T <sub>A</sub> = 25°C value in full 360 degree rotation	X-Y axes			±0.25		°
<b>TMAG5170A2</b>							
B <sub>RANGE</sub>	Linear magnetic range	x_RANGE <sup>(1)</sup> = 00b			±150		mT
		x_RANGE <sup>(1)</sup> = 01b			±75		mT
		x_RANGE <sup>(1)</sup> = 10b			±300		mT
SENS	Sensitivity	X, Y, or Z axis	x_RANGE <sup>(1)</sup> = 00b		218		LSB/mT
			x_RANGE <sup>(1)</sup> = 01b		436		LSB/mT
			x_RANGE <sup>(1)</sup> = 10b		108		LSB/mT
SENS <sub>ERR</sub>	Sensitivity error	X, Y, or Z axis T <sub>A</sub> = 25°C	B <sub>RANGE</sub> = 75 mT, 150 mT		±1.0%		
	Sensitivity error		B <sub>RANGE</sub> = 300 mT		±1.0%		
SENS <sub>ERR_DRI</sub> FT	Sensitivity Drift from T <sub>A</sub> = 25°C value	X, Y, or Z axis B <sub>RANGE</sub> = 75 mT, 150 mT	T <sub>A</sub> = -40°C to 125°C		±0.5%	±4.5%	
			T <sub>A</sub> = 25°C to 125°C		±0.5%	±4.0%	
		X, Y, or Z axis B <sub>RANGE</sub> = 300 mT	T <sub>A</sub> = -40°C to 25°C		±1.6%	±6.2%	
SENS <sub>LE</sub>	Sensitivity Linearity Error	T <sub>A</sub> = 25°C	X, Y axes		±0.1%		
			Z axis		±0.1%		
SENS <sub>LT_DRIFT</sub>	Sensitivity Lifetime drift	X, Y, Z axes			±0.6%		



over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SENS <sub>MIS</sub>	Sensitivity mismatch	X-Y axes T <sub>A</sub> = 25°C	B <sub>RANGE</sub> = 75 mT, 150 mT		±0.37%		
			B <sub>RANGE</sub> = 300 mT		±0.42%		
		Y-Z axes T <sub>A</sub> = 25°C	B <sub>RANGE</sub> = 75 mT, 150 mT		±0.41%		
			B <sub>RANGE</sub> = 300 mT		±0.37%		
		X-Z axes T <sub>A</sub> = 25°C	B <sub>RANGE</sub> = 75 mT, 150 mT		±0.38%		
			B <sub>RANGE</sub> = 300 mT		±1.2%		
SENS <sub>MIS_DRIFT</sub>	Sensitivity mismatch drift from T <sub>A</sub> = 25°C value	X-Y axes	T <sub>A</sub> = -40°C to 125°C B <sub>RANGE</sub> = 75 mT, 150 mT		±0.5%	±4.0%	
			T <sub>A</sub> = 25°C to 125°C B <sub>RANGE</sub> = 300 mT		±0.5%	±5.2%	
			T <sub>A</sub> = -40°C to 25°C B <sub>RANGE</sub> = 300 mT		±0.9%	±7.6%	
		Y-Z axes	T <sub>A</sub> = -40°C to 125°C B <sub>RANGE</sub> = 75 mT, 150 mT		±0.4%	±4.0%	
			T <sub>A</sub> = 25°C to 125°C B <sub>RANGE</sub> = 300 mT		±0.2%	±5.4%	
			T <sub>A</sub> = -40°C to 25°C B <sub>RANGE</sub> = 300 mT		±0.5%	±8.1%	
		X-Z axes	T <sub>A</sub> = -40°C to 125°C B <sub>RANGE</sub> = 75 mT, 150 mT		±0.2%	±5.5%	
			T <sub>A</sub> = -40°C to 125°C B <sub>RANGE</sub> = 300 mT		±1.1%	±6.6%	
B <sub>OFFSET</sub>	Magnetic offset	T <sub>A</sub> = 25°C	B <sub>RANGE</sub> = 75 mT, 150 mT		±50		μT
	Magnetic offset		B <sub>RANGE</sub> = 300 mT		±300		μT
B <sub>OFFSET_DRIFT</sub>	Offset drift from value at T <sub>A</sub> = 25°C	T <sub>A</sub> = 25°C to 125°C	X or Y axis B <sub>RANGE</sub> = 75 mt, 150 mT		±1.0		μT/°C
			Z axis B <sub>RANGE</sub> = 75 mt, 150 mT		±1.5		μT/°C
		T <sub>A</sub> = -40°C to 25°C	X or Y axis B <sub>RANGE</sub> = 75 mt, 150 mT		±3.5		μT/°C
			Z axis B <sub>RANGE</sub> = 75 mt, 150 mT		-0.4	±5.0	μT/°C
		T <sub>A</sub> = -40°C to 125°C	X, Y, or Z axis B <sub>RANGE</sub> = 300 mT		±2.5	±12.0	μT/°C
		B <sub>OFFSET_LT_DRIFT</sub>	Offset Lifetime drift			±50	

**ADVANCE INFORMATION**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
B <sub>N,RMS</sub>	RMS (1 Sigma) magnetic noise	X or Y axis x_RANGE <sup>(1)</sup> = 00b XONV_AVG = 000b	T <sub>A</sub> = 25°C		160		μT
			T <sub>A</sub> = 125°C		193		μT
		X or Y axis x_RANGE <sup>(1)</sup> = 00b XONV_AVG = 101b	T <sub>A</sub> = 25°C		28		μT
			T <sub>A</sub> = 125°C		34		μT
		Z axis Z_RANGE <sup>(1)</sup> = 00b XONV_AVG = 000b	T <sub>A</sub> = 25°C		72		μT
			T <sub>A</sub> = 125°C		84		μT
Z axis Z_RANGE <sup>(1)</sup> = 00b XONV_AVG = 101b	T <sub>A</sub> = 25°C		13		μT		
	T <sub>A</sub> = -40°C to 125°C		15		μT		
ANG <sub>ERR</sub>	Angle drift from T <sub>A</sub> = 25°C value in full 360 degree rotation	Y-Z axes			±0.5		Degree
	Angle drift from T <sub>A</sub> = 25°C value in full 360 degree rotation	X-Z axes	RANGE - 10 CONV_AVG = 101b		±0.5		Degree
	Angle drift from T <sub>A</sub> = 25°C value in full 360 degree rotation	X-Y axes			±0.25		Degree

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>TEMPERATURE COMPENSATION</b>							
STC	Temperature compensation (no compensation)	MAG_TEMPCO =00b	MAG_TEMPCO =00b		0		%/°C
STC	Temperature compensation (for NdBFe magnet)	MAG_TEMPCO =01b	MAG_TEMPCO =01b		0.12		%/°C
STC	Temperature compensation (for SmCo magnet)	MAG_TEMPCO =10b	MAG_TEMPCO =10b		0.03		%/°C
STC	Temperature compensation (for Ceramic magnet)	MAG_TEMPCO =11b	MAG_TEMPCO =11b		0.2		%/°C

(1) x\_RANGE denotes the X\_RANGE, Y\_RANGE, or Z\_RANGE register bits

## 7.7 Power up Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>V<sub>CC</sub> = 5.5 V</b>						
t <sub>start_power_up</sub>	Time to start up after V <sub>VCC</sub> supply voltage crossing V <sub>VCC_MIN</sub>			246		μs
t <sub>start_sleep</sub>	Time to activate from sleep mode			40		μs
t <sub>go_sleep</sub>	Time to go into sleep mode after $\overline{CS}$ goes high			50		μs
t <sub>start_deep_sleep</sub>	Time to start up from deep sleep mode			246		μs
t <sub>start_deep_sleep</sub>	Time to go into deep sleep mode after $\overline{CS}$ goes high			75		μs
t <sub>stand_by</sub>	Time to go to Stand-by mode from Configuration mode			90		μs
t <sub>spi_sleep</sub>	Setup time between $\overline{CS}$ going low and SCK start during sleep mode			8		μs
<b>V<sub>CC</sub> =2.3 V</b>						
t <sub>start_power_up</sub>	Time to start up after V <sub>CC</sub> supply voltage crossing V <sub>CC_MIN</sub>			260		μs
t <sub>start_sleep</sub>	Time to activate from sleep mode			40		μs
t <sub>go_sleep</sub>	Time to go into sleep mode after $\overline{CS}$ goes high			60		μs
t <sub>start_deep_sleep</sub>	Time to start up from deep sleep mode			260		μs
t <sub>start_deep_sleep</sub>	Time to go into deep sleep mode after $\overline{CS}$ goes high			75		μs
t <sub>stand_by</sub>	Time to go to Stand-by mode from Configuration mode			90		μs
t <sub>spi_sleep</sub>	Delay time between $\overline{CS}$ going low and SCK start during sleep mode			8		μs

## 7.8 SPI Interface Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SPI Interface</b>						
f <sub>SPI</sub>	SPI clock (SCK) frequency	LOAD = 25 pF			10	MHz
t <sub>whigh</sub>	High time: SCK logic high time duration		45			ns
t <sub>wlow</sub>	Low time: SCK logic low time duration		45			ns
t <sub>su_cs</sub>	$\overline{CS}$ setup time: Time delay between falling edge of $\overline{CS}$ and rising edge of SCK		45			ns
t <sub>h_cs</sub>	Hold time: Time between the falling edge of SCK and rising edge of $\overline{CS}$		45			ns
t <sub>pd_soen</sub>	Delay time: Time delay from falling edge of $\overline{CS}$ to data valid at SDO				45	ns
t <sub>pd_sodis</sub>	Delay time: Time delay from rising edge of $\overline{CS}$ to SDO transition to tristate				55	ns

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su\_si}$	SDI setup time: Setup time of SDI before the rising edge of SCK		25			ns
$t_{h\_si}$	Hold time: Time between the rising edge of SCK to SDI valid		25			ns
$t_{pd\_so}$	Propagation delay from falling edge of SCK to SDO				45	ns
$t_{w\_cs}$	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high.	LOAD = 25 pF	100			ns
$t_{spi\_sleep}$	Setup time between $\overline{CS}$ going low and SCK start during sleep mode			8	10	$\mu$ s

## 7.9 Typical Characteristics

ADVANCE INFORMATION

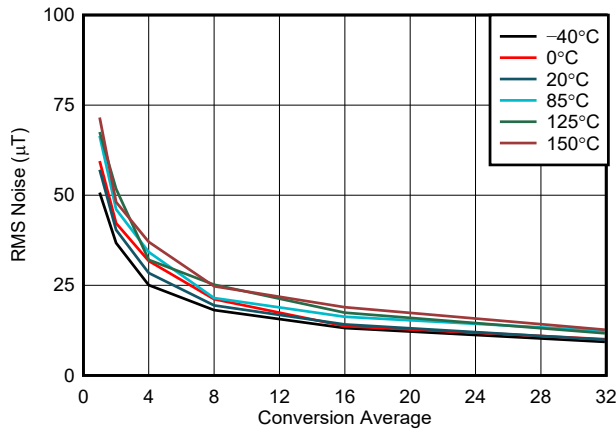


Figure 7-1. Z-Axis Noise vs Conversion Average, 25-mT Range

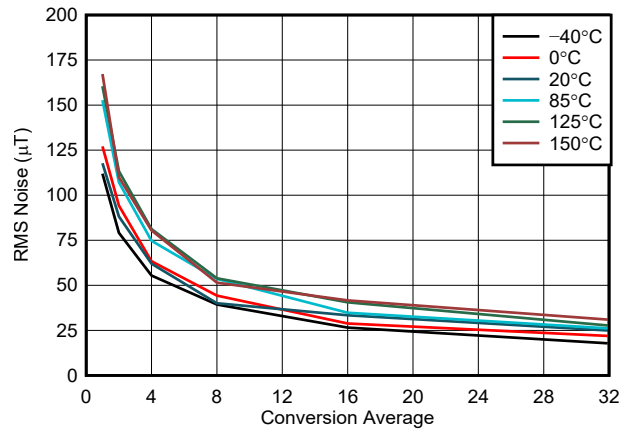


Figure 7-2. X, Y-Axis Noise vs Conversion Average, 25-mT Range

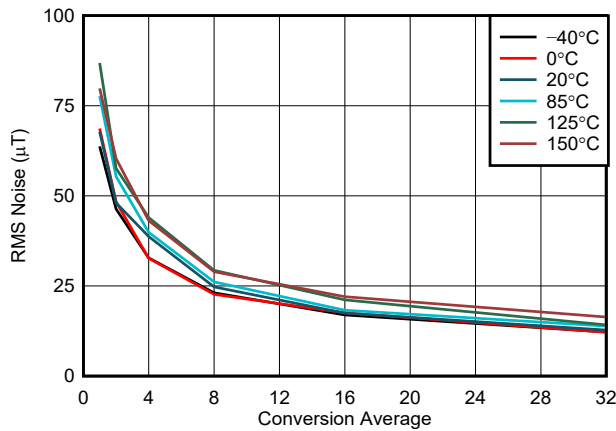


Figure 7-3. Z-Axis Noise vs Conversion Average, 50-mT Range

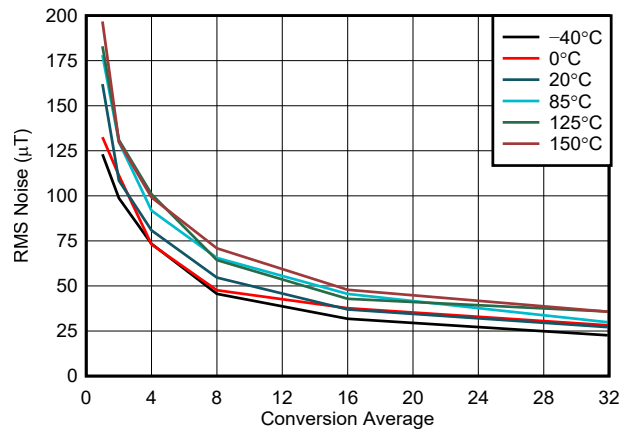


Figure 7-4. X, Y-Axis Noise vs Conversion Average, 50-mT Range

### 7.9 Typical Characteristics (continued)

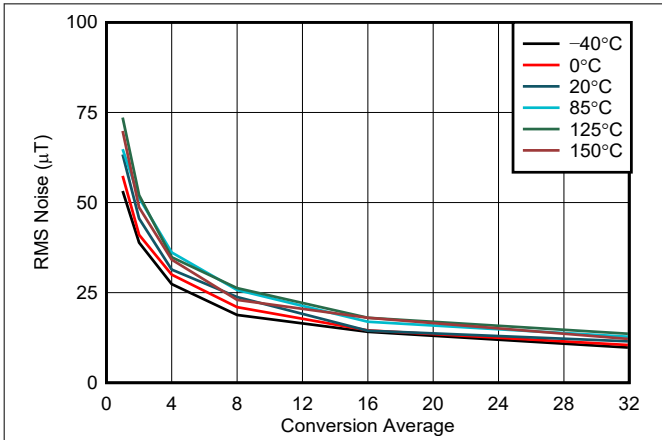


Figure 7-5. Z-Axis Input vs Conversion Average, 75-mT Range

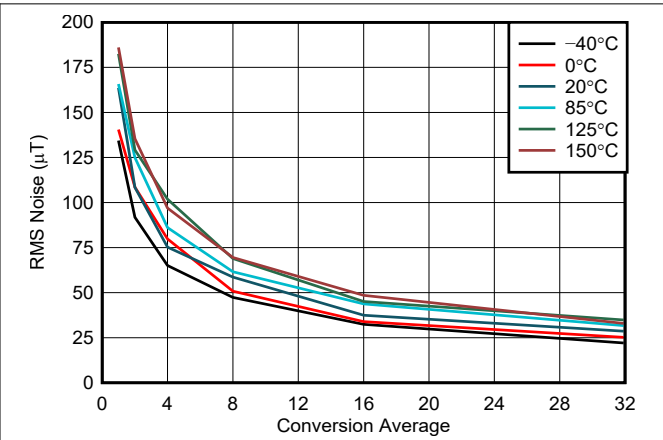


Figure 7-6. X, Y-Axis Noise vs Conversion Average, 75-mT Range

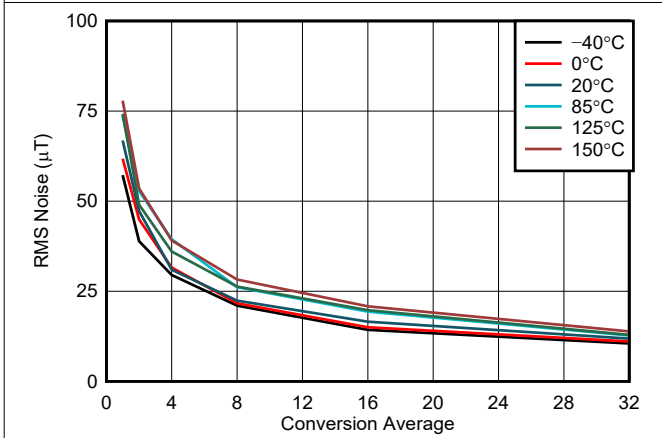


Figure 7-7. Z-Axis Noise vs Conversion Average, 100-mT Range

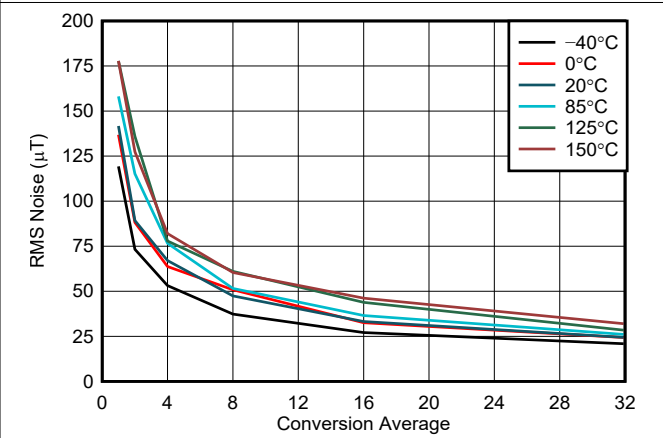


Figure 7-8. X, Y-Axis Noise vs Conversion Average, 100-mT Range

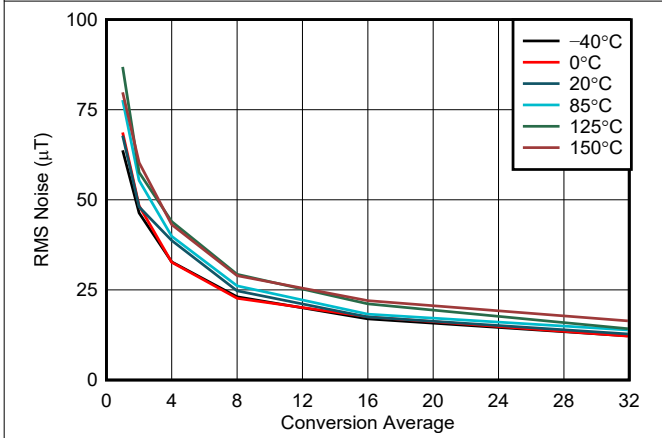


Figure 7-9. Z-Axis Noise vs Conversion Average, 150-mT Range

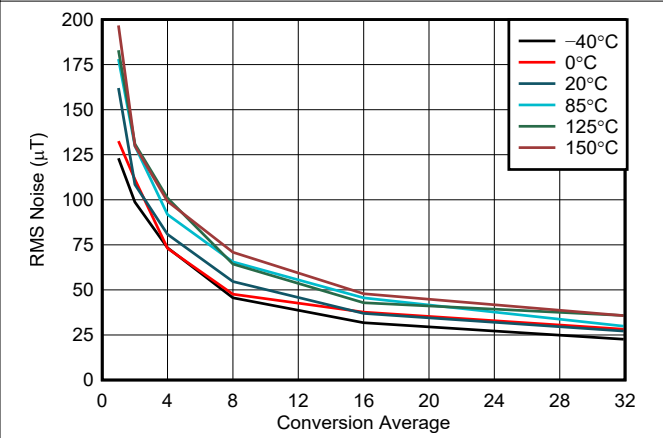
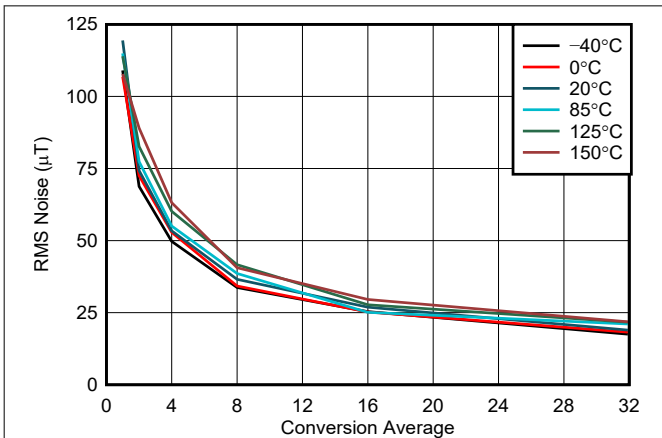


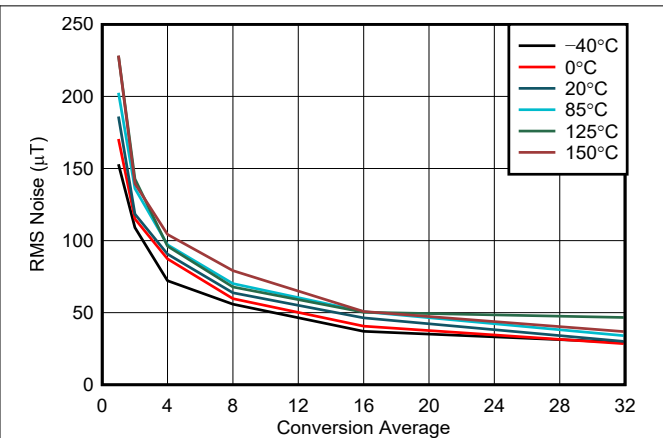
Figure 7-10. X, Y-Axis Noise vs Conversion Average, 150-mT Range

### 7.9 Typical Characteristics (continued)

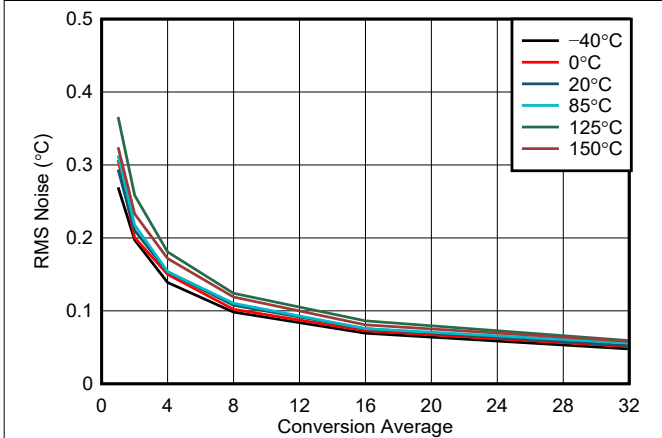
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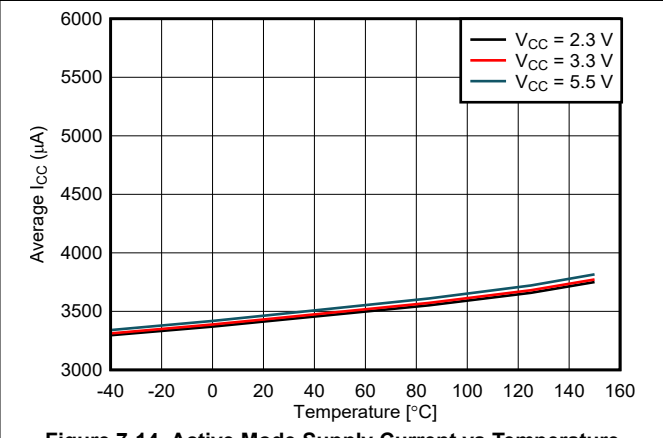
**Figure 7-11. Z-Axis Noise vs Conversion Average, 300-mT Range**



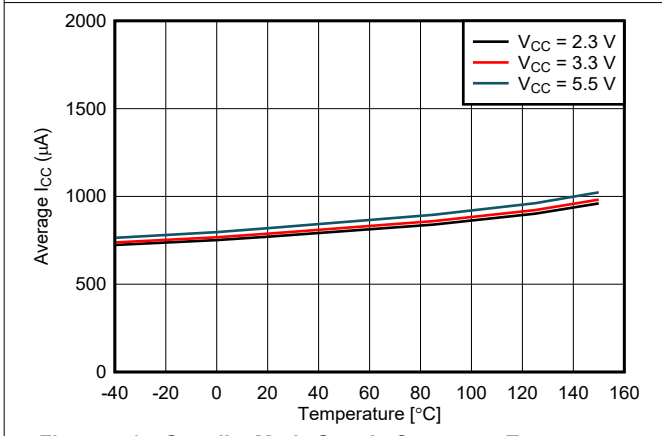
**Figure 7-12. X, Y-Axis Noise vs Conversion Average, 300-mT Range**



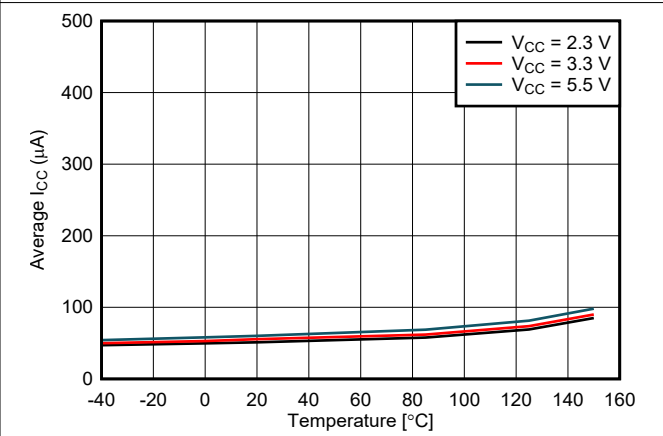
**Figure 7-13. Temperature Sensor Noise vs Conversion Average**



**Figure 7-14. Active Mode Supply Current vs Temperature**



**Figure 7-15. Standby Mode Supply Current vs Temperature**



**Figure 7-16. Configuration Mode Supply Current vs Temperature**

### 7.9 Typical Characteristics (continued)

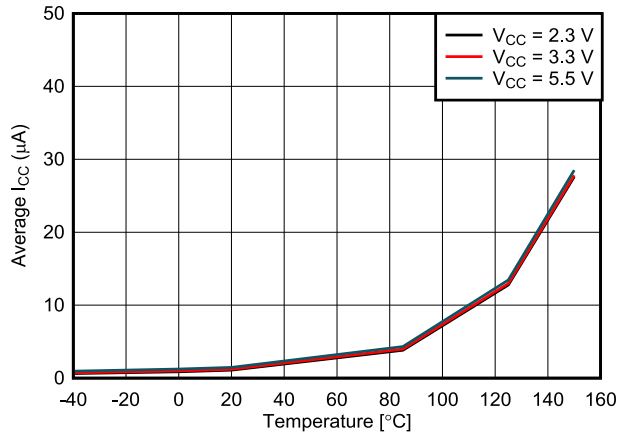


Figure 7-17. Sleep Mode Supply Current vs Temperature

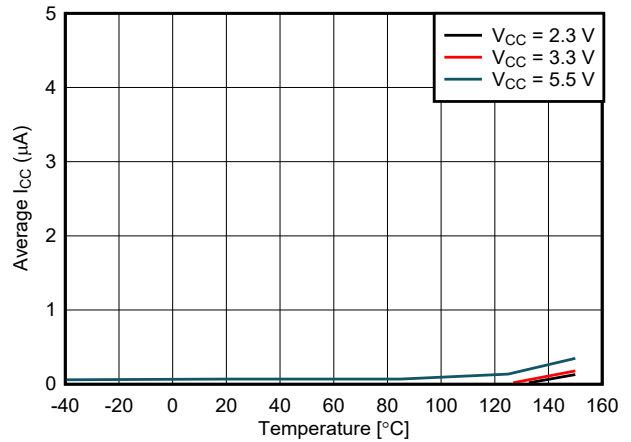


Figure 7-18. Deep Sleep Mode Supply Current vs Temperature

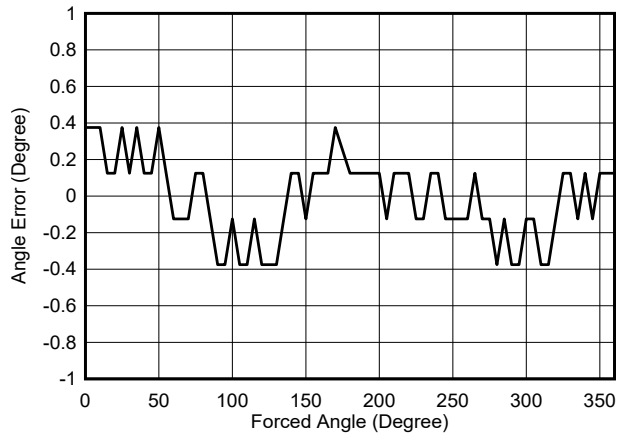


Figure 7-19. Angle Error at 25°C, X-Y Configuration, 50-mT Range

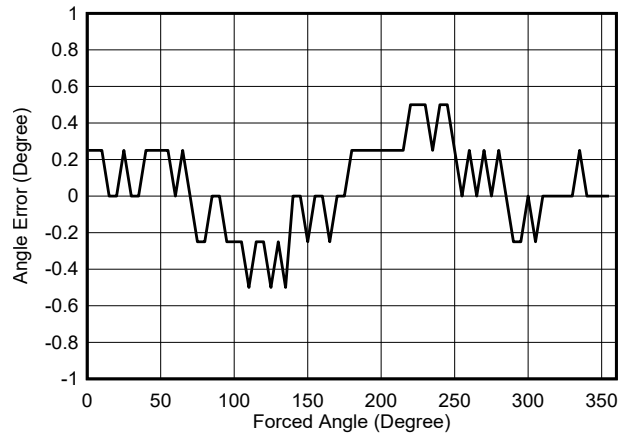


Figure 7-20. Angle Error at 25°C, X-Z Configuration, 50-mT Range

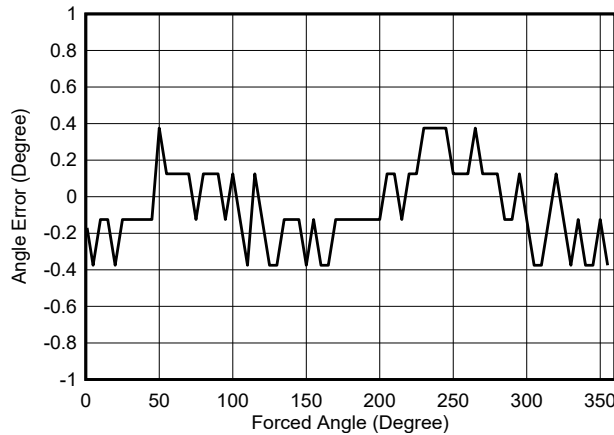


Figure 7-21. Angle Error at 25°C, Y-Z Configuration, 50-mT Range

## 8 Detailed Description

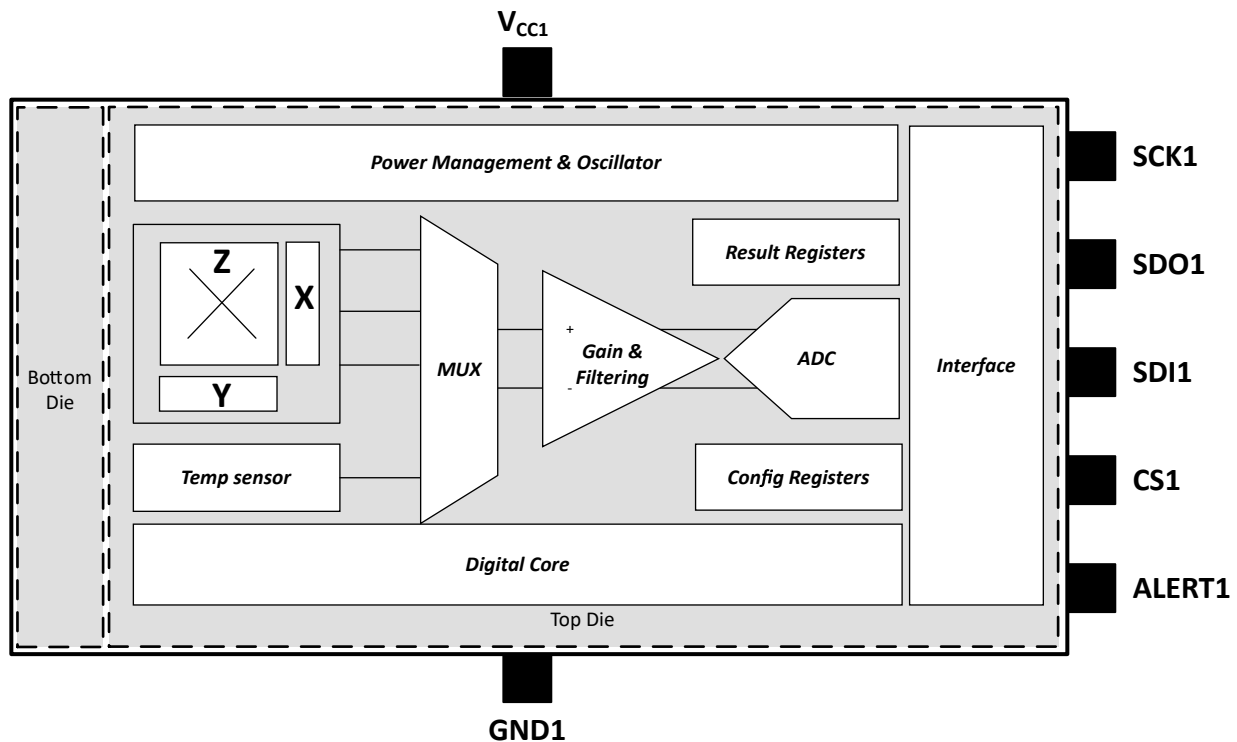
### 8.1 Overview

The TMAG5170D-Q1 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z magnetic data and die temperature data) is provided through the SPI. The device can be configured in multiple settings through user access registers in the SPI.

The IC consists of the following functional and building blocks:

- The Power Management & Oscillator block contains a low-power oscillator, biasing circuitry, undervoltage and overvoltage detection circuitry, and a fast oscillator.
- The sensing and temperature measurement block contains the Hall biasing, Hall sensors with multiplexers, noise filters, integrator circuit, temperature sensor, and the ADC. The Hall sensor data and temperature data are multiplexed through the same ADC.
- The Interface block contains the SPI control circuitry, ESD protection circuits, and all the I/O circuits. The TMAG5170D-Q1 supports SPI along with an integrated cyclic redundancy check (CRC).
- The diagnostic blocks are embedded in the circuitry to enable mandatory and user-enabled diagnostic checks.

### 8.2 Functional Block Diagram

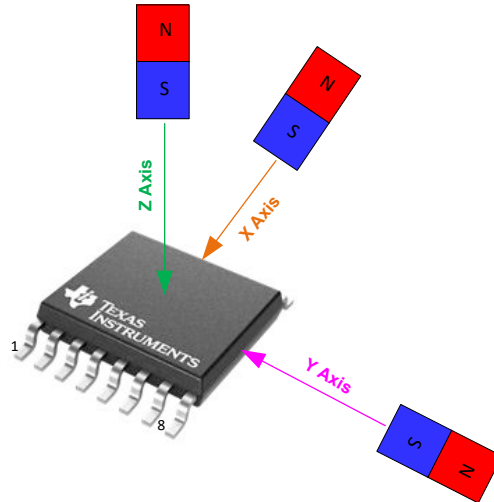


### 8.3 Feature Description

#### 8.3.1 Magnetic Flux Direction

The TMAG5170D-Q1 is sensitive to the magnetic field component in X, Y, and Z directions. The X and Y fields are in-plane with the package. The Z field is perpendicular to the top of the package. The device is sensitive to both magnetic north and south poles in each axis. As shown in [Figure 8-1](#), the device generates positive ADC codes in response to a magnetic south pole in the proximity. Similarly, the device generates negative ADC codes if magnetic north poles approach from the same directions.

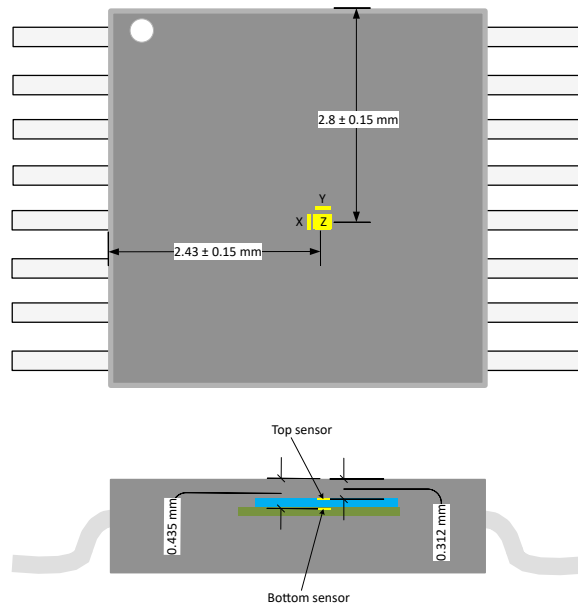




**Figure 8-1. Direction of Applied Magnetic South Pole to Generate Positive ADC Codes**

### 8.3.2 Sensor Location

Figure 8-2 shows the location of the X, Y, Z Hall elements inside the TMAG5170D-Q1.



**Figure 8-2. Location of X, Y, Z Hall Elements**

### 8.3.3 Magnetic Range Selection

Table 8-1 shows the magnetic range selection for the TMAG5170D-Q1 device. Each axis range can be independently selected irrespective of the others.

**Table 8-1. Magnetic Range Selection**

	RANGE REGISTER SETTING	TMAG5170A1-Q1	TMAG5170A2-Q1	COMMENT
X Axis Field	X_RANGE = 00b	±50 mT	±150 mT	
	X_RANGE = 01b	±25 mT	±75 mT	Best resolution case
	X_RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case
Y Axis Field	Y_RANGE = 00b	±50 mT	±150 mT	
	Y_RANGE = 01b	±25 mT	±75 mT	Best resolution case
	Y_RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case
Z Axis Field	Z_RANGE = 00b	±50 mT	±150 mT	
	Z_RANGE = 01b	±25 mT	±75 mT	Best resolution case
	Z_RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case

### 8.3.4 Update Rate Settings

The TMAG5170D-Q1 offers multiple update rates for system design flexibility. Figure 8-4 shows the different update rates for the TMAG5170D-Q1 during continuous conversion.

**Table 8-2. Update Rate Settings**

OPERATING MODE	REGISTER SETTING	UPDATE RATE			COMMENT
		SINGLE AXIS	TWO AXIS	THREE AXIS	
X, Y, Z Axis	CONV_AVG = 000b	20 kSPS	13.3 kSPS	10 kSPS	Fastest update rate
X, Y, Z Axis	CONV_AVG = 001b	13.3 kSPS	8.0 kSPS	5.7 kSPS	
X, Y, Z Axis	CONV_AVG = 010b	8.0 kSPS	4.4 kSPS	3.1 kSPS	
X, Y, Z Axis	CONV_AVG = 011b	4.4 kSPS	2.4 kSPS	1.6 kSPS	
X, Y, Z Axis	CONV_AVG = 100b	2.4 kSPS	1.2 kSPS	0.8 kSPS	
X, Y, Z Axis	CONV_AVG = 101b	1.2 kSPS	0.6 kSPS	0.4 kSPS	Best SNR case

### 8.3.5 ALERT Function

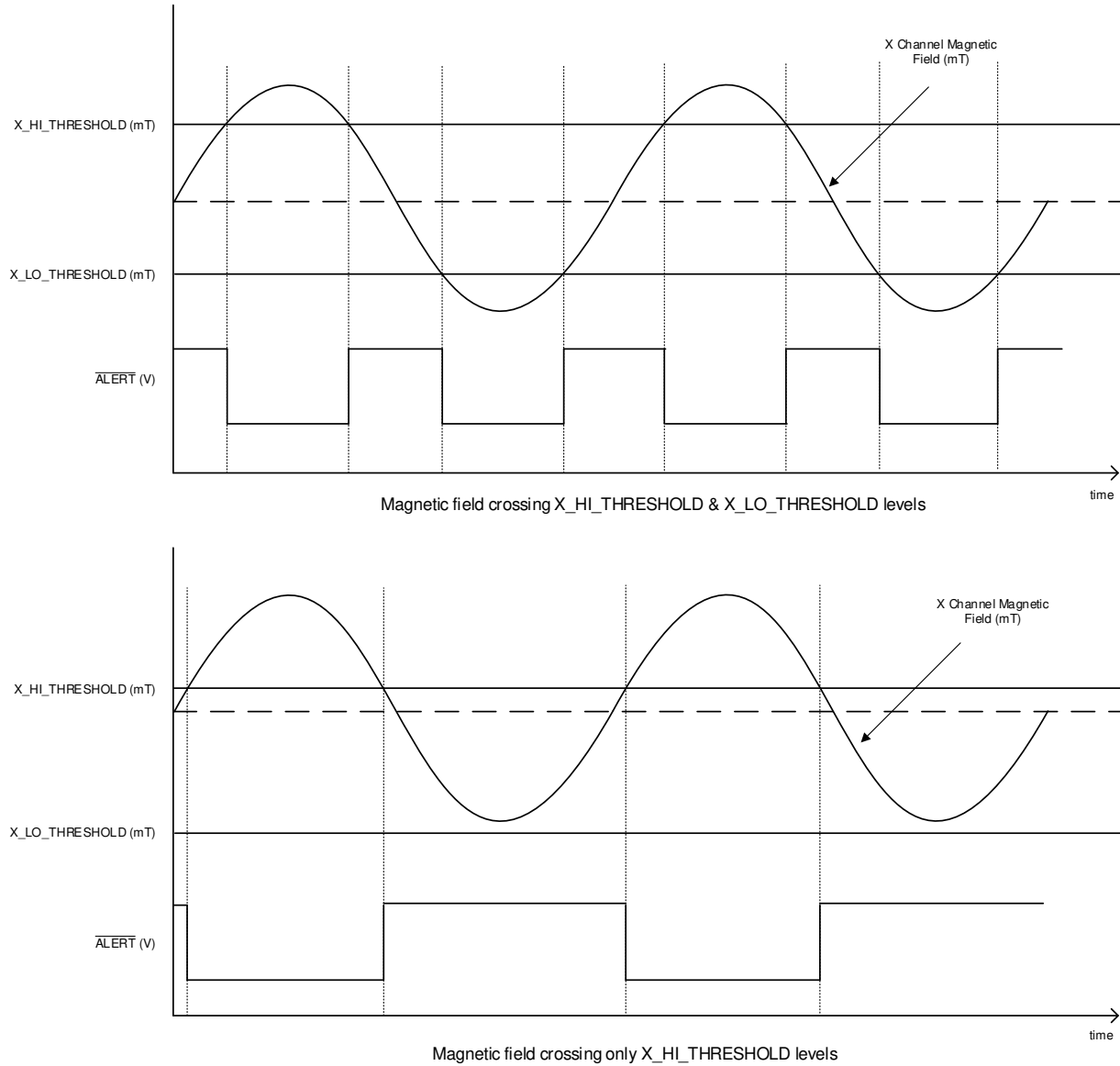
The  $\overline{\text{ALERT}}$  pin of the TMAG5170D-Q1 supports multiple operating modes targeting different applications.

#### 8.3.5.1 Interrupt and Trigger Mode

With ALERT\_MODE at default value of 0b, the  $\overline{\text{ALERT}}$  output can be configured to generate an interrupt signal for the microcontroller when a user-defined event occurs. A user-defined event can be a conversion completion or an error from diagnostic tests. The  $\overline{\text{ALERT}}$  pin can also trigger a conversion start in this mode using the TRIGGER\_MODE register bit.

#### 8.3.5.2 Magnetic Switch Mode

With ALERT\_MODE set at 1b, the  $\overline{\text{ALERT}}$  output is configured as a magnetic switch. One or multiple magnetic channels can be selected in the ALERT\_CONFIG register. The magnetic switch thresholds are determined by the \*\_THR\_X\_CONFIG register bits setting. If the measured magnetic field is greater than \*\_HI\_THRESHOLD, or smaller than \*\_LO\_THRESHOLD, the  $\overline{\text{ALERT}}$  output will assert low. Figure 8-3 shows the magnetic switch function using the X-axis magnetic field as an example.



**Figure 8-3. ALERT Pin Working as Magnetic Switch**

### 8.3.6 Threshold Count

The THRX\_COUNT bits in the ALERT\_CONFIG register offer robust noise filtering and immunity against false tripping while the TMAG5170D-Q1 implements the  $\overline{\text{ALERT}}$  function for a specific magnetic or temperature threshold crossing. With THRX\_COUNT at default 00b, only one measured value must cross the threshold to be considered a valid threshold crossing event. With THRX\_COUNT at 11b, four successive measured values must cross the threshold to be considered a valid threshold crossing. An internal counter tracks and records the number of threshold crossing for a given sensor.

The counter resets if any of the below events occur:

- The device meets the threshold cross count for the specified number per the THRX\_COUNT bits, the corresponding \*CH\_THX bit(s) are set, and the SPI read of the SYS\_STATUS register occurred
- If a measured result does not cross the threshold

When the  $\overline{\text{ALERT}}$  pin is configured to work as a magnetic switch, the threshold count is active for both low-to-high and high-to-low transitions, offering noise immunity in both directions of the threshold cross.

### 8.3.7 Diagnostics

The TMAG5170D-Q1 supports several device and system level diagnostics features to detect, monitor, and report failures during the device operation.

In the event of a failure, the TMAG5170D-Q1 reports back to the controller through the following mechanisms:

- **ERROR\_STAT** bit during the SDO read frame
- **Direct read** of the status registers through the SPI
- **ALERT** pin response to indicate a failure, if enabled
- No response through SDO line, or CRC error during SPI communication

The TMAG5170D-Q1 performs the following device and system level checks:

#### 8.3.7.1 Memory Cyclic Redundancy Check (CRC)

This diagnostic mechanism checks the content of the internal memory by comparing a calculated CRC of the read content against a factory-programmed expected CRC value. During runtime, when the internal memory is read again for configuration for different channels, the CRC is checked again, providing detection of memory errors even during runtime.

Run Mode	Continuous
Configuration Register(s)	N/A
Fault Register Bit	TRIM_STAT
Impact if disabled	N/A. Cannot be disabled

#### 8.3.7.2 ALERT Integrity Check

This diagnostic mechanism checks and compares the read back value of the  $\overline{\text{ALERT}}$  pin to the value that is driven by the device. This will check the presence of an external short on  $\overline{\text{ALERT}}$  pin to a higher voltage such as VCC which will prevent device to indicate a fault. When the controller is driving the  $\overline{\text{ALERT}}$  pin to trigger a measurement, the controller can read the ALRT\_LVL bit to check if the correct polarity of the  $\overline{\text{ALERT}}$  was detected by the device, thus checking any failures on the pin.

Run Mode	Continuous
Configuration Register(s)	N/A
Fault Register Bit	ALRT_DRV and ALRT_LVL
Impact if disabled	When driven by device N/A. Cannot be disabled. When driven by controller, device may not detect a new measurement command and still report old measurement data.

#### 8.3.7.3 VCC Check

This diagnostic mechanism continuously checks the external voltage supply on VCC pin and flags a fault if the supply is out of range.

Run Mode	Continuous
Data Sheet Parameters	V <sub>VCC_UV</sub> , V <sub>VCC_OV</sub>
Fault Register Bit	VCC_UV and VCC_OV
Impact if disabled	N/A. Cannot be disabled.

#### 8.3.7.4 Internal LDO Undervoltage Check

This diagnostic mechanism continuously monitors the internal regulator that supplies the critical analog blocks and Hall sensor biasing, and flags a fault if the internal regulator falls below a threshold after which the accuracy of the magnetic field measurement cannot be guaranteed.

Run Mode	Continuous
Data Sheet Parameters	N/A
Fault Register Bit	LDO_STAT
Impact if disabled	N/A. Cannot be disabled.

#### 8.3.7.5 Digital Core Power-On Reset Check

This diagnostic mechanism continuously monitors the internal regulator that supplies the internal digital core, and puts the device in reset if the digital core cannot function reliably. The occurrence of the fault is detected by reading the CFG\_RESET bit which can only be set at power up or if the digital core was reset.

Run Mode	Continuous
Data Sheet Parameters	N/A
Fault Register Bit	CFG_RESET
Impact if disabled	N/A. Cannot be disabled.

#### 8.3.7.6 SDO Output Check

This diagnostic mechanism continuously compares the internally driven value by device on the SDO pin to the read-back value on SDO pin to detect any shorts to ground or power supply.

Run Mode	Continuous, every time a SPI transaction is initiated
Data Sheet Parameters	N/A
Fault Register Bit	SDO_DRV
Impact if disabled	N/A. Cannot be disabled.

#### 8.3.7.7 Communication Cyclic Redundancy Check (CRC)

This diagnostic mechanism for every SPI transaction will compute the CRC of the received SPI frame from the controller and check the CRC against the CRC value transmitted by the controller, and flag a fault if the values do not match. The device also embeds a CRC value as part of the SPI frame in the response for the controller to check the integrity of the received data. This check detects faults with the SPI communication block in the digital core, the SPI I/O buffers and, and the controller to check for any faults on the SPI external to the device.

Another check also runs in the background that counts the number of SPI clocks in a SPI frame and flags a fault if the number of clocks sent by the controller is not same as the expected value. This can help the controller detect any issues with the SPI.

Run Mode	Continuous, every time a SPI transaction is initiated
Configuration Register(s)	CRC_DIS to disable CRC in the SPI protocol
Fault Register Bit	CRC_STAT, FRAME_STAT
Impact if disabled	If CRC is disabled, then any fault with SPI communication will not be detected and incorrect value of measured field can be reported.

#### 8.3.7.8 Oscillator Integrity Check

This diagnostic mechanism allows the controller to check any hardware fault with the internal oscillator. With this check, any drift of internal oscillators can be checked. The high-frequency oscillator is critical for precision measurement of the magnetic field and low-power oscillator is critical to control wake-up and sleep mode and other state machine control.

To run this check, external software code on the controller is required. The controller must instate the check by setting the OSC\_CNT\_CTL bits to select a particular oscillator and start the internal count on the device. At the same time, the controller also starts a counter using its own timebase. After a predetermined time, the controller issues a stop to the oscillator count by setting OSC\_CNT\_CTL=0x3 and read the OSC\_COUNT. The read value of the OSC\_COUNT should not exceed the value based off maximum  $f_{HFOSC}$ ,  $f_{LFOSC}$  in the specification section. Consider the variation of controller speed and SPI communication when calculating the error margin for the OSC\_COUNT.

Run Mode	On-demand as run by the external controller
Data Sheet Parameter(s)	$f_{HFOSC}$ , $f_{LFOSC}$
Configuration Register(s)	OSC_CNT_CTL
Fault Register Bit	OSC_COUNT
Impact if disabled	If the controller decides not to run this test, then any drift of HF oscillator can impact the accuracy of the reported sensor data

### 8.3.7.9 Magnetic Field Threshold Check

This diagnostic mechanism allows the controller to monitor the external applied field. The controller can use this check to determine if a magnetic field is present within specified thresholds. This check, though used as check at system level, can also indicate any gross problems with the signal path if a field much outside the expected range is detected and reported.

To run this check, the controller must enable the check separately for each axis and also set the thresholds for each axis independently. The user can configure the ALERT pin to toggle if the threshold crossed, which is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	X_HLT_EN, Y_HLT_EN, Z_HLT_EN to enable test. X_THRX_CONFIG, Y_THRX_CONFIG, Z_THRX_CONFIG to set threshold
Fault Register Bit	XCH_THX, YCH_THX, ZCH_THX
Impact if disabled	Disabling this check does not have an impact on device-level failure detection but can impact at system level. Examples of system failure would be loss of magnet, magnet too far, or too close to the sensor.

### 8.3.7.10 Temperature Alert Check

This diagnostic mechanism allows the controller to monitor the junction temperature of the die, which is also an indication of the ambient temperature as the device does not generate significant self-heating. This is useful to monitor the temperature at the system level accurately and alert the controller if the temperature is exceeded. The check can also be used to warn the controller if the die temperature due to some internal failure has increased beyond the expected range.

To run this check, the controller must enable the temperature check and set the threshold. The user can configure the ALERT pin to toggle if the threshold crossed, which is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	T_HLT_EN to enable test. T_THRX_CONFIG to set threshold
Fault Register Bit	TEMP_THX
Impact if disabled	Disabling this check does not have an impact on device-level failure detection but can impact at system level increase or decrease of temperature.

### 8.3.7.11 Analog Front-End (AFE) Check

This diagnostic mechanism allows the controller to check the performance of the analog signal path. In this check, the device disconnects the Hall sensor from the signal path and uses an alternate resistance bridge to create a known, predetermined signal as an input to the signal path. This mechanism then checks if the measured digital value compared to a fixed value from the factory is within a pre-programmed, factory-determined value. This mechanism can detect issues with multiplexers, offset cancellation mechanism, the gain stages, the low-pass filter, and the ADC as well.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the AFE is not available for magnetic field conversion. The user can configure the  $\overline{\text{ALERT}}$  pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	SENS_STAT
Impact if disabled	If disabled, any failures or drift with the analog front-end signal path may not be detected.

### 8.3.7.12 Hall Resistance and Switch Matrix Check

This diagnostic mechanism allows the controller to check if the sensitivity of the Hall sensor is within the factory-determined limits by checking the resistance of the Hall-effect sensor. In this check, the biasing and multiplexing control of all directions of the Hall sensor (X, Y and Z) are also checked.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the Hall sensor is not available for magnetic field conversion. The user can configure the  $\overline{\text{ALERT}}$  pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	ZHS_STAT, YHS_STAT and XHS_STAT
Impact if disabled	If disabled, any failures or drift in the Hall-effect sensor properties and biasing will not be detected, leading to potentially incorrect magnetic field conversion

### 8.3.7.13 Hall Offset Check

This diagnostic mechanism allows the controller to check if the offset of the Hall sensor is within the factory-determined limits and the offset cancellation circuitry is working properly.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the AFE is not available for magnetic field conversion. The user can configure the  $\overline{\text{ALERT}}$  pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	SENS_STAT
Impact if disabled	If disabled, any failures with offset cancellation mechanism or large drift of Hall-effect sensor may not be detected, leading to potentially incorrect magnetic field conversion.

### 8.3.7.14 ADC Check

This diagnostic mechanism checks ADC functionality and conversion. This check is done by converting a known band-gap voltage, which is completely independent of the ADC reference, and comparing the voltage against the factory-determined tolerance limits.

To run this check, the controller must enable the check and set the scheduling for the run. During this check the AFE is not available for magnetic field conversion. The user can configure the  $\overline{\text{ALERT}}$  pin to toggle if an error is detected. This error is also reported in the user register.

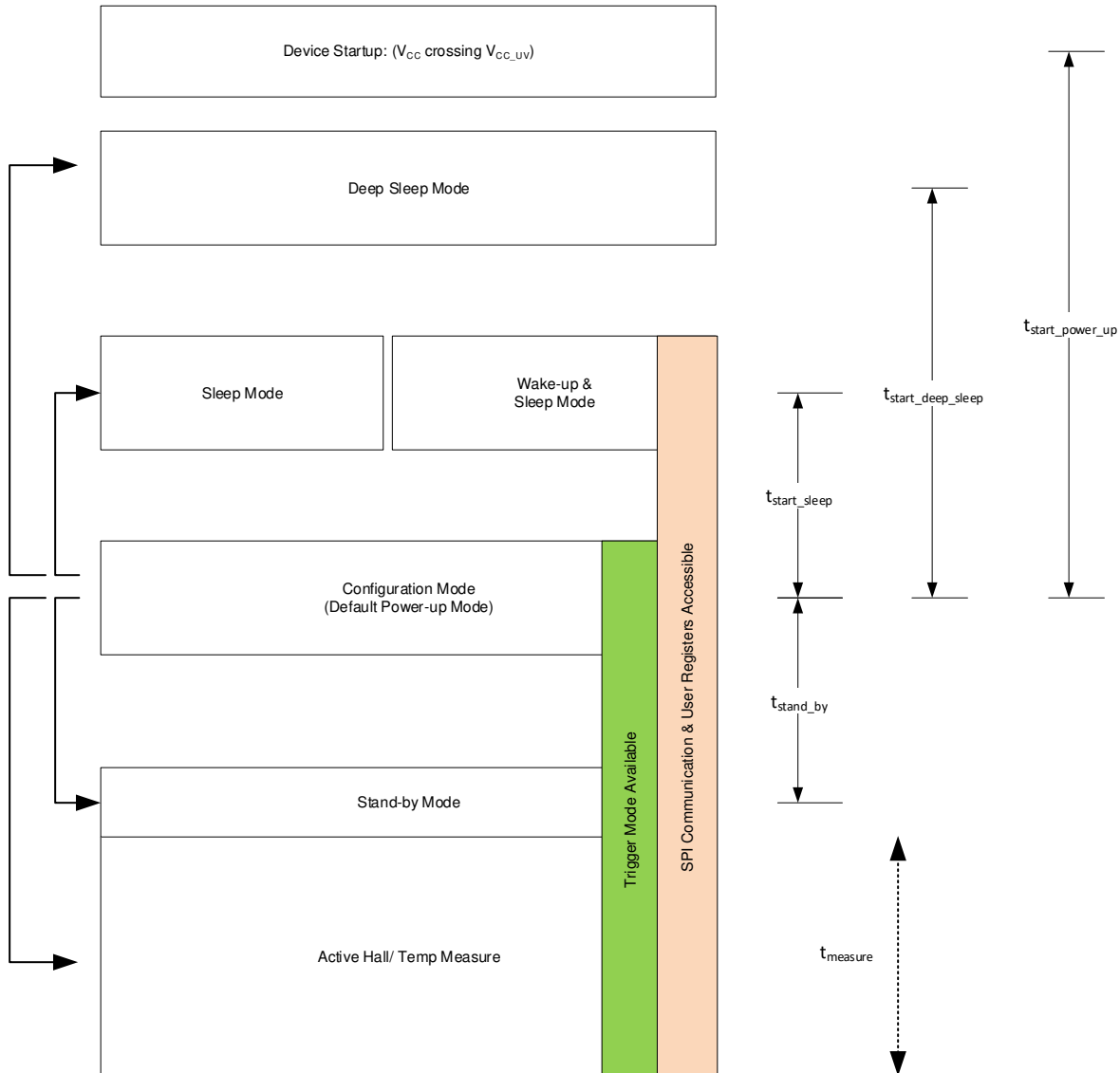
Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	TEMP_STAT
Impact if disabled	If disabled, any failures with ADC conversion will not be detected, leading to potentially incorrect errors in the converted magnetic field values.

## 8.4 Device Functional Modes

### 8.4.1 Operating Modes

The TMAG5170D-Q1 supports multiple operating modes for wide array of applications as explained in [Figure 8-4](#). The device starts powering up after the VCC supply crosses the minimum threshold as specified in the [Recommended Operating Conditions](#) table. Any particular operating mode can be selected by setting the corresponding OPERATING\_MODE register bits.

ADVANCE INFORMATION



**Figure 8-4. TMAG5170D-Q1 Power-Up Sequence**

[Table 8-3](#) shows different power saving modes of the TMAG5170D-Q1.

**Table 8-3. Comparing Operating Modes**

OPERATING MODE	DEVICE FUNCTION	INITIALIZATION TIME TO START CONVERSION <sup>(1)</sup>	DATA CONVERSION
Active Conversion	Continuously measuring X, Y, Z axis, or temperature data	10 $\mu$ s	Supports continuous and trigger mode conversion
Standby Mode	Device is ready to accept SPI commands and start active conversion	35 $\mu$ s	Supports trigger mode conversion
Configuration Mode	SPI and user configuration registers active	$t_{stand\_by} + 35 \mu$ s	Supports trigger mode conversion



**Table 8-3. Comparing Operating Modes (continued)**

OPERATING MODE	DEVICE FUNCTION	INITIALIZATION TIME TO START CONVERSION <sup>(1)</sup>	DATA CONVERSION
Wake-up & Sleep Mode	Wakes up at a certain interval to measure the X, Y, Z axis, or temperature data	$t_{\text{start\_sleep}} + t_{\text{stand\_by}} + 35 \mu\text{s}$	1, 5, 10, 15, 20, 30, 100, 500, and 1000-ms intervals supported <sup>(1)</sup> .
Sleep Mode	Device retains key configuration settings, and last measurement data	$t_{\text{start\_sleep}} + t_{\text{stand\_by}} + 35 \mu\text{s}$	The microcontroller can use sleep mode to implement other power saving intervals not supported by wake-up and sleep mode.
Deep-sleep Mode	Device does not retain key configuration settings, and last measurement data	$t_{\text{start\_deep\_sleep}} + t_{\text{stand\_by}} + 35 \mu\text{s}$	No conversion start is supported during deep-sleep mode

(1) The timing numbers are typical parameters. Their value may vary depending on the internal oscillator frequency.

#### 8.4.1.1 Active Mode

The TMAG5170D-Q1 converts the magnetic sensor or temperature data during active mode. Active mode supports both continuous conversion and trigger mode conversion based off the OPERATING\_MODE setting. Continuous operation at this mode is useful for applications where the fastest data conversion is required, and power budget is not stringent. In the active trigger mode, a controller can trigger a conversion through one of several trigger mechanisms as described in the TRIGGER\_MODE register bits. When the conversion started, the time it takes to finish a conversion is denoted by  $t_{\text{measure}}$ . The conversion time can vary widely based off the MAG\_CH\_EN, CONV\_AVG, DIAG\_SEL, and DIAG\_EN register bits setting. The average current consumption during the active conversion is  $I_{\text{ACT}}$ .

#### 8.4.1.2 Standby Mode

In standby mode, the TMAG5170D-Q1 is ready to start sensor conversion with a trigger command from a controller. Several trigger methods are supported as defined in the TRIGGER\_MODE register bits. During this operating mode, the relevant analog and digital support circuitry remain active to enable a faster conversion start. The average current consumption during this mode is denoted by  $I_{\text{STDBY}}$ . The time it takes for the device to go to standby mode from configuration mode is denoted by  $t_{\text{stand\_by}}$ .

#### 8.4.1.3 Configuration Mode (DEFAULT)

At power up, the TMAG5170D-Q1 goes into the default configuration mode. In this mode, the SPI communication and user register access are enabled. A controller may configure the device to select the desired operating mode, sensor data conversion, enable or disable diagnostic features, and so forth. The average current consumption during this mode is denoted by  $I_{\text{CFG}}$ . Similar to the standby mode, the configuration mode also supports sensor conversion start with a trigger. However, the configuration mode takes longer time to start the sensor conversion, and consumes approximately ten times less current compared to standby mode.

#### 8.4.1.4 Sleep Mode

The TMAG5170D-Q1 supports the sleep mode where the device retains the user configuration settings and previous conversion results. A controller can wake up the device from sleep mode through either the SPI communication or the ALERT signal. The average power consumption in this mode is denoted by  $I_{\text{SLP}}$ . The time it takes for the device to go to the configuration mode from the sleep mode is denoted by  $t_{\text{start\_sleep}}$ .

#### 8.4.1.5 Wake-Up and Sleep Mode

The TMAG5170D-Q1 supports the wake-up and sleep mode where the device is configured to wake up at a certain time interval, and perform the sensor conversion as defined in the SENSOR\_CONFIG register setting. When the sensor conversion is complete, an ALERT signal can be generated to notify the controller that the new conversion data is ready. It is possible to generate an ALERT signal only in the event a particular magnetic or temperature threshold is exceeded. Detail setting on ALERT signal is specified in the ALERT\_CONFIG register. A controller can wake up the TMAG5170D-Q1 and access the conversion data at any time. The average power consumption in the wake-up and sleep mode is denoted by  $I_{\text{VCC\_DCM}}$ . The time it takes for the device to go to configuration mode from wake-up and sleep mode is denoted by  $t_{\text{start\_sleep}}$ .

### 8.4.1.6 Deep-Sleep Mode

For ultra-low power system, the TMAG5170D-Q1 supports a deep-sleep mode to conserve power. In this mode, the TMAG5170D-Q1 does not retain the user configuration or previous result data. The device reverts back to factory setting in this mode. The average power consumption in this mode is  $I_{DEEP\_SLP}$ . The time it takes for the device to go to the configuration mode from the deep-sleep mode is denoted by  $t_{start\_sleep}$ .

## 8.5 Programming

### 8.5.1 Data Definition

#### 8.5.1.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in the X\_CH\_RESULT, Y\_CH\_RESULT, and Z\_CH\_RESULT registers, respectively. Figure 8-5 shows the 12-bit ADC output stored in 16-bit result registers in 2's complement format. With fastest conversion (CONV\_AVG = 000b), the ADC output loads the 12 MSB bits of the 16-bit result register along with 4 LSB bits as zeros. With CONV\_AVG ≠ 000b, all the 16 bits are used to store the results. With DATA\_TYPE = 00b, the 16-bit magnetic sensor data can be accessed through regular 32-bit SPI read. Use Equation 1 to calculate the measured magnetic field.

$$B = \frac{-(D_{15} \times 2^{15}) + \sum_{i=0}^{14} D_i \times 2^i}{2^{16}} \times 2|B_R| \quad (1)$$

where

- B is magnetic field in mT.
- $D_i$  is the data bit as shown in Figure 8-5.
- $B_R$  is the magnetic range in mT for the corresponding channel.

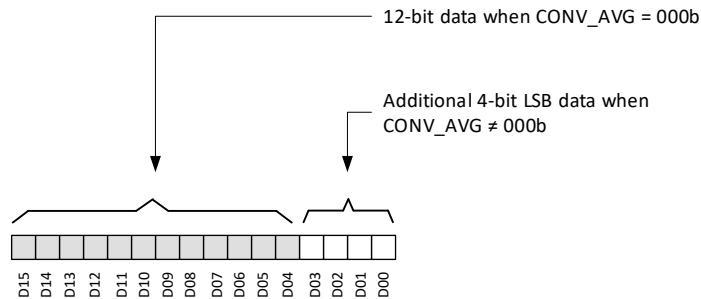


Figure 8-5. Magnetic Sensor Data Definition

With DATA\_TYPE ≠ 00b, the 12 MSB bits (D04 to D15) from the magnetic result registers can be accessed. In this mode, use Equation 2 to calculate the measured magnetic field.

$$B = \frac{-(D_{15} \times 2^{11}) + \sum_{i=4}^{14} D_i \times 2^{i-4}}{2^{12}} \times 2|B_R| \quad (2)$$

### 8.5.1.2 Temperature Sensor Data

The TMAG5170D-Q1 temperature sensor will measure temperature from  $-40^{\circ}\text{C}$  to  $170^{\circ}\text{C}$ . Figure 8-6 shows the temperature stored in the 16-bit TEMP\_RESULT register. With DATA\_TYPE = 00b, the 16-bit temperature data can be accessed through regular 32-bit SPI read. Use Equation 3 to calculate the temperature.

$$T = T_{SENS\_T0} + \frac{TADC_T - TADC_{T0}}{TADC_{RES}} \quad (3)$$

where

- T is the measured temperature in degree Celsius.
- $T_{SENS\_T0}$  is the reference temperature in degree Celsius as listed in the [Electrical Characteristics](#) table.
- $TADC_{RES}$  is the change in ADC code per degree Celsius as listed in the [Electrical Characteristics](#) table.
- $TADC_{T0}$  is the TEMP\_RESULT decimal value at reference temperature,  $T_{SENS\_T0}$  as listed in the [Electrical Characteristics](#) table.
- $TADC_T$  is the measured TEMP\_RESULT decimal value for temperature T.

With DATA\_TYPE  $\neq$  00b, the 12 MSB bits from the TEMP\_RESULT register can be accessed. In this mode, use Equation 4 to calculate the temperature.

$$T = T_{SENS\_T0} + \frac{16 \times \left( TADC_T - \frac{TADC_{T0}}{16} \right)}{TADC_{RES}} \quad (4)$$

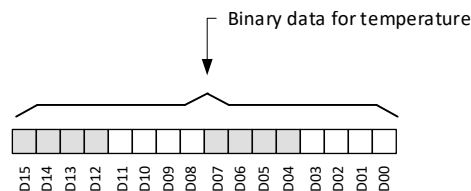


Figure 8-6. Temperature Sensor Data Definition

### 8.5.1.3 Magnetic Sensor Offset Correction

Figure 8-7 shows that the TMAG5170D-Q1 can enable offset correction for a pair of magnetic axes. The magnetic axes and order are selected based off the ANGLE\_EN register bit settings. The MAG\_OFFSET\_CONFIG register stores the offset values to be corrected in 2's complement data format. The selection and order of the sensors are defined in the ANGLE\_EN register bits setting. The default value of these offset correction registers are set as zero.

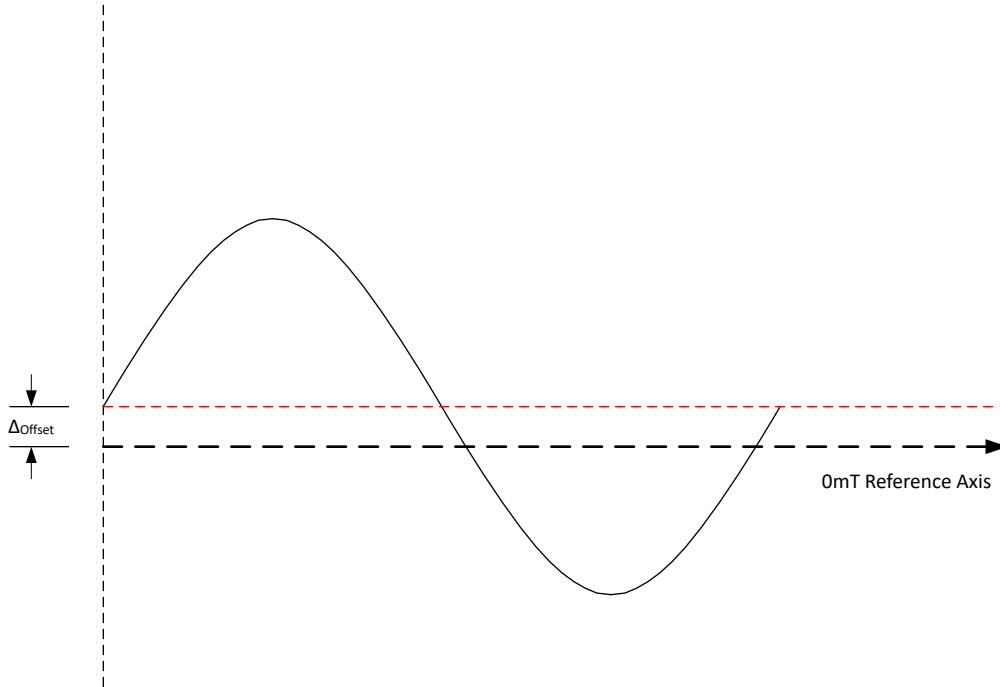


Figure 8-7. Magnetic Sensor Data Offset Correction

Use Equation 5 and Equation 6 to calculate the amount of offset for each axis. As an example, with a  $\pm 50$ -mT magnetic range for X and Z axes, MAG\_OFFSET\_CONFIG set at 1110 0000 0011 0000b, ANGLE\_EN set at 11b. With these conditions the offset correction for the X axis is  $-1.56$  mT and Z axis is  $1.17$  mT. The offset values are added to the sensor conversion results before loading into the corresponding result registers.

$$\Delta_{Offset\_Value1} = \frac{-(D_{13} \times 2^6) + \sum_{i=0}^5 D_i \times 2^i}{2^{12}} \times 2|B_R| \quad (5)$$

$$\Delta_{Offset\_Value2} = \frac{-(D_6 \times 2^6) + \sum_{i=0}^5 D_i \times 2^i}{2^{12}} \times 2|B_R| \quad (6)$$

where

- $\Delta_{Offset\_Value1}$  is the amount of offset correction (in mT) to be applied for first axis.
- $\Delta_{Offset\_Value2}$  is the amount of offset correction (in mT) to be applied for second axis.
- $D_i$  is the data bit in the offset MAG\_OFFSET\_CONFIG register.
- $B_R$  is the magnetic range in mT for the corresponding channel.

### 8.5.1.4 Angle and Magnitude Data Definition

The TMAG5170D-Q1 calculates the angle based off the ANGLE\_EN register bit settings. Figure 8-8 shows that the ANGLE\_RESULT register stores the angle information in the 13-LSB bits. Bits D04-D12 store angle integer value from 0 to 360 degree. Bits D00-D03 store fractional angle value. The 3-MSB bits are always populated as b000. The TMAG5170D-Q1 CORDIC offers angle resolution of ¼ degree. Less than ¼ degree angle resolution can be implemented by performing a CORDIC angle calculation on the system microcontroller using the X, Y, and Z axis readings from the TMAG5170. The [TMAG170 code example software package](#) has functions that can be ported to the system microcontroller for an accurate but computationally inexpensive angle calculation using the TMAG5170D-Q1 axes readings. Use Equation 7 to calculate the angle.

$$A = \sum_{i=4}^{12} D_i \times 2^{i-4} + \frac{\sum_{i=0}^3 D_i \times 2^i}{16} \quad (7)$$

where

- A is the angle measured in degree.
- $D_i$  is the data bit as shown in Figure 8-8.

For example: a 354.50 degree is populated as 0001 0110 0010 1000b and a 17.25 degree is populated as 0000 0001 0001 0100b.

With DATA\_TYPE ≠ 00b, the D01-D12 bits from the ANGLE\_RESULT register can be accessed. In this mode, the angle fractional value is represented by 3 bit. Use Equation 8 to calculate the angle in degree.

$$A = \sum_{i=4}^{12} D_i \times 2^{i-4} + \frac{\sum_{i=1}^3 D_i \times 2^{i-1}}{8} \quad (8)$$

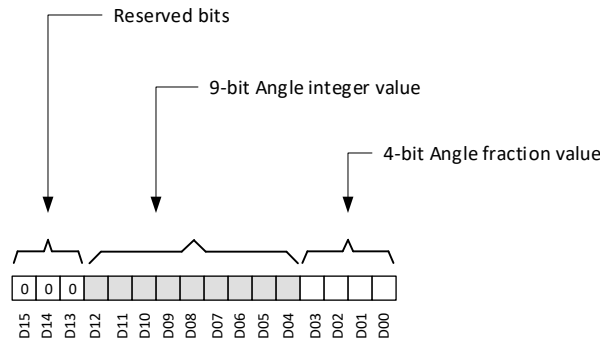


Figure 8-8. Angle Data Definition

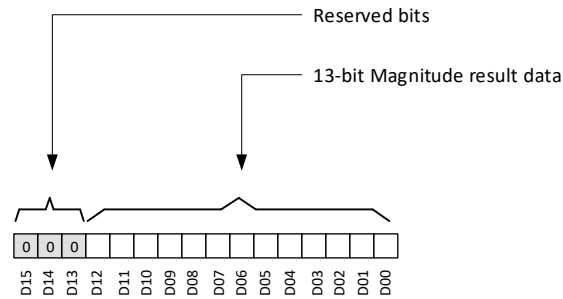
During the angle calculation, use Equation 9 to calculate the resultant vector magnitude.

$$M = \sqrt{MADC_{Ch1}^2 + MADC_{Ch2}^2} \quad (9)$$

where

- $MADC_{Ch1}$ ,  $MADC_{Ch2}$  are the ADC codes of the two magnetic channels selected for the angle calculation.

Figure 8-9 shows the magnitude value stored in the MAGNITUDE\_RESULT register. This value should be constant during 360 degree angle measurements.



**Figure 8-9. Magnitude Result Data Definition**

The magnitude result can be accessed through SPI in 16-bit or 12-bit formats. In the 12-bit format, bit D01 to bit D12 are sent through the SPI.

### 8.5.2 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is a synchronous serial communication interface used for short distance communication, usually between devices on a printed circuit board (PCB) assembly. The TMAG5170D-Q1 supports a 4-wire SPI interface. The primary communication between the device and the external microcontroller is through the SPI bus that provides full-duplex communication. The external microcontroller works as the SPI controller that sends command requests on the SDI pin and receives device responses on the SDO pin. The TMAG5170D-Q1 device works as the SPI peripheral device that receives command requests and sends responses (such as status and measured values) to the external microcontroller over the SDO line. The TMAG5170D-Q1 supports a fixed 32-bit frame size to communicate with a controller device. However, the 32-bit frame can be configured through DATA\_TYPE register bits to support a regular single register read data packet, or a special packet to read two-channel data simultaneously.

#### 8.5.2.1 SCK

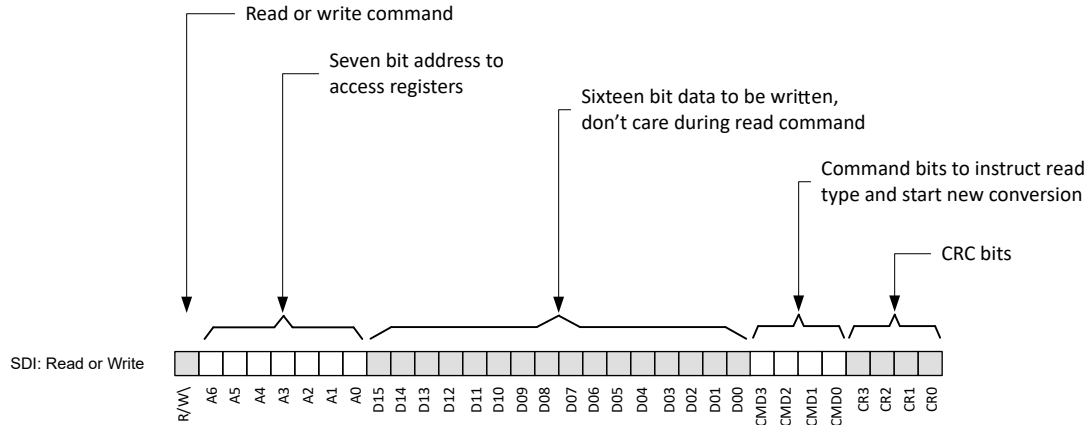
The Serial Clock (SCK) represents the controller clock signal. This clock determines the speed of data transfer and all receiving and sending are done synchronously to this clock. The output data on the SDO pin transitions on the falling edge of the SCK and input data on the SDI pin is latched on the rising edge of the SC.

#### 8.5.2.2 $\overline{CS}$

The  $\overline{CS}$  activates the SPI. As long as the  $\overline{CS}$  signal is at high level, the TMAG5170D-Q1 will not accept the SCK signal or the Serial-data-in (SDI), and the Serial-data-out (SDO) is in high impedance. Hold  $\overline{CS}$  low for the duration of a communication frame without toggling to ensure proper communication. The SPI is disabled each time  $\overline{CS}$  is brought from low to high.

#### 8.5.2.3 SDI

The Serial-data-in (SDI) line is used by the controller to configure the user access registers, start a new conversion, or send a read command. The SDI bits are transmitted with each SCK rising edge when the  $\overline{CS}$  pin is low. Figure 8-10 explains the SDI frame details. There are four command bits in the SDI line to select the status bit for the next frame or start a new conversion.



CMD0	CMD0 = 0	No conversion start through command bits
	CMD0 = 1	Start of conversion at the CS going high
CMD1	CMD1 = 0	Display SET_COUNT [2:0] in STAT [2:0] bits at SDO next frame
	CMD1 = 1	Display DATA_TYPE [2:0] in STAT [2:0] bits at SDO next frame

- \* CMD2 & CMD3 are reserved bits
- \*\* SET\_COUNT register bits indicate the rolling count of the conversion data set. The counter is reset after 111b.
- \*\*\* DATA\_TYPE register bits indicate the type of data being read through the SDO line

**Figure 8-10. 32-Bit Frame Definition of the SDI Line**

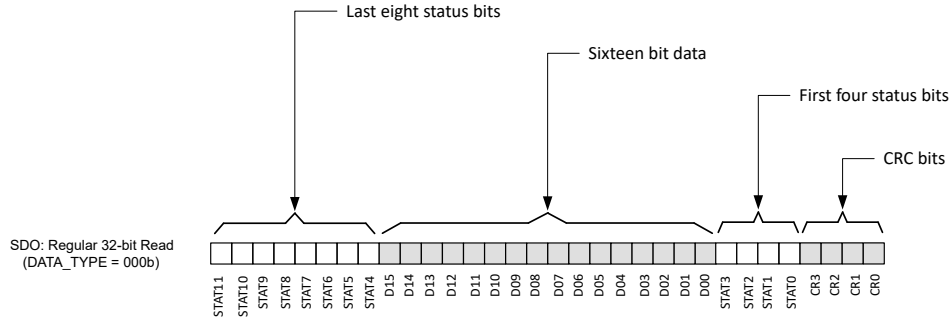
### 8.5.2.4 SDO

The Serial-data-out (SDO) line is used by the controller to read the data from the TMAG5170D-Q1. The TMAG5170D-Q1 will shift out command responses and ADC conversion data serially with each rising SCK edge when the  $\overline{CS}$  pin is low. This pin assumes a high-impedance state when  $\overline{CS}$  is high. Based off the DATA\_TYPE bit setting, the TMAG5170D-Q1 supports two different SDO frames:

- [Regular 32-Bit SDO Read](#)
- [Special 32-Bit SDO Read](#)

#### 8.5.2.4.1 Regular 32-Bit SDO Read

With DATA\_TYPE = 000b, the TMAG5170D-Q1 supports a regular 16-bit register read during the 32-bit SDO frame as explained in [Figure 8-11](#). In this read mode, 12-bit status bits are displayed. All the status bits except for the ERROR\_STAT bit are directly read from the status registers. The ERROR\_STAT bit indicates if any error bit set in the device. [Figure 8-11](#) shows how the status bits STAT[2:0] can be changed based off CMD1 value in the previous frame.



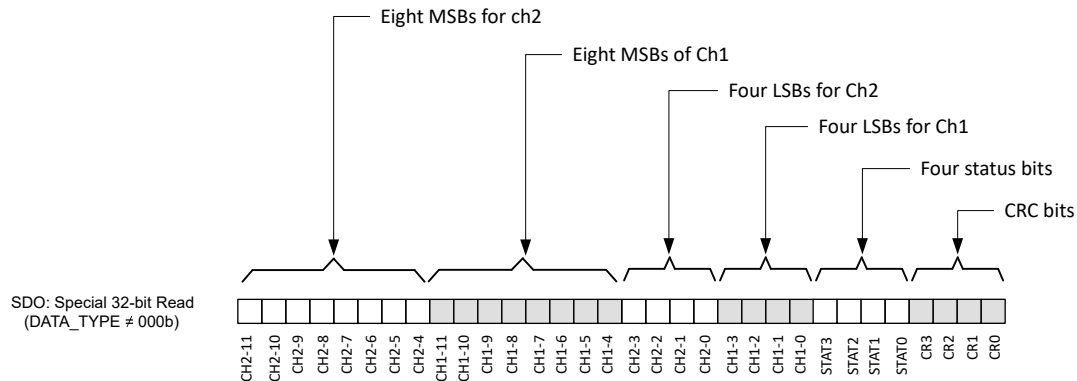
STAT11	STAT10	STAT9	STAT8	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
PREV_CRC_STAT	CFG_RESET	ALRT_STATUS1	ALRT_STATUS0	X	Y	Z	T	ERROR_STAT	Follows CMD1 instruction from previous frame		

- \* PREV\_CRC\_STAT indicates if there is any CRC error in the immediate past frame
- \*\* ERROR\_STAT indicates if there is any error bit flipped in the part
- \*\*\* STAT10 to STAT4 indicate select status bits from the CONV\_STATUS and AFE\_STATUS registers

**Figure 8-11. Regular 32-Bit SDO Read**

#### 8.5.2.4.2 Special 32-Bit SDO Read

With DATA\_TYPE > 000b, the TMAG5170D-Q1 supports a special 32-bit SDO frame for two-channel simultaneous data read. Each channel data is limited to 12 bits. This feature is useful for systems requiring faster data throughput while performing multi-axis measurements. Figure 8-12 explains the detail construction of the special 32-bit SDO frame. When the device is set to special 32-bit read, the device will continue to deliver the 2-channel data set through the SDO line during consecutive read or write cycles. DATA\_TYPE bits must be reset to get back to a regular read cycle. Only four status bits are transmitted in this mode. All the status bits except for the ERROR\_STAT bit are directly read from the status registers. The ERROR\_STAT bit indicates if any error bit set in the device. The status bits, STAT[2:0], can be changed based off CMD1 value in the previous frame.



STAT3	STAT2	STAT1	STAT0
ERROR_STAT	Follows CMD1 instruction from previous frame		

- \* ERROR\_STAT indicates if there is any error bit set in the device

**Figure 8-12. Special 32-Bit SDO Read**



### 8.5.2.5 SPI CRC

The TMAG5170D-Q1 performs mandatory CRC for SPI communication. The data integrity is maintained in both directions by a 4-bit CRC covering the content of the incoming and outgoing 32-bit messages. The four LSB bits of each 32-bit SPI frame are dedicated for the CRC. The CRC code is generated by the polynomial  $x^4 + x + 1$ . Initialize the CRC bits with b1111.

During the SDI write frame, the TMAG5170D-Q1 reads for the CRC data before executing a write instruction. The write instruction from the controller is ignored if there is any CRC error present in the frame. During the SDI regular read frame, the TMAG5170D-Q1 starts to deliver the requested data through SDO line in the same frame and notifies the controller of any error occurrence through the ERROR\_STAT bit. If the device detects a CRC error in the SDI line, the device will invert the last bit of the SDO CRC in the same frame to promptly signal to a controller that the SPI communication is compromised. A controller can also determine the presence of a CRC error in the SDI frame by checking the Status11 bit in the next regular read frame.

#### Note

The TMAG5170D-Q1 default mode at power up is CRC-enabled. With CRC enabled, the device will ignore all the SDI commands if proper CRC codes are not received. To disable the CRC at the SDI line, send the SPI SDI command x0F000407.

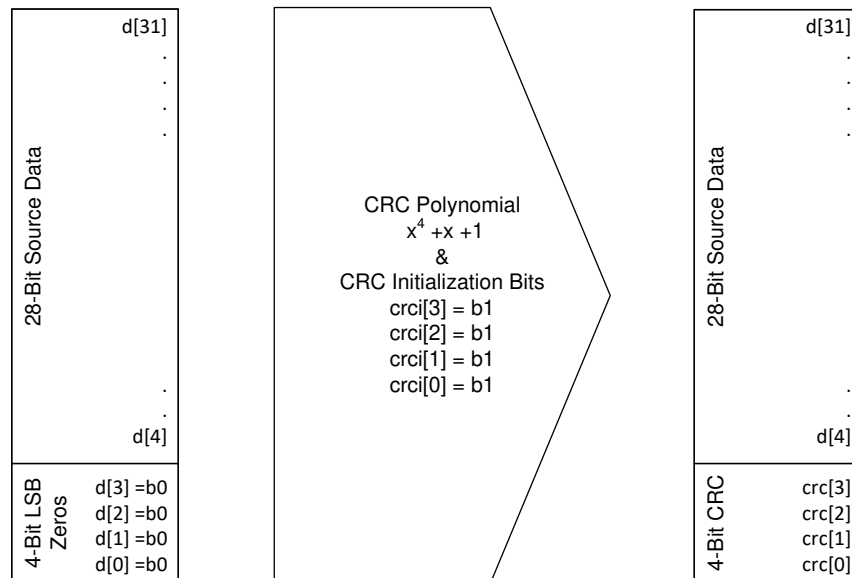


Figure 8-13. 4-Bit CRC Calculation

Use the following XOR function equations to calculate the 4-bit CRC. Figure 8-13 describes the notations of these equations.

$$crc[0] = d[30] \wedge d[26] \wedge d[25] \wedge d[24] \wedge d[23] \wedge d[21] \wedge d[19] \wedge d[18] \wedge d[15] \wedge d[11] \wedge d[10] \wedge d[9] \wedge d[8] \wedge d[6] \wedge d[4] \wedge d[3] \wedge d[0] \wedge crci[2] \quad (10)$$

$$crc[1] = d[31] \wedge d[30] \wedge d[27] \wedge d[23] \wedge d[22] \wedge d[21] \wedge d[20] \wedge d[18] \wedge d[16] \wedge d[15] \wedge d[12] \wedge d[8] \wedge d[7] \wedge d[6] \wedge d[5] \wedge d[3] \wedge d[1] \wedge d[0] \wedge crci[2] \wedge crci[3] \quad (11)$$

$$crc[2] = d[31] \wedge d[28] \wedge d[24] \wedge d[23] \wedge d[22] \wedge d[21] \wedge d[19] \wedge d[17] \wedge d[16] \wedge d[13] \wedge d[9] \wedge d[8] \wedge d[7] \wedge d[6] \wedge d[4] \wedge d[2] \wedge d[1] \wedge crci[0] \wedge crci[3] \quad (12)$$

$$crc[3] = d[29] \wedge d[25] \wedge d[24] \wedge d[23] \wedge d[22] \wedge d[20] \wedge d[18] \wedge d[17] \wedge d[14] \wedge d[10] \wedge d[9] \wedge d[8] \wedge d[7] \wedge d[5] \wedge d[3] \wedge d[2] \wedge crci[1] \quad (13)$$

The following shows example codes for calculating the 4-bit CRC.

```
function logic [3:0] calculate_crc4;
    input logic [27:0] frame;

    logic [31:0]    padded_frame;
    logic [3:0]    frame_crc;
    logic          inv;
    integer        i;

    padded_frame = {frame, 4'b0000};

    begin
        frame_crc = 4'hf; // initial value
        for (i=31; i >= 0; i=i-1) begin
            inv = padded_frame[i] ^ frame_crc[3];
            frame_crc[3] = frame_crc[2];
            frame_crc[2] = frame_crc[1];
            frame_crc[1] = frame_crc[0] ^ inv;
            frame_crc[0] = inv;
        end
        return frame_crc;
    end
endfunction
```

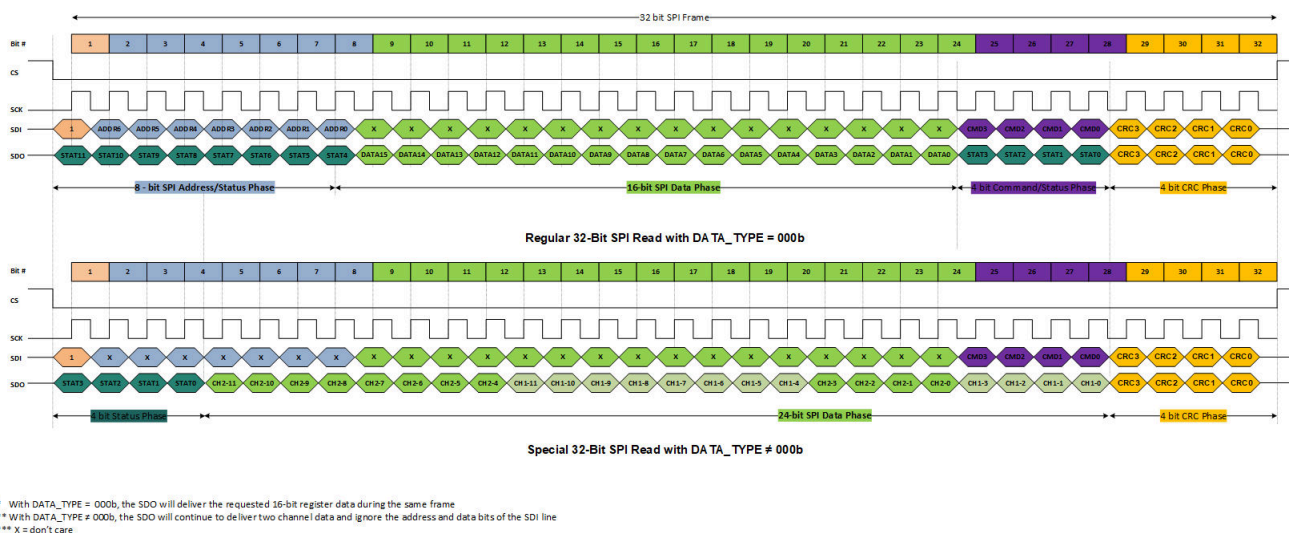
### 8.5.2.6 SPI Frame

With the flexible definition of the 32-bit frames, the TMAG5170D-Q1 supports a wide array of application requirements catering to multiple user-specific data throughout. Two different frame examples are shown in this section to illustrate the complete SPI bus communication:

- [32-Bit Read Frame](#)
- [32-Bit Write Frame](#)

#### 8.5.2.6.1 32-Bit Read Frame

Figure 8-14 shows both regular and special SDO frames during SDI read command. The TMAG5170D-Q1 implements in-frame communication. When the controller sends a register read command during a regular read cycle, the corresponding 16-bit register data is sent through the SDO line in the same frame. During the special read cycle, the TMAG5170D-Q1 ignores the address and data bits of the SDI line and sends the two channel data set through the SDO line as defined in the DATA\_TYPE register bits.

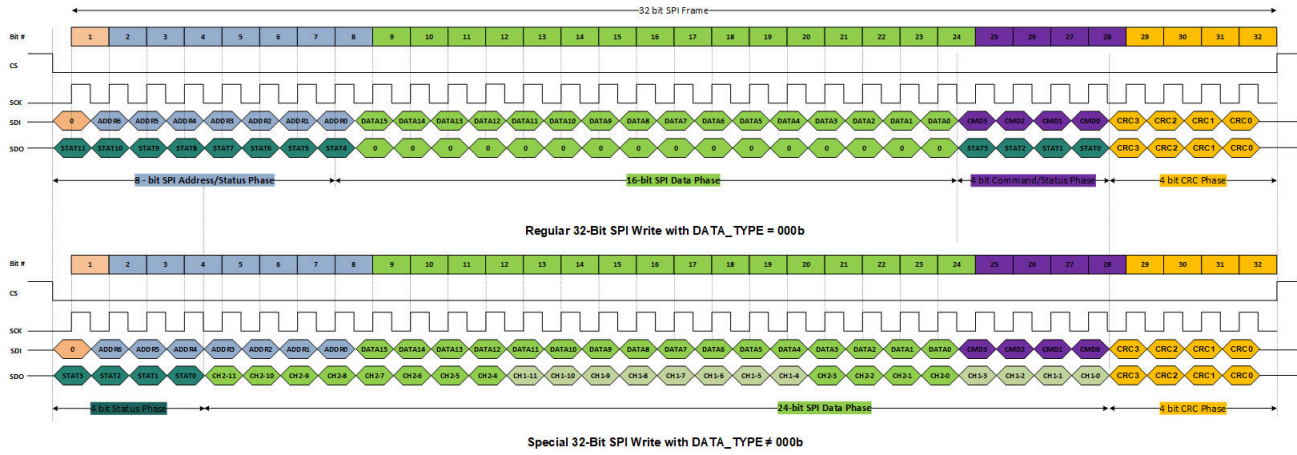


**Figure 8-14. 32-Bit SPI Read**

#### 8.5.2.6.2 32-Bit Write Frame

Figure 8-15 shows both regular and special SDO frames during SDI write command. During a regular 32-bit frame write command through SDI, the SDO delivers '0's in place of 16-bit data placeholders. During the special

frame write cycle through SDI line, the TMAG5170D-Q1 will continue to send the two channel data through SDO line as defined by the DATA\_TYPE register bits.



\* With DATA\_TYPE = 000b, the SDO will deliver '0's in the 16-bit register data during the same frame  
 \*\* With DATA\_TYPE ≠ 000b, the SDO will continue to deliver two channel data during either read or write frame

**Figure 8-15. 32-Bit Write Frame**

## 8.6 Register Map

### 8.6.1 TMAG5170D-Q1 Registers

Table 8-4 lists the memory-mapped registers for the TMAG5170D-Q1 registers. All register offset addresses not listed in Table 8-4 should be considered as reserved locations and the register contents should not be modified.

**Table 8-4. TMAG5170D-Q1 Registers**

Offset	Acronym	Register Name	Section
0h	DEVICE_CONFIG	Configure Device Operation Modes	DEVICE_CONFIG Register (Offset = 0h) [Reset = 0000h]
1h	SENSOR_CONFIG	Configure Device Operation Modes	SENSOR_CONFIG Register (Offset = 1h) [Reset = 0000h]
2h	SYSTEM_CONFIG	Configure Device Operation Modes	SYSTEM_CONFIG Register (Offset = 2h) [Reset = 0000h]
3h	ALERT_CONFIG	Configure Device Operation Modes	ALERT_CONFIG Register (Offset = 3h) [Reset = 0000h]
4h	X_THRX_CONFIG	Configure Device Operation Modes	X_THRX_CONFIG Register (Offset = 4h) [Reset = 7D83h]
5h	Y_THRX_CONFIG	Configure Device Operation Modes	Y_THRX_CONFIG Register (Offset = 5h) [Reset = 7D83h]
6h	Z_THRX_CONFIG	Configure Device Operation Modes	Z_THRX_CONFIG Register (Offset = 6h) [Reset = 7D83h]
7h	T_THRX_CONFIG	Configure Device Operation Modes	T_THRX_CONFIG Register (Offset = 7h) [Reset = 6732h]
8h	CONV_STATUS	Conversion Status Register	CONV_STATUS Register (Offset = 8h) [Reset = 0000h]
9h	X_CH_RESULT	Conversion Result Register	X_CH_RESULT Register (Offset = 9h) [Reset = 0000h]
Ah	Y_CH_RESULT	Conversion Result Register	Y_CH_RESULT Register (Offset = Ah) [Reset = 0000h]
Bh	Z_CH_RESULT	Conversion Result Register	Z_CH_RESULT Register (Offset = Bh) [Reset = 0000h]
Ch	TEMP_RESULT	Conversion Result Register	TEMP_RESULT Register (Offset = Ch) [Reset = 0000h]
Dh	AFE_STATUS	Status Register	AFE_STATUS Register (Offset = Dh) [Reset = 8000h]
Eh	SYS_STATUS	Status Register	SYS_STATUS Register (Offset = Eh) [Reset = 0000h]
Fh	TEST_CONFIG	Test Configuration Register	TEST_CONFIG Register (Offset = Fh) [Reset = X]

**Table 8-4. TMAG5170D-Q1 Registers (continued)**

Offset	Acronym	Register Name	Section
10h	OSC_MONITOR	Conversion Result Register	<a href="#">OSC_MONITOR Register (Offset = 10h) [Reset = 0000h]</a>
11h	MAG_GAIN_CONFIG	Configure Device Operation Modes	<a href="#">MAG_GAIN_CONFIG Register (Offset = 11h) [Reset = 0000h]</a>
12h	MAG_OFFSET_CONFIG	Configure Device Operation Modes	<a href="#">MAG_OFFSET_CONFIG Register (Offset = 12h) [Reset = 0000h]</a>
13h	ANGLE_RESULT	Conversion Result Register	<a href="#">ANGLE_RESULT Register (Offset = 13h) [Reset = 0000h]</a>
14h	MAGNITUDE_RESULT	Conversion Result Register	<a href="#">MAGNITUDE_RESULT Register (Offset = 14h) [Reset = 0000h]</a>

Complex bit access types are encoded to fit into small table cells. [Table 8-5](#) shows the codes that are used for access types in this section.

**Table 8-5. TMAG5170D-Q1 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

### 8.6.1.1 DEVICE\_CONFIG Register (Offset = 0h) [Reset = 0000h]

DEVICE\_CONFIG is shown in [Table 8-6](#).

Return to the [Summary Table](#).

**Table 8-6. DEVICE\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	CONV_AVG	R/W	0h	Enables additional sampling of the sensor data to reduce the noise effect (or to increase resolution) 0h = 1x - 10.0 kSPS (3-axes) or 20 kSPS (1 axis) 1h = 2x - 5.7 kSPS (3-axes) or 13.3 kSPS (1 axis) 2h = 4x - 3.1 kSPS (3-axes) or 8.0 kSPS (1 axis) 3h = 8x - 1.6 kSPS (3-axes) or 4.4 kSPS (1 axis) 4h = 16x - 0.8 kSPS (3-axes) or 2.4 kSPS (1 axis) 5h = 32x - 0.4 kSPS (3-axes) or 1.2 kSPS (1 axis) 6h = Code not used, defaults to 000b if selected 7h = Code not used, defaults to 000b if selected
11-10	RESERVED	R	0h	Reserved
9-8	MAG_TEMPCO	R/W	0h	Temperature coefficient of sense magnet 0h = 0%/ deg C (Current sensor applications) 1h = 0.12%/deg C (NdBFe) 2h = 0.03% /deg C (SmCo) 3h = 0.2%/deg C (Ceramic)
7	RESERVED	R	0h	Reserved
6-4	OPERATING_MODE	R/W	0h	Selects operating mode 0h = Configuration mode, Default (TRIGGER_MODE active) 1h = Stand-by mode (TRIGGER_MODE active) 2h = Active measure mode (Continuous conversion) 3h = Active trigger mode (TRIGGER_MODE active) 4h = Wake-up and sleep mode (duty-cycled mode) 5h = Sleep mode 6h = Deep sleep mode (wakes up at CS signal from controller) 7h = Code not used, defaults to 000b if selected
3	T_CH_EN	R/W	0h	Enables temperature compensation of the sensor data. Set this bit to '1b' for precision performance. If only temperature channel is enabled, the CONV_AVG register bits need to set at 000b. 0h = Temp channel disabled, Default 1h = Temp channel enabled
2	T_RATE	R/W	0h	Temperature conversion rate. It is linked to the CONV_AVG field 0h = Same as other sensors per CONV_AVG, Default 1h = Once per conversion set
1	T_HLT_EN	R/W	0h	Enables temperature limit check 0h = Temperature limit check off, Default 1h = Temperature limit check on
0	RESERVED	R	0h	Reserved

### 8.6.1.2 SENSOR\_CONFIG Register (Offset = 1h) [Reset = 0000h]

SENSOR\_CONFIG is shown in [Table 8-7](#).

Return to the [Summary Table](#).

**Table 8-7. SENSOR\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	ANGLE_EN	R/W	0h	Enable angle calculation using two axis data 0h = No angle calculation (default) 1h = X-Y-angle calculation enabled 2h = Y-Z-angle calculation enabled 3h = X-Z-angle calculation enabled
13-10	SLEEPTIME	R/W	0h	Selects the time spent in low power mode between conversions when OPERATING_MODE = 010b 0h = 1 ms 1h = 5 ms 2h = 10 ms 3h = 15 ms 4h = 20 ms 5h = 30 ms 6h = 50 ms 7h = 100 ms 8h = 500 ms 9h = 1000 ms Ah = Code not used, defaults to 0000b if selected Bh = Code not used, defaults to 0000b if selected Ch = Code not used, defaults to 0000b if selected Dh = Code not used, defaults to 0000b if selected Eh = Code not used, defaults to 0000b if selected Fh = Code not used, defaults to 0000b if selected
9-6	MAG_CH_EN	R/W	0h	Enables data acquisition of the magnetic axis channel(s) 0h = All magnetic channels of OFF, DEFAULT 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channels enabled 4h = Z channel enabled 5h = Z, X channels enabled 6h = Y, Z channels enabled 7h = X, Y, Z channels enabled 8h = XYX channels enabled 9h = YXY channels enabled Ah = YZY channels enabled Bh = ZYZ channels enabled Ch = ZXZ channels enabled Dh = XZX channels enabled Eh = XYZYX channels enabled Fh = XYZZYX channels enabled
5-4	Z_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from $\pm 25$ mT to $\pm 300$ mT 0h = $\pm 50$ mT (TMAG5170A1)/ $\pm 150$ mT(TMAG5170A2), Default 1h = $\pm 25$ mT (TMAG5170A1)/ $\pm 75$ mT(TMAG5170A2) 2h = $\pm 100$ mT (TMAG5170A1)/ $\pm 300$ mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected
3-2	Y_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from $\pm 25$ mT to $\pm 300$ mT 0h = $\pm 50$ mT (TMAG5170A1)/ $\pm 150$ mT(TMAG5170A2), Default 1h = $\pm 25$ mT (TMAG5170A1)/ $\pm 75$ mT(TMAG5170A2) 2h = $\pm 100$ mT (TMAG5170A1)/ $\pm 300$ mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected

**Table 8-7. SENSOR\_CONFIG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
1-0	X_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from $\pm 25$ mT to $\pm 300$ mT 0h = $\pm 50$ mT (TMAG5170A1)/ $\pm 150$ mT(TMAG5170A2), Default 1h = $\pm 25$ mT (TMAG5170A1)/ $\pm 75$ mT(TMAG5170A2) 2h = $\pm 100$ mT (TMAG5170A1)/ $\pm 300$ mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected

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### 8.6.1.3 SYSTEM\_CONFIG Register (Offset = 2h) [Reset = 0000h]

SYSTEM\_CONFIG is shown in [Table 8-8](#).

Return to the [Summary Table](#).

**Table 8-8. SYSTEM\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-12	DIAG_SEL	R/W	0h	Selects a diagnostic mode run 0h = Run all data path diagnostics all together, Default 1h = Run only enabled data path diagnostics all together 2h = Run all data path diagnostics in sequence 3h = Run only enabled data path diagnostics in sequence
11	RESERVED	R	0h	Reserved
10-9	TRIGGER_MODE	R/W	0h	Selects a condition which initiates a single conversion based off already configured registers. A running conversion completes before executing a trigger. Redundant triggers are ignored. TRIGGER_MODE is available only during the modes explicitly mentioned in OPERATING_MODE. 0h = Conversion start at SPI command, Default 1h = Conversion start at $\overline{CS}$ pulse 2h = Conversion start at $\overline{ALERT}$ pulse 3h = Code not used, defaults to 00b if selected
8-6	DATA_TYPE	R/W	0h	Data Type to be accessed from results registers via SPI 0h = Default 32-bit register access 1h = 12-Bit XY data access 2h = 12-Bit XZ data access 3h = 12-Bit ZY data access 4h = 12-Bit XT data access 5h = 12-Bit YT data access 6h = 12-Bit ZT data access 7h = 12-Bit AM data access
5	DIAG_EN	R/W	0h	Enables user controlled AFE diagnostic tests 0h = Execution of AFE diagnostics is disabled, Default 1h = Execution of AFE diagnostics is enabled
4-3	RESERVED	R	0h	Reserved
2	Z_HLT_EN	R/W	0h	Enables magnetic field limit check on Z axis 0h = Z axis limit check off, Default 1h = Z axis limit check on
1	Y_HLT_EN	R/W	0h	Enables magnetic field limit check on Y axis 0h = Y axis limit check off, Default 1h = Y axis limit check on
0	X_HLT_EN	R/W	0h	Enables magnetic field limit check on X axis 0h = X axis limit check off, Default 1h = X axis limit check on

### 8.6.1.4 ALERT\_CONFIG Register (Offset = 3h) [Reset = 0000h]

ALERT\_CONFIG is shown in [Table 8-9](#).

Return to the [Summary Table](#).

**Table 8-9. ALERT\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	ALERT_LATCH	R/W	0h	Latched $\overline{\text{ALERT}}$ mode select 0h = $\overline{\text{ALERT}}$ sources are not latched. $\overline{\text{ALERT}}$ is asserted only while the source of the $\overline{\text{ALERT}}$ response is present 1h = $\overline{\text{ALERT}}$ sources are latched. $\overline{\text{ALERT}}$ response is latched when the source of the $\overline{\text{ALERT}}$ is asserted until cleared on Read of the corresponding status register (AFE_STATUS, SYS_STATUS, or result registers)
12	ALERT_MODE	R/W	0h	ALERT mode select 0h = Interrupt mode 1h = Switch mode. This mode overrides any interrupt function (ALERT trigger is also disabled), and implements Hall switch function based off the *_THR*_ALRT settings. In the switch mode the corresponding X_HLT_EN, Y_HLT_EN, Z_HLT_EN need to be set.
11	STATUS_ALRT	R/W	0h	Enable $\overline{\text{ALERT}}$ response when any flag in the AFE_STATUS or SYS_STATUS registers are set 0h = $\overline{\text{ALERT}}$ is not asserted when any of the AFE_STATUS or SYS_STATUS bit is set 1h = $\overline{\text{ALERT}}$ output is asserted when any of the AFE_STATUS or SYS_STATUS bit is set
10-9	RESERVED	R	0h	Reserved
8	RSLT_ALRT	R/W	0h	Enable $\overline{\text{ALERT}}$ response when the configured set of conversions is complete 0h = $\overline{\text{ALERT}}$ is not used to signal when the configured set of conversions are complete 1h = $\overline{\text{ALERT}}$ output is asserted when the configured set of conversions are complete
7-6	RESERVED	R	0h	Reserved
5-4	THR*_COUNT	R/W	0h	Number of conversions above the HIGH threshold or below the LOW threshold before the $\overline{\text{ALERT}}$ response is initiated 0h = 1-Conversion result 1h = 2-Conversion results 2h = 3-Conversion results 3h = 4-Conversion results
3	T_THR*_ALRT	R/W	0h	Temperature threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when temperature thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when temperature thresholds are crossed
2	Z_THR*_ALRT	R/W	0h	Z-Channel threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when Z-Axis magnetic thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when Z-Axis magnetic thresholds are crossed
1	Y_THR*_ALRT	R/W	0h	Y-Channel threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when Y-Axis magnetic thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when Y-Axis magnetic thresholds are crossed
0	X_THR*_ALRT	R/W	0h	X-Channel threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when X-Axis magnetic thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when X-Axis magnetic thresholds are crossed

### 8.6.1.5 X\_THRX\_CONFIG Register (Offset = 4h) [Reset = 7D83h]

X\_THRX\_CONFIG is shown in [Table 8-10](#).

Return to the [Summary Table](#).

**Table 8-10. X\_THRX\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	X_HI_THRESHOLD	R/W	7Dh	X-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: $(X\_RANGE/128)*X\_HI\_THRESHOLD$ . Default to 98% of the full-scale
7-0	X_LO_THRESHOLD	R/W	83h	X-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: $(X\_RANGE/128)*X\_LO\_THRESHOLD$ . Default to -98% of the full-scale

### 8.6.1.6 Y\_THRX\_CONFIG Register (Offset = 5h) [Reset = 7D83h]

Y\_THRX\_CONFIG is shown in [Table 8-11](#).

Return to the [Summary Table](#).

**Table 8-11. Y\_THRX\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	Y_HI_THRESHOLD	R/W	7Dh	Y-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: $(Y\_RANGE/128)*Y\_HI\_THRESHOLD$ . Default to 98% of the full-scale.
7-0	Y_LO_THRESHOLD	R/W	83h	Y-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: $(Y\_RANGE/128)*Y\_LO\_THRESHOLD$ . Default to -98% of the full-scale.

### 8.6.1.7 Z\_THRX\_CONFIG Register (Offset = 6h) [Reset = 7D83h]

Z\_THRX\_CONFIG is shown in [Table 8-12](#).

Return to the [Summary Table](#).

**Table 8-12. Z\_THRX\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	Z_HI_THRESHOLD	R/W	7Dh	Z-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: $(Z\_RANGE/128) * Z\_HI\_THRESHOLD$ . Default to 98% of the full-scale
7-0	Z_LO_THRESHOLD	R/W	83h	Z-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: $(Z\_RANGE/128) * X\_LO\_THRESHOLD$ . Default to -98% of the full-scale

### 8.6.1.8 T\_THRX\_CONFIG Register (Offset = 7h) [Reset = 6732h]

T\_THRX\_CONFIG is shown in [Table 8-13](#).

Return to the [Summary Table](#).

**Table 8-13. T\_THRX\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-8	T_HI_THRESHOLD	R/W	67h	Temperature maximum threshold. User input as 2's complement 8-bit binary number. Each LSB in this field corresponds to 4.267°C. Default value of 67h represents 172°C.
7-0	T_LO_THRESHOLD	R/W	32h	Temperature minimum threshold. User input as 2's complement 8-bit binary number. Each LSB in this field corresponds to 4.267°C. Default value of 32h represents -53°C.

### 8.6.1.9 CONV\_STATUS Register (Offset = 8h) [Reset = 0000h]

CONV\_STATUS is shown in [Table 8-14](#).

Return to the [Summary Table](#).

**Table 8-14. CONV\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RDY	R	0h	Conversion data buffer is ready. 0h = Conversion data not valid (result registers hold previous conversion value) 1h = Conversion data valid
12	A	R	0h	Angle/Magnitude data from current conversion 0h = Data is not current 1h = Data is current
11	T	R	0h	Temperature data from current conversion 0h = Temperature data is not current 1h = Temperature data is current
10	Z	R	0h	Z-Channel data from current conversion 0h = Z-Channel data is not current 1h = Z-Channel data is current
9	Y	R	0h	Y-Channel data from current conversion 0h = Y-Channel data is not current 1h = Y-Channel data is current
8	X	R	0h	X-Channel data from current conversion 0h = X-Channel data is not current 1h = X-Channel data is current
7	RESERVED	R	0h	Reserved
6-4	SET_COUNT	R	0h	Rolling count of conversion data sets
3-2	RESERVED	R	0h	Reserved
1-0	ALRT_STATUS	R	0h	State of $\overline{\text{ALERT}}$ response 0h = No $\overline{\text{ALERT}}$ conditions 1h = AFE status flag set 2h = SYS status flag set 3h = Flags set in both AFE and SYS status registers

### 8.6.1.10 X\_CH\_RESULT Register (Offset = 9h) [Reset = 0000h]

X\_CH\_RESULT is shown in [Table 8-15](#).

Return to the [Summary Table](#).

**Table 8-15. X\_CH\_RESULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	X_CH_RESULT	R	0h	X-Channel data conversion results



### 8.6.1.11 Y\_CH\_RESULT Register (Offset = Ah) [Reset = 0000h]

Y\_CH\_RESULT is shown in [Table 8-16](#).

Return to the [Summary Table](#).

**Table 8-16. Y\_CH\_RESULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	Y_CH_RESULT	R	0h	Y-Channel data conversion results

### 8.6.1.12 Z\_CH\_RESULT Register (Offset = Bh) [Reset = 0000h]

Z\_CH\_RESULT is shown in [Table 8-17](#).

Return to the [Summary Table](#).

**Table 8-17. Z\_CH\_RESULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	Z_CH_RESULT	R	0h	Z-Channel data conversion results

### 8.6.1.13 TEMP\_RESULT Register (Offset = Ch) [Reset = 0000h]

TEMP\_RESULT is shown in [Table 8-18](#).

Return to the [Summary Table](#).

**Table 8-18. TEMP\_RESULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	TEMP_RESULT	R	0h	Temperature sensor data conversion results

### 8.6.1.14 AFE\_STATUS Register (Offset = Dh) [Reset = 8000h]

AFE\_STATUS is shown in [Table 8-19](#).

Return to the [Summary Table](#).

**Table 8-19. AFE\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	CFG_RESET	RC	1h	Device power up status. This bit is reset when microcontroller reads the AFE_STATUS register. 0h = Device reset has been acknowledged and cleared 1h = Device has experienced a hardware reset after a power down or brown-out
14-13	RESERVED	R	0h	Reserved
12	SENS_STAT	RC	0h	Analog front end sensor diagnostic status 0h = No error detected 1h = Analog front end sensor diagnostic test failed
11	TEMP_STAT	RC	0h	Temperature sensor diagnostic status 0h = No error detected 1h = Analog front end temperature sensor diagnostic test failed
10	ZHS_STAT	RC	0h	Z-Axis hall sensor diagnostic status 0h = No error detected 1h = Z-Axis hall sensor diagnostic test failed
9	YHS_STAT	RC	0h	Y-Axis hall sensor diagnostic status 0h = No error detected 1h = Y-Axis hall sensor diagnostic test failed
8	XHS_STAT	RC	0h	X-Axis hall sensor diagnostic status 0h = No error detected 1h = X-Axis hall sensor diagnostic test failed
7-2	RESERVED	R	0h	Reserved
1	TRIM_STAT	RC	0h	Trim data error 0h = No trim data errors were detected 1h = Trim data error was detected
0	LDO_STAT	RC	0h	LDO error 0h = No faults in the internal LDO supplied power were detected 1h = A fault in the internal LDO supplied power was detected

### 8.6.1.15 SYS\_STATUS Register (Offset = Eh) [Reset = 0000h]

SYS\_STATUS is shown in [Table 8-20](#).

Return to the [Summary Table](#).

**Table 8-20. SYS\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ALRT_LVL	R	0h	Reflects the current state of the $\overline{\text{ALERT}}$ pin feed-back path 0h = The input $\overline{\text{ALERT}}$ logic level is low 1h = The input $\overline{\text{ALERT}}$ logic level is high
14	ALRT_DRV	RC	0h	Each time the open drain $\overline{\text{ALERT}}$ signal is driven, the feedback circuit checks if the $\overline{\text{ALERT}}$ output goes Low. An error flag is generated at the ALRT_DRV bit if the output doesn't go Low. 0h = No $\overline{\text{ALERT}}$ drive error detected 1h = $\overline{\text{ALERT}}$ drive error detected
13	SDO_DRV	RC	0h	The Logic value driven output on SDO was not the value of the SDO Pin Feed-back path when SDO is being driven by the device 0h = No SDO drive error detected 1h = SDO drive error detected
12	CRC_STAT	RC	0h	Cyclic redundancy check error 0h = No cyclic redundancy check error was detected 1h = Cyclic redundancy check error was detected for a SPI transaction
11	FRAME_STAT	RC	0h	Incorrect number of clocks in SPI frame 0h = No frame error was detected 1h = Incorrect number of clocks detected for a SPI transaction
10-8	OPERATING_STAT	R	0h	Reports the status of operating mode 0h = Config state 1h = Standby state 2h = Active measure (Continuous Mode) state 3h = Active triggered mode state 4h = DCM active state 5h = DCM Sleep state 6h = Sleep state
7-6	RESERVED	R	0h	Reserved
5	VCC_OV	RC	0h	VCC over-voltage detection in active or stand-by mode 0h = No over-voltage detected on VCC 1h = VCC was detected to be over-voltage
4	VCC_UV	RC	0h	VCC under voltage detection in active or stand-by mode 0h = No under-voltage was detected on VCC 1h = VCC was detected to be under-voltage
3	TEMP_THX	RC	0h	Temperature threshold crossing detected 0h = No temperature threshold crossing detected 1h = Temperature threshold crossing detected
2	ZCH_THX	RC	0h	Z-Channel threshold crossing detected 0h = No Z-Axis magnetic field threshold crossing detected 1h = Z-Axis magnetic field threshold crossing detected
1	YCH_THX	RC	0h	Y-Channel threshold crossing detected 0h = No Y-Axis magnetic field threshold crossing detected 1h = Y-Axis magnetic field threshold crossing detected
0	XCH_THX	RC	0h	X-Channel threshold crossing detected 0h = No X-Axis magnetic field threshold crossing detected 1h = X-Axis magnetic field threshold crossing detected

**8.6.1.16 TEST\_CONFIG Register (Offset = Fh) [Reset = X]**

 TEST\_CONFIG is shown in [Table 8-21](#).

 Return to the [Summary Table](#).

**Table 8-21. TEST\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	1h	Reserved
5-4	VER	R	X	Indicates the version of the device 0h = A1 rev 1h = A2 rev 2h = reserved 3h = reserved
3	RESERVED	R	0h	Reserved
2	CRC_DIS	R/W	0h	Enable or disable CRC in SPI communication 0h = CRC enabled in SPI communication (Default) 1h = CRC disabled in SPI communication
1-0	OSC_CNT_CTL	R/W	0h	Oscillator count control - starts, stops, and resets the counter driven by the HFOSC or LFOSC oscillator to facilitate oscillator frequency and integrity checks 0h = Reset OSC counter (default) 1h = Start OSC counter driven by HFOSC 2h = Start OSC counter driven by LFOSC 3h = Stop OSC counter

### 8.6.1.17 OSC\_MONITOR Register (Offset = 10h) [Reset = 0000h]

OSC\_MONITOR is shown in [Table 8-22](#).

Return to the [Summary Table](#).

**Table 8-22. OSC\_MONITOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	OSC_COUNT	R	0h	Oscillator Counter. The number of selected oscillator clock cycles that have been counted since Oscillator Counter was started. The HFOSC and LFOSC clock roll-over the 16-bit counter once reaching the max value.

### 8.6.1.18 MAG\_GAIN\_CONFIG Register (Offset = 11h) [Reset = 0000h]

MAG\_GAIN\_CONFIG is shown in [Table 8-23](#).

Return to the [Summary Table](#).

**Table 8-23. MAG\_GAIN\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	GAIN_SELECTION	R/W	0h	Enables the selection of a particular Hall axis for amplitude correction to get accurate angle measurement 0h = No axis is selected (Default) 1h = X-axis is selected 2h = Y-axis is selected 3h = Z-axis is selected
13-11	RESERVED	R	0h	Reserved
10-0	GAIN_VALUE	R/W	0h	11-bit gain value determined by controller to adjust the a particular Hall axis value. The gain value is anywhere between 0 and 2. Gain is calculated as 'user entered value/1024'.



### 8.6.1.19 MAG\_OFFSET\_CONFIG Register (Offset = 12h) [Reset = 0000h]

MAG\_OFFSET\_CONFIG is shown in [Table 8-24](#).

Return to the [Summary Table](#).

**Table 8-24. MAG\_OFFSET\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-14	OFFSET_SELECTION	R/W	0h	Enables the selection of a particular Hall axis for offset correction to get accurate angle measurement: 00b = No axis is selected for offset correction (Default). 01b = Only OFFSET_VALUE1 is used for offset correction. Applied to X axis when ANGLE_EN = 01b or 11b, and to Y axis when ANGLE_EN = 10b. No axis is selected if ANGLE_EN = 00b. 10b = Only OFFSET_VALUE2 is used for offset correction. Applied to Y axis when ANGLE_EN = 01b, and to Z axis when ANGLE_EN = 10b or 11b. No axis is selected if ANGLE_EN = 00b. 11b = Both OFFSET_VALUE1 and OFFSET_VALUE2 are used for offset correction. OFFSET_VALUE1 applied to X axis when ANGLE_EN = 01b or 11b, and to Y axis when ANGLE_EN = 10b. OFFSET_VALUE2 applied to Y axis when ANGLE_EN = 01b, and to Z axis when ANGLE_EN = 10b or 11b. No axis is selected if ANGLE_EN = 00b.
13-7	OFFSET_VALUE1	R/W	0h	7-bit, 2' complement offset value determined by controller to adjust a particular Hall axis value. The range of possible offset valid entries can be +/-64. The offset value is calculated from the user input as the 7 LSB bits of a 11-bit range per SENSOR_CONFIG register setting for the corresponding axis. Default offset value is 0.
6-0	OFFSET_VALUE2	R/W	0h	7-bit, 2' complement offset value determined by controller to adjust a particular Hall axis value. The range of possible offset valid entries can be +/-64. The offset value is calculated from the user input as the 7 LSB bits of a 11-bit range per SENSOR_CONFIG register setting for the corresponding axis. Default offset value is 0.

### 8.6.1.20 ANGLE\_RESULT Register (Offset = 13h) [Reset = 0000h]

ANGLE\_RESULT is shown in [Table 8-25](#).

Return to the [Summary Table](#).

**Table 8-25. ANGLE\_RESULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	ANGLE_RESULT	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

**8.6.1.21 MAGNITUDE\_RESULT Register (Offset = 14h) [Reset = 0000h]**

MAGNITUDE\_RESULT is shown in [Table 8-26](#).

Return to the [Summary Table](#).

**Table 8-26. MAGNITUDE\_RESULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	MAGNITUDE_RESULT	R	0h	Resultant vector magnitude (during angle measurement) result. This value should be constant during 360 degree measurements

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Selecting the Sensitivity Option

Select the highest TMAG5170D-Q1 sensitivity option that can measure the required range of magnetic flux density so that the ADC output range is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations under the [TMAG5170-Q1 product folder](#) on ti.com.

#### 9.1.2 Temperature Compensation for Magnets

The TMAG5170D-Q1 temperature compensation is designed to directly compensate the average temperature drift of several magnets as specified in the MAG\_TEMP\_CO register bits. The residual induction ( $B_r$ ) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite magnets as the temperature increases. Set the MAG\_TEMP\_CO bit to default 00b if the device temperature compensation is not needed.

#### 9.1.3 Sensor Conversion

Multiple conversion schemes can be adopted based off the MAG\_CH\_EN, CONV\_AVG, DIAG\_SEL, and DIAG\_EN register bit settings.

##### 9.1.3.1 Continuous Conversion

The TMAG5170D-Q1 can be set in continuous conversion mode when OPERATING\_MODE is set to 010b. [Figure 9-1](#) shows few examples of continuous conversion. The input magnetic field is processed in two steps. In the first step the device spins the hall sensor elements, and integrates the sampled data. In the second step, the ADC block converts the analog signal into digital bits and stores in the corresponding result register. While the ADC starts processing the first magnetic sample, the spin block can start processing another magnetic sample. The temperature data is taken at the beginning of each new conversion. This temperature data is used to compensate for the magnetic thermal drift.

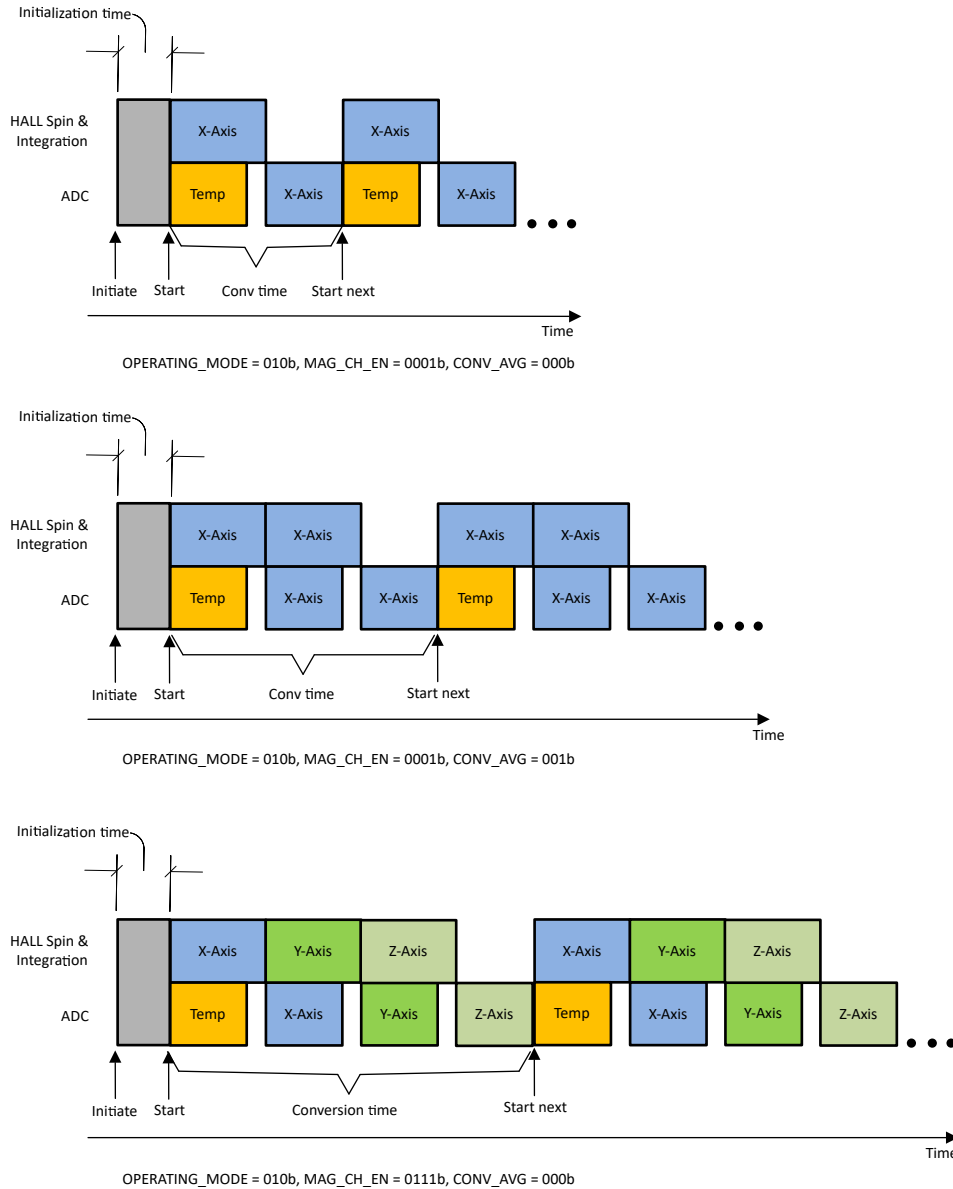
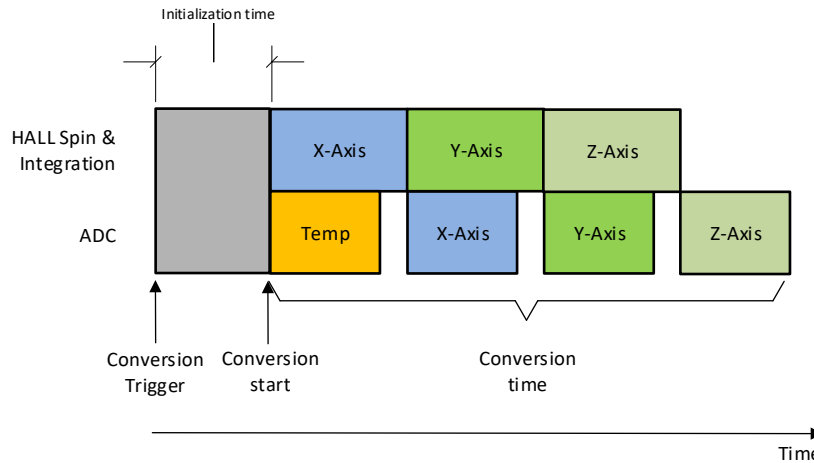


Figure 9-1. Continuous Conversion Examples

### 9.1.3.2 Trigger Conversion

The TMAG5170D-Q1 supports trigger conversion with OPERATING\_MODE set to 000b, 001b, or 011b. During trigger conversion, the initialization time can vary depending on the operating mode (see Table 8-3). The trigger event can be initiated through a SPI command,  $\overline{\text{ALERT}}$ , or  $\overline{\text{CS}}$  signal. Figure 9-2 shows an example of trigger conversion with X, Y, Z, and temperature sensors activated.



**Figure 9-2. Trigger Conversion for X, Y, Z, and Temperature Sensors**

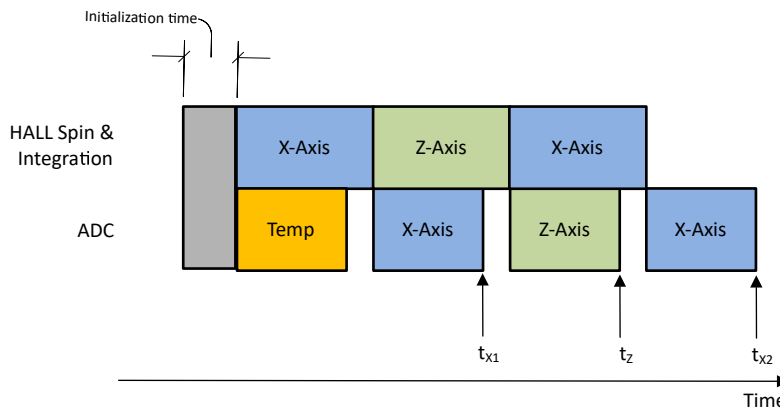
**9.1.3.3 Pseudo-Simultaneous Sampling**

In absolute angle measurement, application sensor data from multiple axes are required to calculate an accurate angle. The magnetic field data collected at different times through the same signal chain introduces error in angle calculation. The TMAG5170D-Q1 offers pseudo-simultaneous sampling data collection modes to eliminate this error. Figure 9-3 shows an example where MAG\_CH\_EN is set at 1101b to collect XZX data. Equation 14 shows that the time stamps for the X and Z sensor data are the same.

$$t_z = \frac{t_{x1} + t_{x2}}{2} \tag{14}$$

where

- $t_{x1}$ ,  $t_z$ ,  $t_{x2}$  are time stamps for X, Z, X sensor data completion as defined in Figure 9-3.



**Figure 9-3. XZX Magnetic Field Conversion**

The vertical X, Y sensors of the TMAG5170D-Q1 exhibit more noise than the horizontal Z sensor. The pseudo-simultaneous sampling can be used to equalize the noise floor when two set of vertical sensor data are collected against one set of horizontal sensor data, as in examples of XZX or YZY modes.

**9.1.4 Error Calculation During Linear Measurement**

The TMAG5170D-Q1 offers independent configurations to perform linear position measurements in X, Y, and Z axes. To calculate the expected error during linear measurement, the contributions from each of the individual error sources must be understood. The relevant error sources include sensitivity error, offset, noise, cross axis sensitivity, hysteresis, nonlinearity, drift across temperature, drift across life time, and so forth. For a 3-axis Hall

solution like the TMAG5170D-Q1, the cross-axis sensitivity and hysteresis error sources are insignificant. Use [Equation 15](#) to estimate the linear measurement error calculation at room temperature.

$$Error_{LM\_25C} = \frac{\sqrt{(B \times SENS_{ER})^2 + B_{off}^2 + N_{RMS\_25}^2}}{B} \times 100\% \quad (15)$$

where

- Error<sub>LM\_25C</sub> is total error in % during linear measurement at 25°C.
- B is input magnetic field.
- SENS<sub>ER</sub> is sensitivity error at 25°C.
- B<sub>off</sub> is offset error at 25°C.
- N<sub>RMS\_25</sub> is RMS noise at 25°C.

In many applications, system level calibration at room temperature can nullify the offset and sensitivity errors at 25°C. The noise errors can be reduced by further digital averaging the sensor data in a microcontroller. Use [Equation 15](#) to estimate the linear measurement error across temperature after calibration at room temperature.

$$Error_{LM\_Temp} = \frac{\sqrt{(B \times SENS_{DR})^2 + B_{off\_DR}^2 + N_{RMS\_Temp}^2}}{B} \times 100\% \quad (16)$$

where

- Error<sub>LM\_Temp</sub> is total error in % during linear measurement across temperature after room temperature calibration.
- B is input magnetic field.
- SENS<sub>DR</sub> is sensitivity drift from value at 25°C.
- B<sub>off\_DR</sub> is offset drift from value at 25°C.
- N<sub>RMS\_Temp</sub> is RMS noise across temperature.

If room temperature calibration is not performed, sensitivity and offset errors at room temperature must also account for total error calculation across temperature (see [Equation 17](#)).

$$Error_{LM\_Temp\_NCal} = \frac{\sqrt{(B \times SENS_{ER})^2 + (B \times SENS_{DR})^2 + B_{off}^2 + B_{off\_DR}^2 + N_{RMS\_Temp}^2}}{B} \times 100\% \quad (17)$$

where

- Error<sub>LM\_Temp\_NCal</sub> is total error in % during linear measurement across temperature without room temperature calibration.

### 9.1.5 Error Calculation During Angular Measurement

The TMAG5170D-Q1 offers on-chip CORDIC to measure angle data from any of the two magnetic axes. The linear magnetic axis data can be used to calculate the angle using an external CORDIC as well. To calculate the expected error during angular measurement, the contributions from each individual error source must be understood. The relevant error sources include sensitivity error, offset, noise, axis-axis mismatch, nonlinearity, drift across temperature, drift across life time, and so forth. Use the [Angle Error Calculation Tool](#) to estimate the total error during angular measurement.

## 9.2 Typical Application

Magnetic angle sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5170D-Q1 offers an on-chip angle calculator that can provide angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE\_EN register bits. The device offers an angle output in complete 360 degree scale. Take several error sources into account for angle calculation, including sensitivity error, offset error, linearity error, noise, mechanical vibration, temperature drift, and so forth.

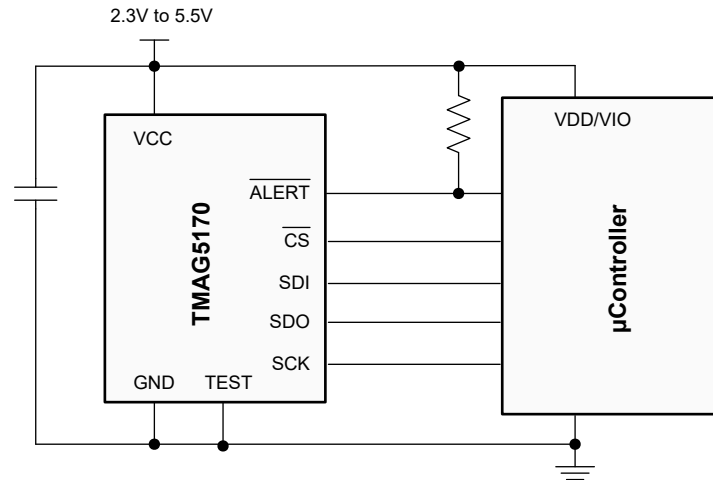


Figure 9-4. TMAG5170D-Q1 Application Diagram

### 9.2.1 Design Requirements

Use the parameters listed in [Table 9-1](#) for this design example

Table 9-1. Design Parameters

DESIGN PARAMETERS	ON-AXIS MEASUREMENT	OFF-AXIS MEASUREMENT
Device	TMAG5170-A1	TMAG5170-A1
VCC	5 V	5 V
Magnet	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<600	<600
Desired Accuracy	<1° for 360° rotation	<1° for 360° rotation

#### 9.2.1.1 Gain Adjustment for Angle Measurement

Common measurement topology include angular position measurements in on-axis or off-axis angular measurements shown in [Figure 9-5](#). Select the on-axis measurement topology whenever possible, as this offers the best optimization of magnetic field and the device measurement ranges. The TMAG5170D-Q1 offers an on-chip gain adjustment option to account for mechanical position misalignments.





Figure 9-5. On-Axis vs. Off-Axis Angle Measurements

### 9.2.2 Detailed Design Procedure

For accurate angle measurement, the two axes amplitudes must be normalized by selecting the proper gain adjustment value in the MAG\_GAN\_CONFIG register. The gain adjustment value is a fractional decimal number between 0 and 1. The following steps must be followed to calculate this fractional value:

1. Set the device at 32x average mode and rotate the shaft a full 360 degree.
2. Record the two axes sensor ADC codes for the full 360 degree rotation.
3. Measure the maximum peak-peak ADC code delta for each axis,  $A_x$  and  $A_y$ , as shown in [Figure 9-6](#) or [Figure 9-7](#).
4. Calculate the gain adjustment value for X axis:

$$G_x = \frac{A_y}{A_x} \quad (18)$$

5. If  $G_x > 1$ , apply the gain adjustment value to Y axis:

$$G_y = \frac{1}{G_x} \quad (19)$$

6. Calculate the target binary gain setting at the GAIN\_VALUE register bits:

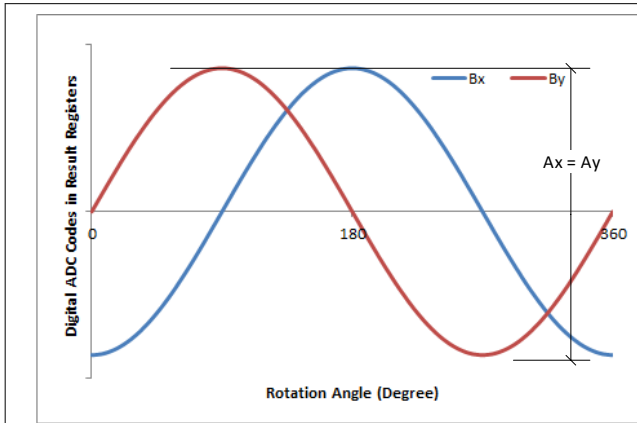
$$G_x \text{ or } G_y = \text{GAIN\_VALUE}_{\text{decimal}} / 1024 \quad (20)$$

**Example 1:** If  $A_x = A_y = 60,000$ , the GAIN\_SELECTION register bits can be set as 00b. The GAIN\_VALUE register bits are don't care bits in this case.

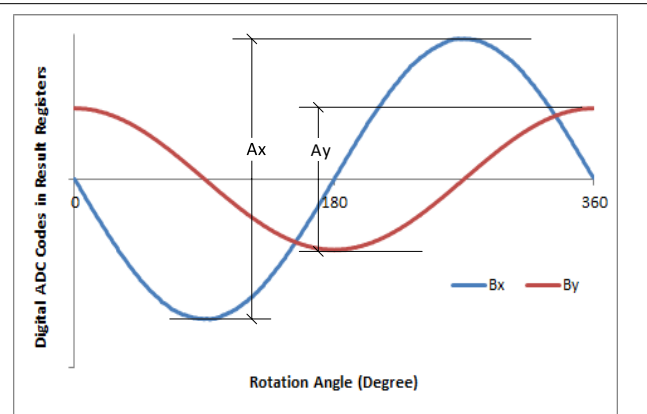
**Example 2:** If  $A_x = 60,000$ ,  $A_y = 45,000$ , the  $G_x = 45,000/60,000 = 0.75$ . Select 01b for the GAIN\_SELECTION register bits.

**Example 3:** If  $A_x = 45,000$ ,  $A_y = 60,000$ , the  $G_x = (60,000/45,000) = 1.33$ . Since  $G_x > 1$ , the gain adjustment needs to be applied to Y axis with  $G_y = 1/G_x$ . Select 10b for the GAIN\_SELECTION register bits.

### 9.2.3 Application Curves



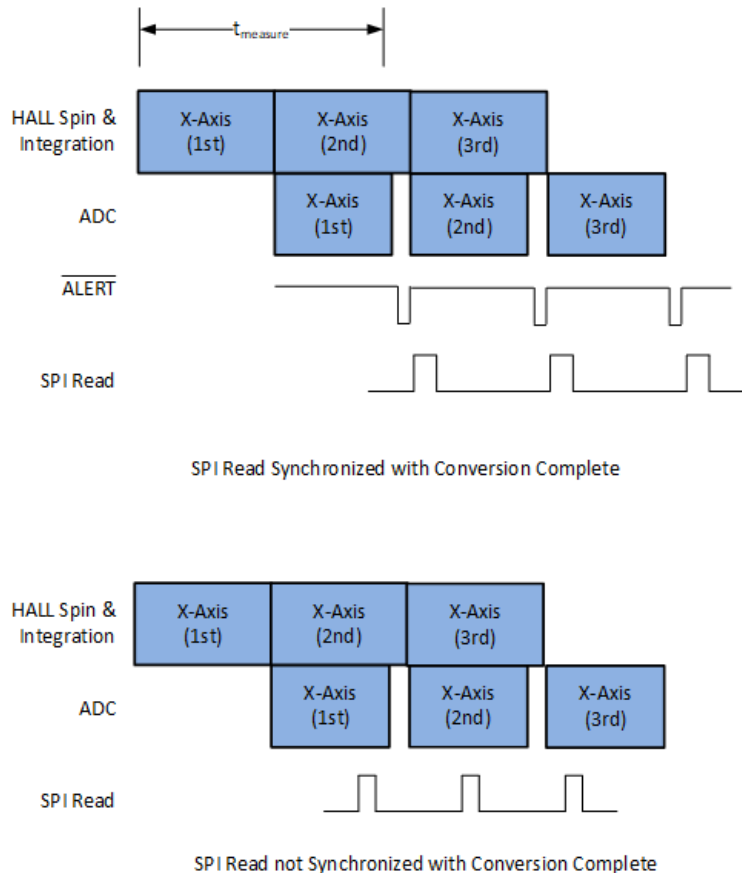
**Figure 9-6. X and Y Sensor Data for Full 360 Degree Rotation for On-Axis Measurement**



**Figure 9-7. X and Y Sensor Data for Full 360 Degree Rotation for Off-Axis Measurement**

### 9.3 Best Design Practices

The TMAG5170D-Q1 updates the result registers at the end of a conversion. SPI read of the result register must be synchronized with the conversion update time to ensure reading the updated result data. The conversion update time,  $t_{\text{measure}}$  is defined in the *Electrical Characteristics* table. Figure 9-8 shows examples of correct and incorrect SPI read timings for applications with strict timing budgets. Use the ALERT signal to notify the controller when a conversion is complete.



**Figure 9-8. SPI Read During Continuous Conversion**

## 9.4 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01  $\mu\text{F}$  between each VCC and GND pins. Connect the TEST pins to the respective ground planes.

## 9.5 Layout

### 9.5.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall-effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

### 9.5.2 Layout Example

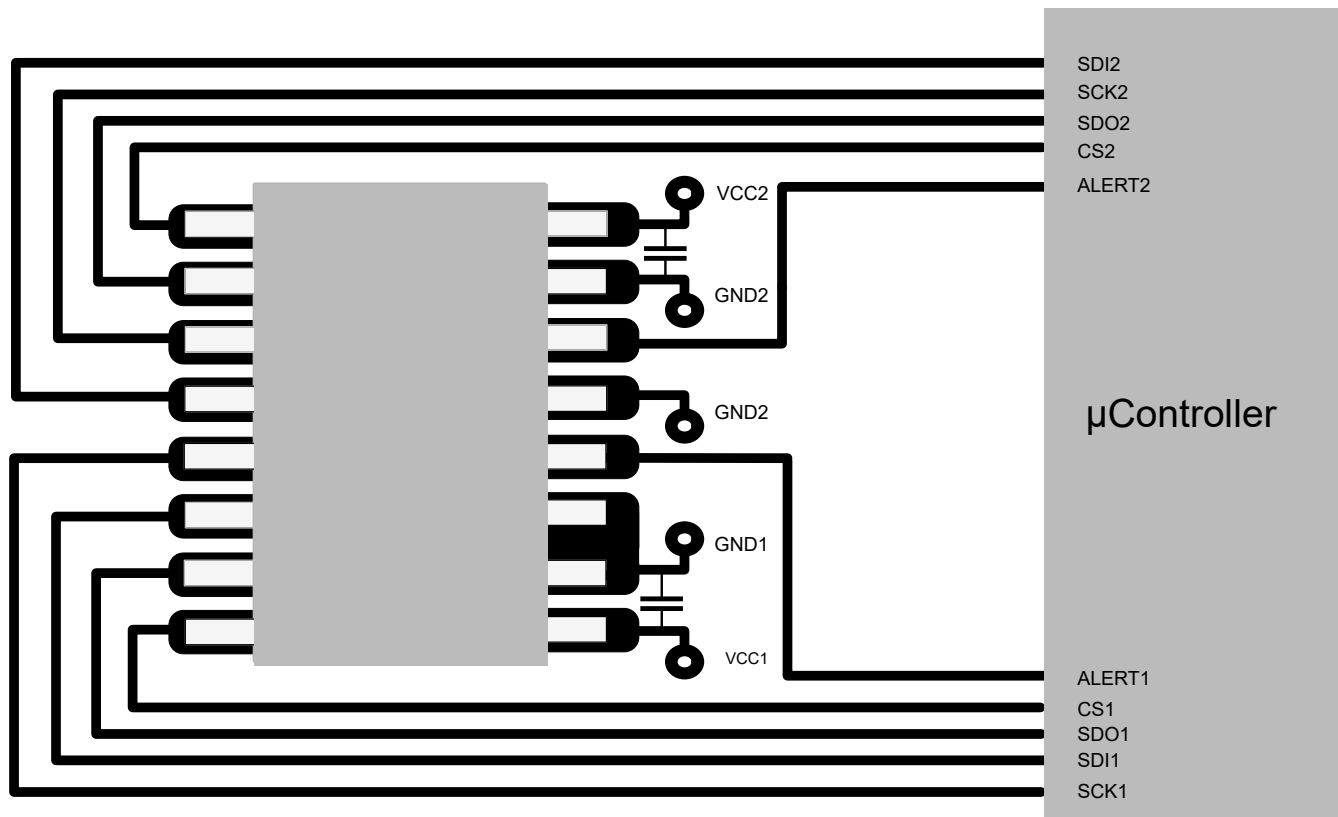


Figure 9-9. Layout Example With TMAG5170D-Q1

## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

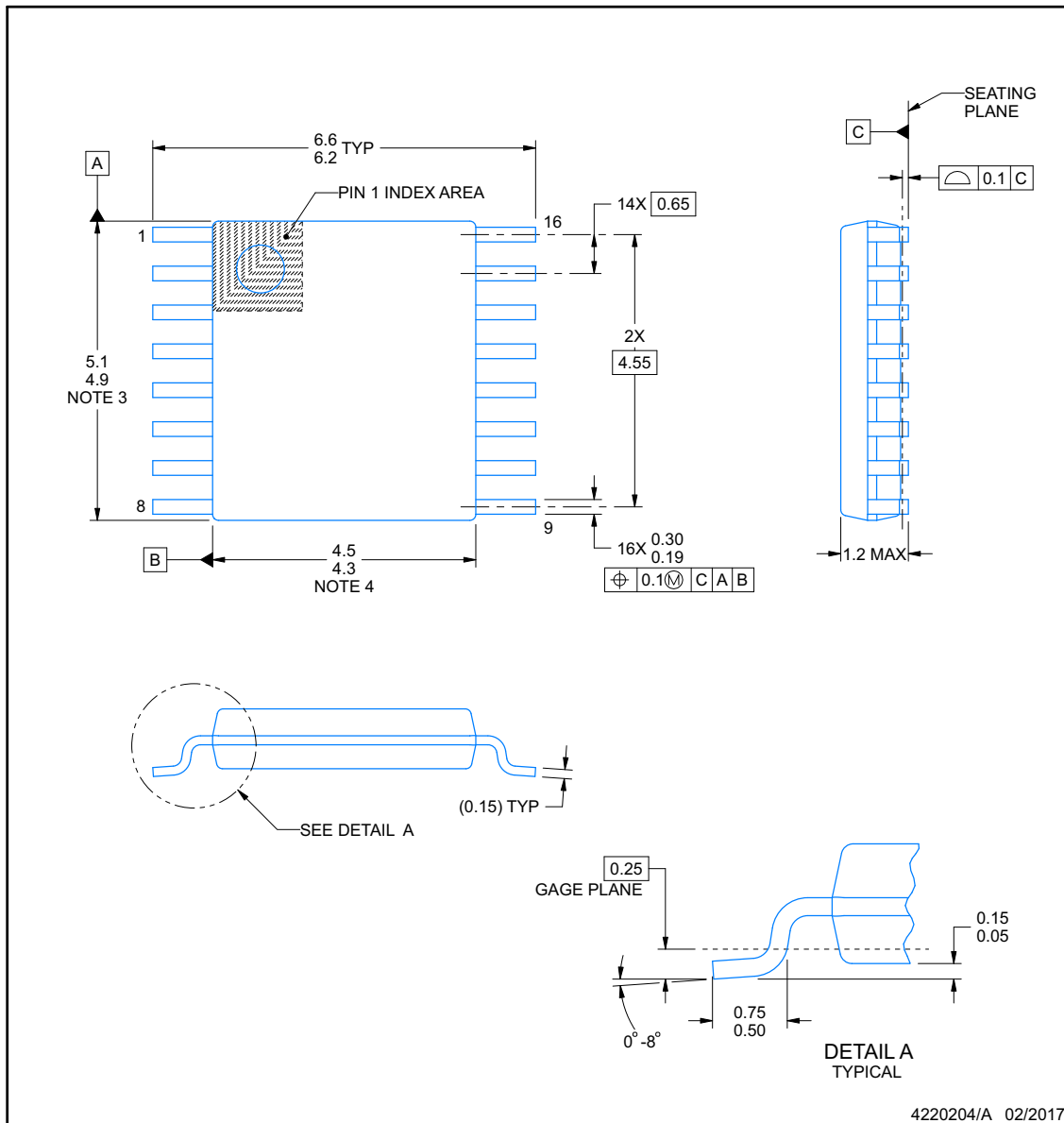
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PW0016A**

**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

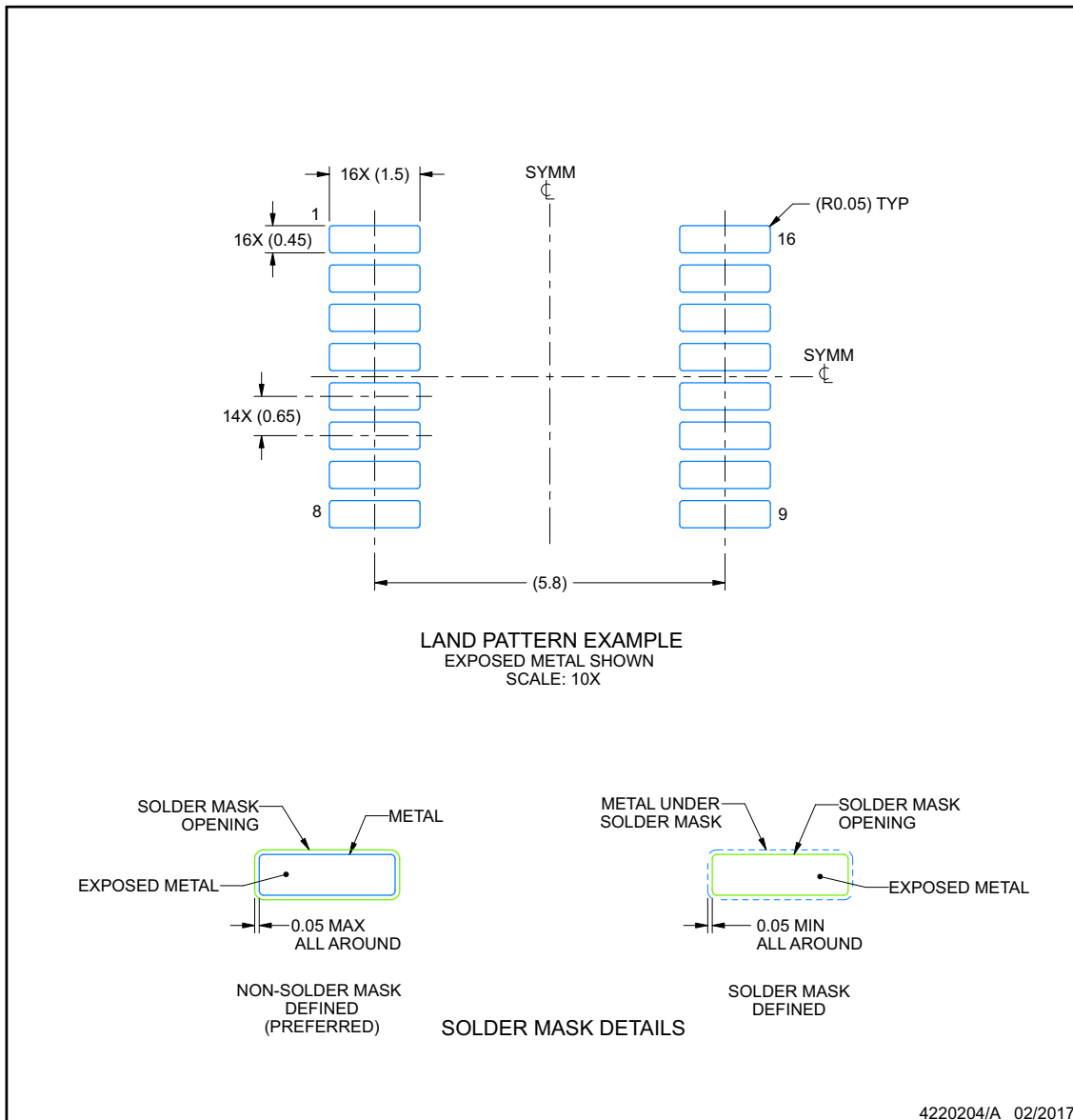
## EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

ADVANCE INFORMATION



NOTES: (continued)

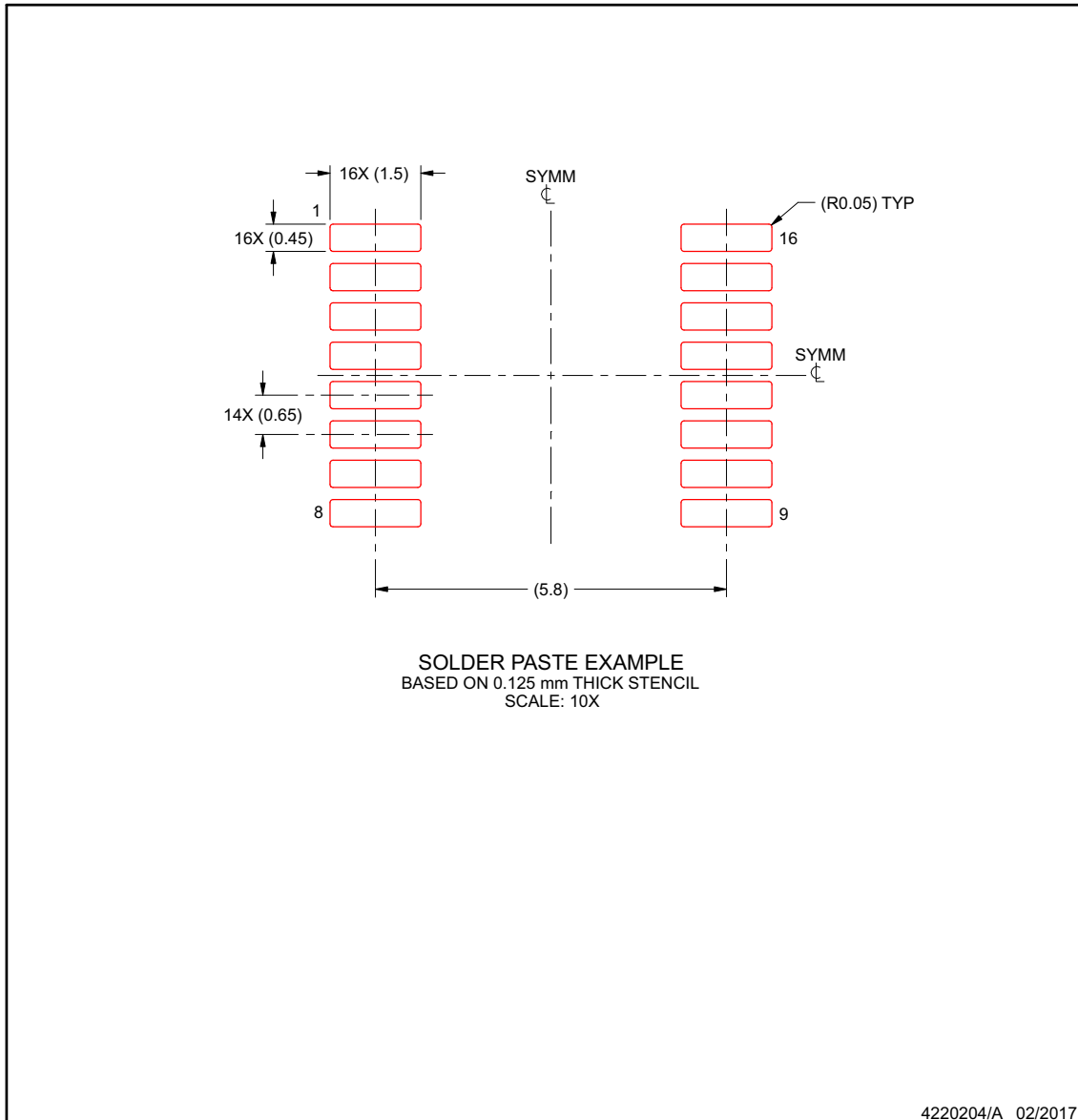
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**PW0016A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

**ADVANCE INFORMATION**

## 11.1 Package Option Addendum

### Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(6)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
PTMAG5170D A2EPWRQ1	ACTIVE	TSSOP	PW	16	2500	Call TI	Call TI	Call TI	-40 to 150	

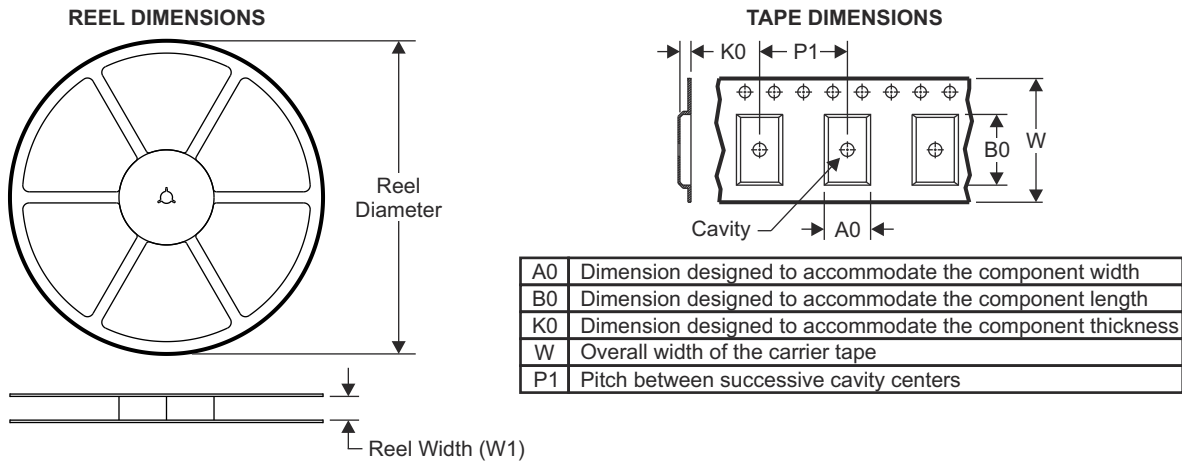
- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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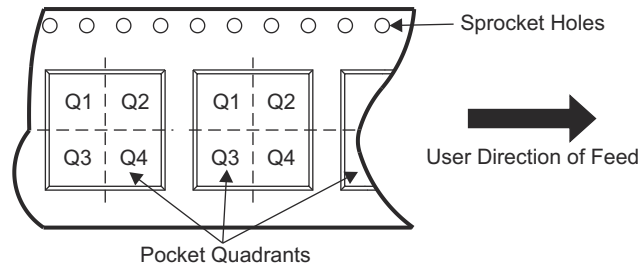
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## 11.2 Tape and Reel Information

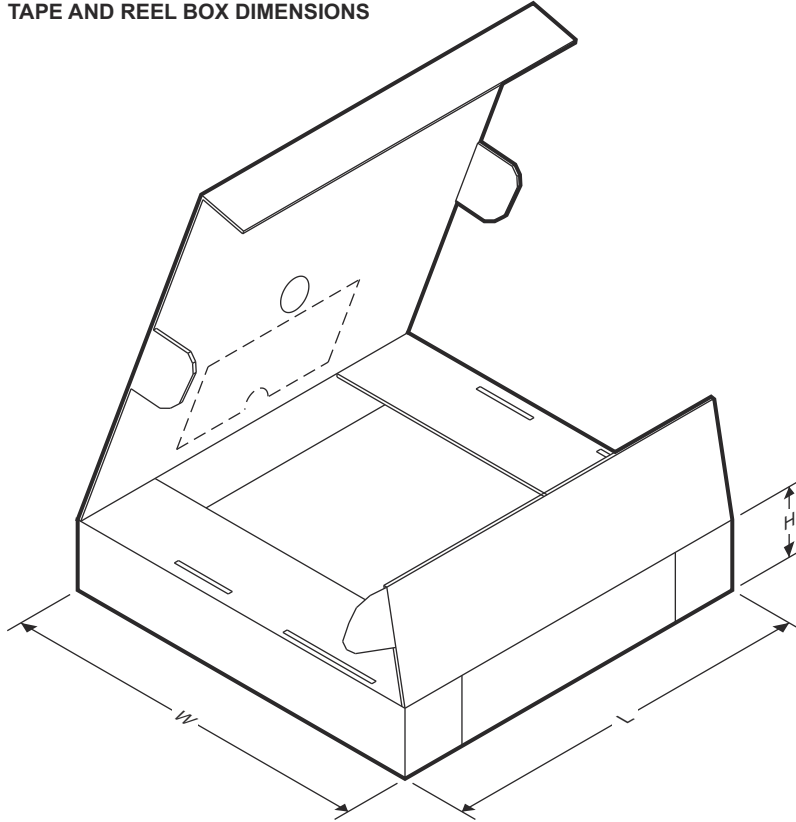


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTMAG5170DA2EPWR Q1	TSSOP	PW	16	2500	330	12.4	6.85	5.45	1.6	1.3	12	Q1

**TAPE AND REEL BOX DIMENSIONS**



**ADVANCE INFORMATION**

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTMAG5170DA2EPWRQ1	TSSOP	PW	16	2500	340	340	38

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMAG5170DA2EPWRQ1	ACTIVE	TSSOP	PW	16	2500	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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