TMP1827 Single-Wire, ±0.3°C Accurate Temperature Sensor With SHA-256-HMAC Authentication Engine, 2-kbit EEPROM

1 Features

- Single-wire interface with multi-drop shared bus and CRC
- Bus powered with operating voltage from 1.7 V to 5.5 V
- IEC 61000-4-2 ESD for 8-kV contact discharge
- High-accuracy digital temperature sensor:
  - ±0.1°C (typical)/±0.3°C (maximum) from –20°C to +85°C
  - ±0.3°C (typical)/±0.5°C (maximum) from –55°C to +125°C
  - ±0.5°C (typical)/±1.0°C (maximum) from –55°C to +150°C
- Active current of 100-µA (typical) and shutdown current of 1.0 µA (typical)
- 16-bit temperature resolution: 7.8125 m°C (1 LSB)
- Fast data rates of 90 kbps in overdrive speed
- Flexible user programmable short address modes for faster device address
- SHA-256-HMAC authentication scheme
  - FIPS 180-4 compliant Secure Hash Implementation
  - FIPS 198-1 compliant HMAC Implementation
- 2-kbit EEPROM features:
  - Write operation in block size of 64-bits
  - Continuous read mode
  - Read with write protection with page size of 256-bits
  - Authenticated write protection mode with page size of 256-bits
  - Read/write current of 95 µA/178 µA (typical)
- NIST traceable factory-programmed non erasable 64-bit identification number for device addressing
- 4 configurable open-drain digital input-output and temperature alert

2 Applications

- Factory automation and control
- Appliances
- Medical accessories
- CPAP machine
- Battery packs
- Cold chain applications
- Temperature transmitters
- EV charging infrastructure

3 Description

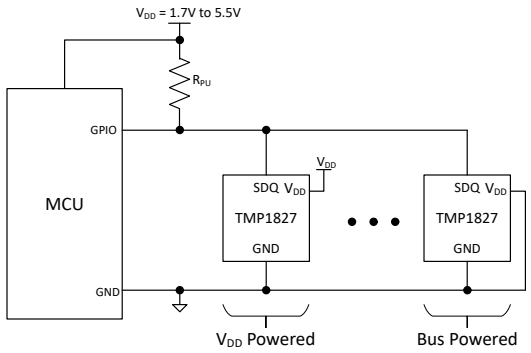
The TMP1827 is a high-accuracy, single-wire compatible digital output temperature sensor with integrated 2-kbit EEPROM and SHA-256-HMAC authentication scheme with a wide operating temperature range from –55°C to +150°C. The TMP1827 provides a high accuracy of ±0.1°C (typical)/±0.3°C (maximum) across the temperature range of –20°C to +85°C. Each device comes with a factory programmed 64-bit unique identification number for addressing and NIST traceability. The TMP1827 supports both standard speed for legacy application and overdrive mode with 90-kbps data rate for low latency communication across a wide voltage range of 1.7 V to 5.5 V.

In the simplest mode of operation, the TMP1827 single-wire interface, with an integrated 8-kV IEC-61000-4-2 ESD protection on the data pin, requires only a single connection and a ground return in bus powered mode, which simplifies and reduces cost by reducing the number of wires and external protection components. Additionally, there is the V_{DD} power pin also available for applications that may want to have a dedicated power supply.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMP1827	WSON (8)	2.50 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2022	*	Initial Release

5 Description (cont.)

The TMP1827 implements the SHA-256-HMAC authentication engine along with key storage, for system authentication requirements of an end equipment. The 2 kbit EEPROM on the device allows the host application to store application specific content in block sizes of 64-bit. The memory can be write protected in page size of 256-bits to avoid accidental data overwrite. The memory architecture enables application to optimize the bus bandwidth when updating variables which are only few bytes while providing an optimal memory size for write protection. The device also features mechanism for host authentication by means of authenticated memory write operations.

ADVANCE INFORMATION

6 Pin Configuration and Functions

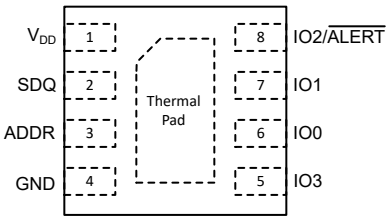


Figure 6-1. NGR 8-Pin WSON Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	WSON		
ADDR	3	I	Resistor address select. If unused, TI recommends to connect pin to ground
GND	4	—	Ground
IO0	6	I/O	General-purpose digital IO. If unused, TI recommends to connect pin to ground
IO1	7	I/O	General-purpose digital IO. If unused, TI recommends to connect pin to ground
IO2/$\overline{\text{ALERT}}$	8	I/O	General-purpose digital IO or configurable as temperature alert. If unused, TI recommends to connect pin to ground
IO3	5	I/O	General-purpose digital IO. If unused, TI recommends to connect pin to ground
SDQ	2	I/O	Serial bidirectional data. In bus power mode, the pin is used to power the internal capacitor
V_{DD}	1	I	Supply voltage in V_{DD} powered mode. In bus powered mode, must be connected to ground

7 Specifications

7.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}		6.5	V
I/O voltage	SDQ, Bus powered mode	–0.3	6.5	V
	SDQ, Supply powered mode	–0.3	V_{DD} + 0.3	
I/O voltage	IO0, IO1, IO2, IO3	–0.3	6.5	V
I/O voltage	ADDR	–0.3	1.65	V
Operating junction temperature, T_J		–55	155	°C
Storage temperature, T_{stg}		–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±500	V
		IEC 61000-4-2 Contact Discharge	SDQ pin	±8000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage V_{DD} powered mode	1.70		5.5	V
V_{PUR}	Supply voltage on SDQ in bus powered mode (V_{DD} = GND)	1.70		5.5	V
$V_{I/O}$	All IO pins in V_{DD} powered mode (except SDQ and ADDR(1))	0		5.5	V
	SDQ pin in V_{DD} powered mode	0		V_{DD} + 0.3	V
T_A	Operating ambient temperature(2)	-55		150	°C

(1) If ADDR pin is not used, it is recommended to be connected to GND
(2) In bus powered mode, overdrive speed supports the max operating temperature up to 150°C, while standard speed supports up to 125°C for full V_{PUR} range and 150C for V_{PUR} > 2.5V (See Figure 7-17)

7.4 Thermal Information

THERMAL METRIC(1)		TMP1827 NGR (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.1	°C/W
M_T	Thermal Mass	TBD	mJ/°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR}	Temperature accuracy	–20 °C to 85°C			±0.1	±0.3	°C
		–55 °C to 125°C			±0.3	±0.5	
		–55 °C to 150°C			±0.5	±1.0	
PSR	DC power supply sensitivity					±0.03	°C/V
T_{RES}	Temperature resolution	Including sign bit			16		Bits
		LSB			7.8125		m°C
T_{REPEAT}	Repeatability(1)	V_{DD} = 3.3 V Averaging enabled, Conversion Time = 5.5 ms, 16-bit mode, 1-Hz conversion interval, 300 acquisition			±2		LSB
T_{LTD}	Long-term stability and drift	1000 hours at 150°C(2)			0.0625		°C
T_{HYST}	Temperature cycling and hysteresis	T_{START} = –40°C T_{FINISH} = 150°C T_{TEST} = 25°C 3 cycles			4		LSB
t_{RESP_L}	Response time (Stirred Liquid)	Single layer Flex PCB	τ = 63 % 25°C to 75°C		0.77		s
		2-layer 62-mil Rigid PCB			1.91		s
t_{ACT}	Active Conversion time (No Averaging)	CONV_TIME_SEL = 0	(Figure 8-12)	TBD	3	TBD	ms
		CONV_TIME_SEL = 1		TBD	5.5	TBD	ms

ADVANCE INFORMATION

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DELAY}	Start-up delay for temperature conversion and EEPROM programming			100		300	µs
SDQ DIGITAL INPUT/OUTPUT							
C_{IN}	SDQ pin capacitance				40		pF
V_{IL}	Input logic low level(3)			–0.3		0.2 × V_S	V
V_{IH}	Input logic high level(3)			0.8 × V_S		V_S + 0.3	V
V_{HYST}	Hysteresis				0.3		V
I_{IN}	Input leakage current				±0.5	TBD	µA
V_{OL}	Output low level	I_{OL} = –4 mA				0.4	V
GPIO CHARACTERISTICS							
C_{IN}	Input capacitance				10		pF
V_{IL}	Input logic low level(3)			–0.3		0.2 × V_S	V
V_{IH}	Input logic high level(3)			0.8 × V_S		V_S + 0.3	V
I_{IN}	Input leakage current				0	±0.1	µA
V_{HYST}	Hysteresis				0.175		V
V_{OL}	Output low level	I_{OL} = –4 mA				0.4	V
RESISTOR ADDRESS DECODER CHARACTERISTICS							
C_{LOAD}	Load capacitance as seen on ADDR pin (includes PCB parasitics)					100	pF
	R_{ADDR} resistor range			6.49		54.9	kΩ
	R_{ADDR} resistor tolerance	T_A = 25°C		–1.0		1.0	%
	R_{ADDR} resistor temperature coefficient			–100		100	ppm/°C
	R_{ADDR} resistor lifetime drift			–0.2		0.2	%
t_{RESDET}	Resistor decoding time				2.8		ms
POWER SUPPLY							
I_{PU}	Pullup current(4)	Bus powered mode, serial bus inactive		300			µA
I_{DD_ACTIVE}	Supply current during temperature conversion	Temperature Conversion, serial bus inactive			97	TBD	µA
I_{DD_SB}	Standby current(5)	V_{DD} powered, serial bus inactive, continous conversion mode	T_A = -55°C to 85°C		1.59	TBD	µA
			T_A = -55°C to 150°C			TBD	
I_{DD_SD}	Shutdown current	Serial bus inactive, one shot conversion mode	T_A = -55°C to 85°C		1.01	TBD	µA
			T_A = -55°C to 150°C			TBD	
V_{POR}	Power-on reset threshold voltage	Supply rising (Figure 7-4, Figure 7-5)		1.5			V
	Brownout detect	Supply falling				1.3	V
t_{INIT}	Reset Initialization Time	Time required by device to reset after power up (Figure 7-4, Figure 7-5)				2.0	ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions. See Figure 7-11
(2) Long term stability is determined using accelerated operational life testing at a junction temperature of 150°C.
(3) In bus powered mode V_S = V_{PUR}. In supply powered mode V_S = V_{DD}.
(4) The pullup current parameter is required to size the bus pullup resistor (See Section 8.3.3) for active temperature conversion or EEPROM read and program or authentication operations.
(5) Quiescent current between conversions.

ADVANCE INFORMATION

7.6 1-Wire Interface Timing

Over free-air temperature range and V_{DD} = 1.70 V to 5.5 V (unless otherwise noted)

		STANDARD MODE		OVERDRIVE MODE		UNIT
		MIN	MAX	MIN	MAX	
BUS RESET AND BIT SLOT TIMING						
t_{RSTL}	Host to device bus reset pulse width (Figure 7-1) (1)	480	560	48	80	µs
t_{RSTH}	Device to host response time (Figure 7-1)(2)	480		48		µs
t_{PDH}	Device turnaround time for bus reset response (Figure 7-1)	15	60	2	8	µs
t_{PDL}	Device to host response pulse width (Figure 7-1)	60	240	8	24	µs
t_{SLOT}	Bit slot time (Figure 7-2, Figure 7-3)	60	120	11		µs
t_{REC}	Recovery time (Figure 7-2, Figure 7-3)	2		2		µs
t_{GF}	Glitch filter width (Figure 7-6)(3)	0.48		0.025		µs
t_F	Fall time		100		100	ns
BIT WRITE TIMING						
t_{WR0L}	Host write 0 width (Figure 7-2)	60	120	9	10	µs
t_{WR1L}	Host write 1 width (Figure 7-2)	2	15	1	2	µs
t_{RDV}	Device read data valid time (Figure 7-2)	15		2		µs
t_{DSW}	Device read data window (Figure 7-2)	15	45	2	7	µs
BIT READ TIMING						
t_{RL}	Host drive read bit slot time (Figure 7-3)	2	5	2	3	µs
t_{RWAIT}	Host wait time before read data sampling window (Figure 7-3)(4)		$t_{RL}+t_{RC}$		$t_{RL}+t_{RC}$	µs
t_{MSW}	Host read data sampling window (Figure 7-3)	$t_{RL}+t_{RC}$	30	$t_{RL}+t_{RC}$	3	µs

(1) In bus powered mode, extending the t_{RSTL} above 600 µs may cause the device to power on reset
(2) The t_{RSTH} is the maximum time the host must wait to receive a response from the furthest device, taking into account the propagation delay and recovery time for all the devices.
(3) The glitch filter timing applies only on the rising edge of the SDQ signal
(4) The t_{RC} time is defined as the time taken for the bus voltage to rise from 0V to minimum V_{IH} of the host. This is a function of the bus pullup resistor and parasitic capcitance of the trace or cable.

7.7 Security Engine Characteristics

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{HASH_DATA}	Computation time for SHA-256 hash calculation for data size of 8 bytes			355	µs
$t_{DECOMMISSION}$	Time for decommission of the device		78	130	ms
I_{DD_HASH}	Hash computation current			TBD	µA

7.8 EEPROM Characteristics

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{PROG}	Programming time for 8-byte data word in user EEPROM		13.2	21	ms
	Programming time for register copy to EEPROM		26.4	42	ms
$t_{READIDLE}$	Idle bus time for EEPROM 8-byte data word fetch			400	µs
I_{DD_PROG}	Programming current		178	TBD	µA
Data Retention	at T_A = 125°C	25			years
	at T_A = 150°C	10			years
Endurance	For erase and program cycles	1000	20000		cycles

ADVANCE INFORMATION

7.9 Timing Diagrams

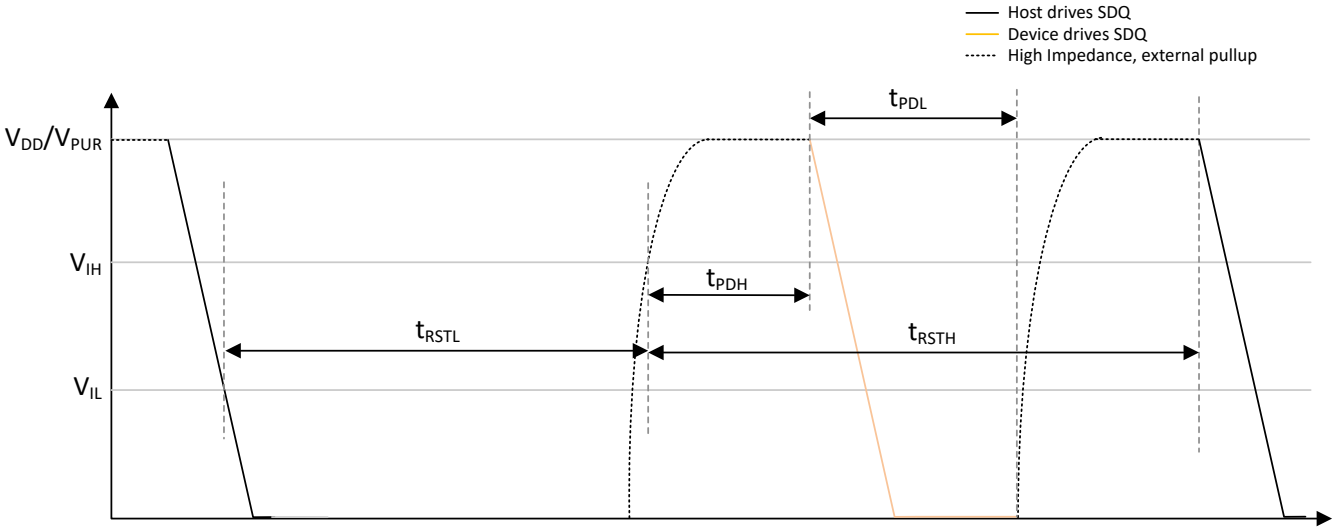


Figure 7-1. Bus Reset Timing Diagram

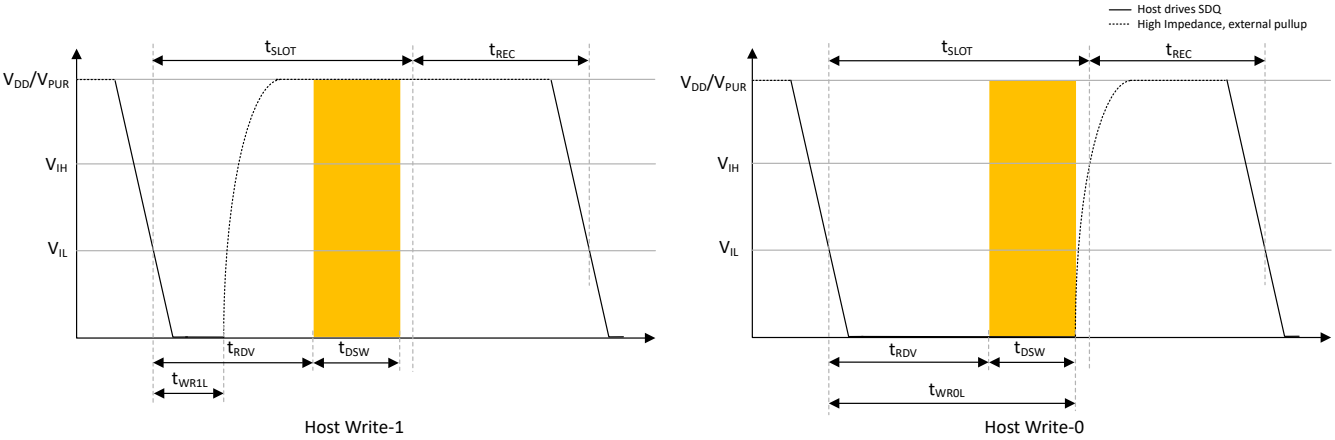


Figure 7-2. Write Timing Diagram

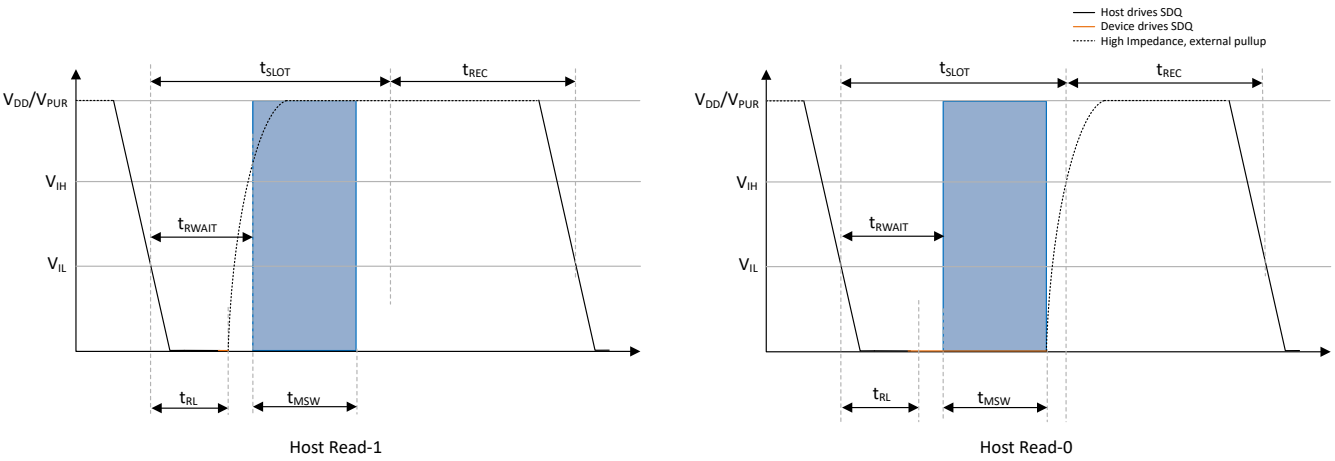


Figure 7-3. Read Timing Diagram

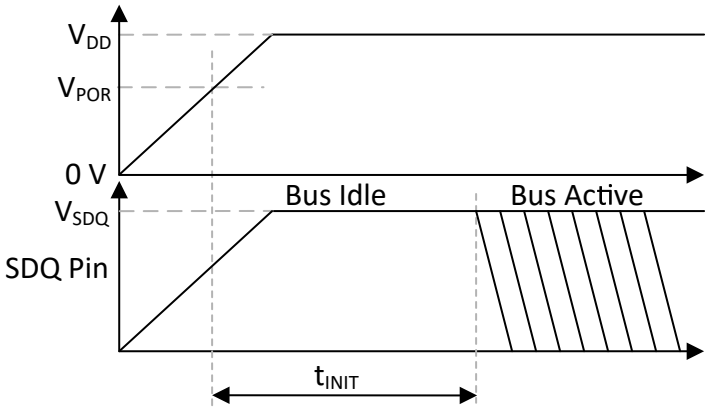


Figure 7-4. V_{DD} Powered Initialization Timing Diagram

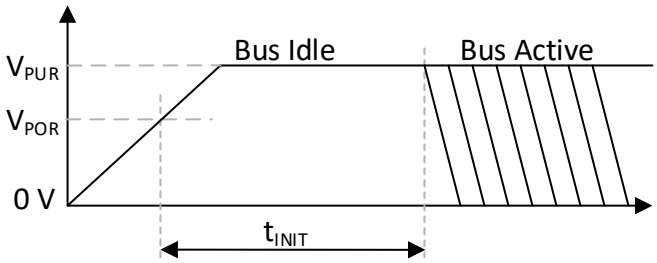


Figure 7-5. Bus Powered Initialization Timing Diagram

ADVANCE INFORMATION

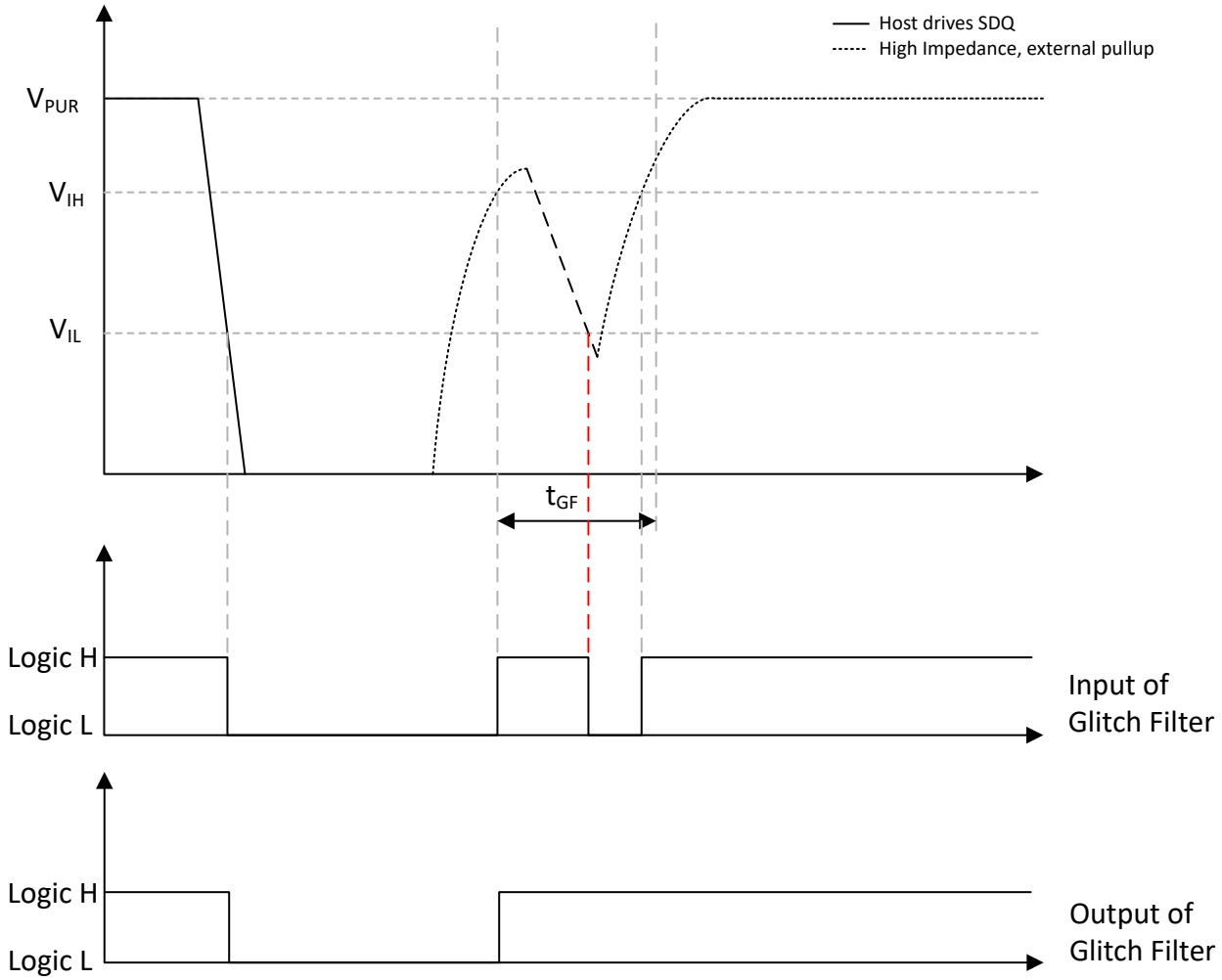


Figure 7-6. Glitch Filter Timing Diagram

7.10 Typical Characteristics

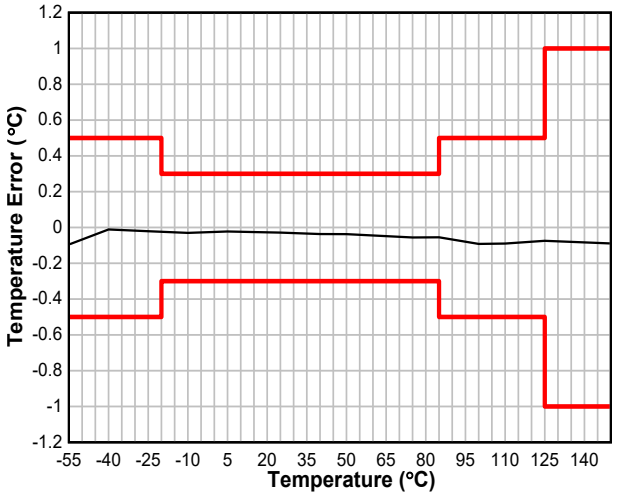


Figure 7-7. Temperature Error vs Temperature (NGR Package)

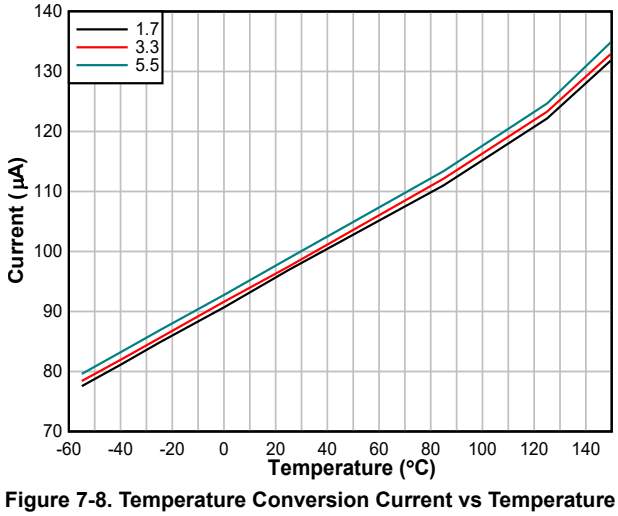


Figure 7-8. Temperature Conversion Current vs Temperature

7.10 Typical Characteristics (continued)

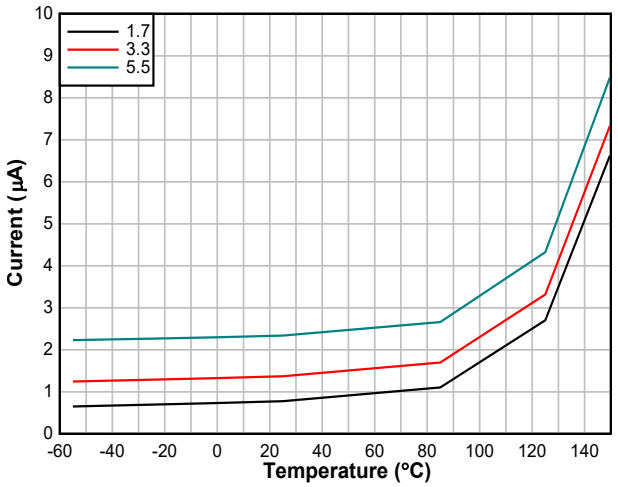


Figure 7-9. Shutdown Current vs Temperature

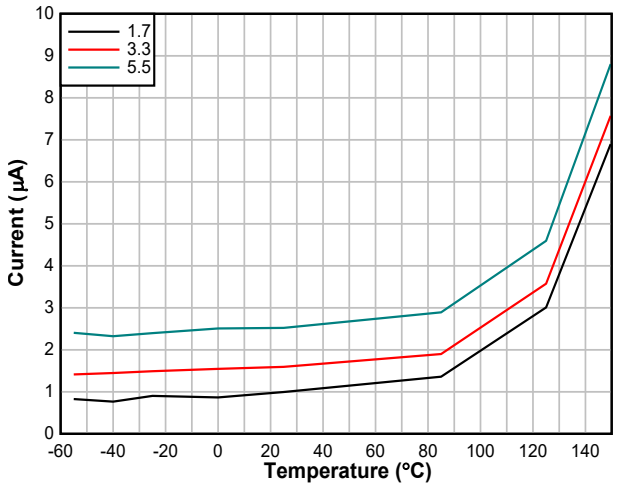
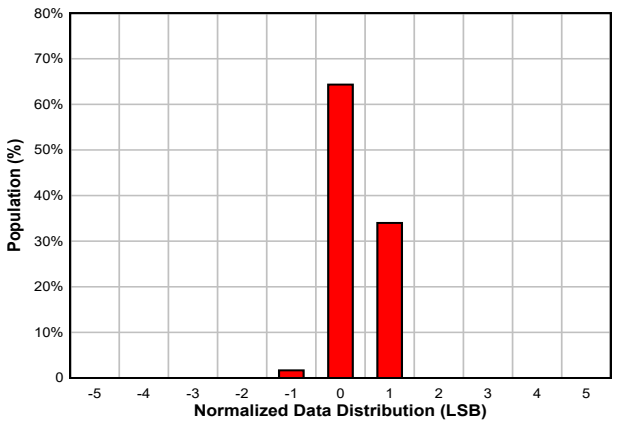
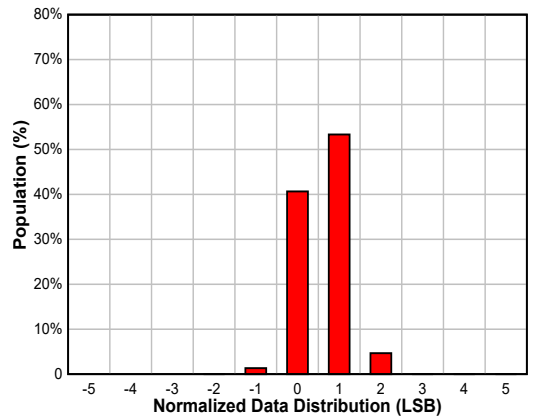


Figure 7-10. Standby Current vs Temperature



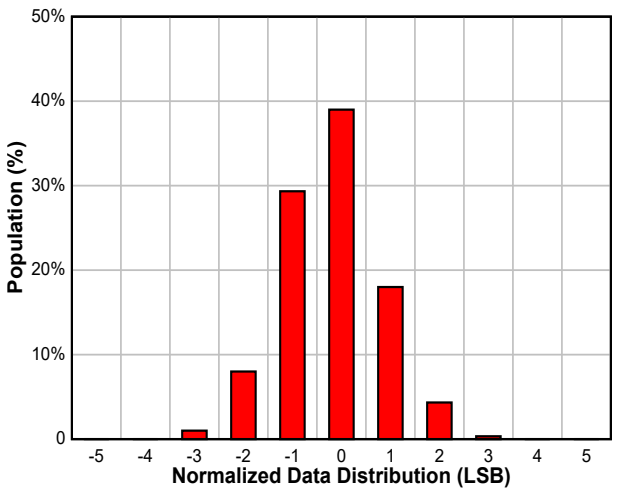
T_A = 25°C

Figure 7-11. Data Distribution With 5.5-ms Conversion Time and Averaging On



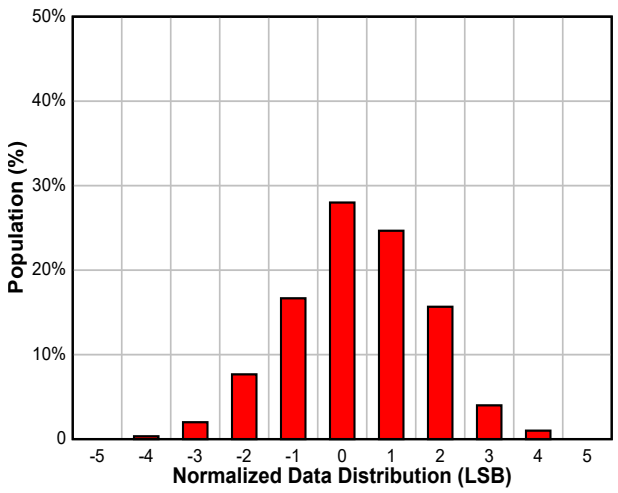
T_A = 25°C

Figure 7-12. Data Distribution With 3-ms Conversion Time and Averaging On



T_A = 25°C

Figure 7-13. Data Distribution With 5.5-ms Conversion Time and Averaging Off

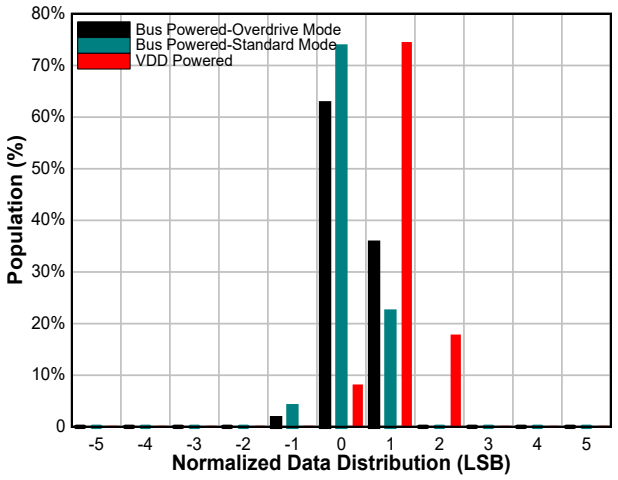


T_A = 25°C

Figure 7-14. Data Distribution With 3-ms Conversion Time and Averaging Off

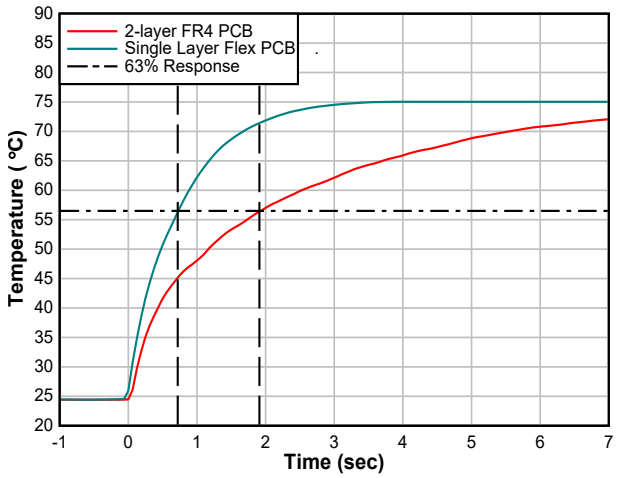
ADVANCE INFORMATION

7.10 Typical Characteristics (continued)



T_A = 25°C, 5.5 ms Conversion Time, Averaging On

Figure 7-15. Data Distribution for Power Mode and Bus Speed



T_{START} = 25°C, T_{FINISH} = 75°C

Figure 7-16. Thermal Response Time (NGR)

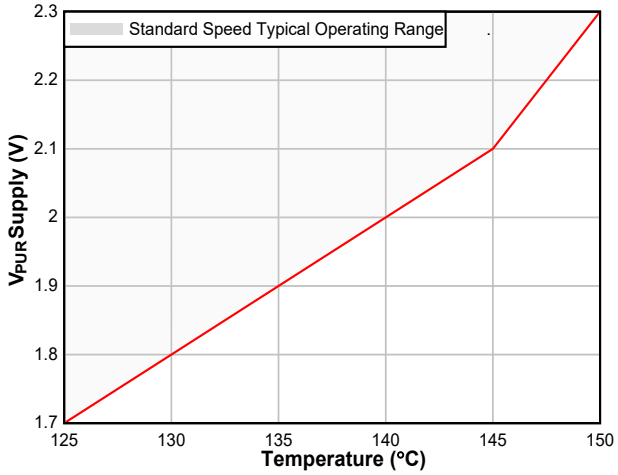


Figure 7-17. V_{PUR} Minimum Supply Voltage vs Temperature (Standard Speed)

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TMP1827 is a digital output temperature sensor designed for thermal-management and thermal-protection applications. The TMP1827 is a single-wire device which can operate in either supply powered or bus powered (parasitic powered) mode. The device features a 2-kbit EEPROM, SHA-256-HMAC based authentication engine. Figure 8-1 shows a block diagram of the TMP1827.

8.2 Functional Block Diagram

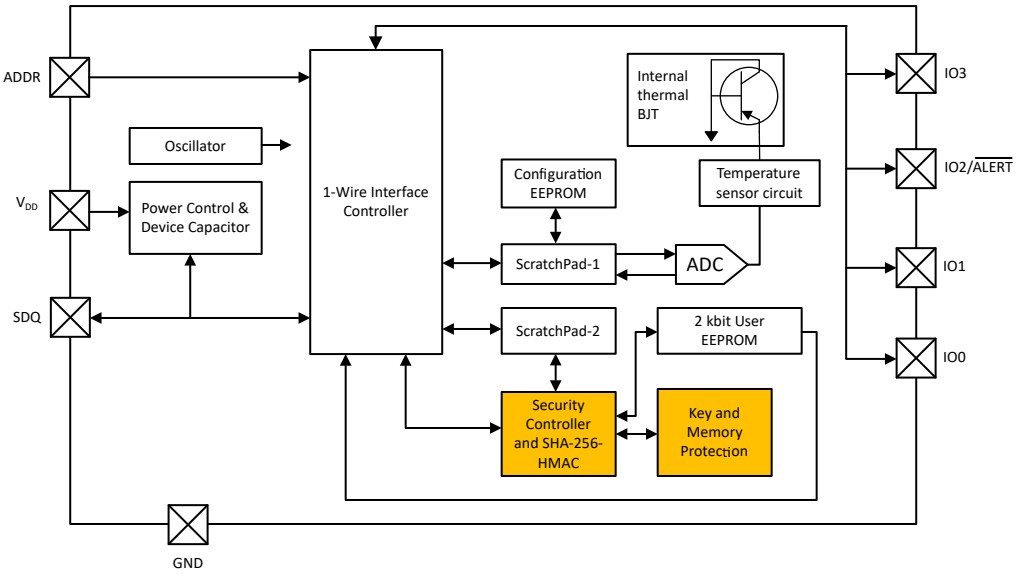


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Power Up

The device operates in both supply powered and bus powered mode. Irrespective of the mode, when the supply voltage reaches within the operating range, the device requires t_{INIT} to initialize itself. After t_{INIT}, the host MCU can begin accessing the device.

During initialization, the device may not respond to any bus activity. When initialization is complete, the device shall wait for the bus reset from the host. During the initialization for the device, the following events take place:

- The EEPROM content for short address, temperature alert low, temperature alert high and temperature offset registers are restored.
- The EEPROM for the IO configuration register is read and contents of the IO configuration register is restored.
- The EEPROM content for device configuration-1 and device configuration-2 registers are restored to the respective registers.
  - If the ARB_MODE bits are set to value other than '00b', then the device will respond to the SEARCHADDR in arbitration mode.
  - If OD_EN bit is set to '1b', then the device shall communicate in overdrive speed, unless the first bus reset pulse from the host is sent in standard speed.
- The user memory protection bits are restored and appropriate protection to the user EEPROM block applied.
- The authentication key and secret bytes are read from the EEPROM to internal flops for the authentication operation.

8.3.2 Power Mode Switch

The device is designed to operate in supply powered or bus powered mode. The dual mode implementation provides a unique method of redundancy that, even in cases where the power supply pin gets disconnected, the

ADVANCE INFORMATION

device can draw power from data pin, as long as the pullup resistor value used is as per the specification limit. This may be the system case where while operating in supply powered mode, the supply pin may accidentally get disconnected, especially under harsh operating conditions.

When the device switches from supply powered to bus powered mode, the device shall operate with the same settings until the internal capacitor is able to provide the current draw required by the device for communication and the external pullup resistor can charge the internal capacitor during bus idle time. If the internal voltage on the capacitor drops below the brown-out threshold, the device shall switch itself off and enter bus powered mode of communication on subsequent power up. The device may not complete the ongoing communication during this time. When the device completes the power-up initialization sequence, as described earlier, the device shall respond to first bus communication starting with the bus reset sequence.

8.3.3 Bus Pullup Resistor

The bus pullup resistance value selected is important for communication as per the speed mode and ensuring that minimal possible energy is consumed in the application. If the resistor value is too small, it may violate the V_{OL} limits on the SDQ pin.

The total SDQ pin and bus capacitance must be considered along with the bus leakage current when selecting the pullup resistor. The pullup resistance value selected must also ensure that the signal level reaches V_{IH} as per the timing requirements for standard and overdrive mode.

In bus powered mode of operation, the device charges its internal capacitor through the SDQ pin and the pullup resistor. This charge on the capacitor is used during bus communication, when the SDQ pin low. For other high current functions like thermal conversion and EEPROM access, the bus is held idle to ensure that the device can draw current through the pullup resistor. The SDQ pin voltage during the high current operation must be maintained to ensure sufficient operating margins. Use Equation 1 to calculate the pullup resistor value.

$$\frac{\left(V_{PUR} - V_{OL(MAX)}\right)}{4 \times 10^{-3}} < R_{PUR} < \frac{(V_{PUR} - 1.6)}{I_{PU(MIN)}} \quad (1)$$

When the device is used in V_{DD} or supply powered mode, a larger pullup resistor value may be used, as the SDQ pin is used only for communication. The user must ensure that the pullup resistor value selected must be able to support the timing for the required bus speed of operation.

For low current consumption devices like TMP1827, selecting the correct pullup resistor value allows the application to avoid low impedance current path components for bus powered mode of operation while maintaining communication speeds and device parameters as per its electrical specification.

8.3.4 Temperature Results

The conversion is initiated by the host MCU by sending the temperature conversion command if the automatic conversion is disabled, or immediately after the presence detect is completed when the automatic conversion is enabled, or in continuous conversion mode if the device is V_{DD} powered. At the end of every conversion, the device updates the temperature registers temperature result and the status register bits. Figure 8-2 shows that the device supports a high precision and legacy format, which can be configured through the TEMP_FMT bit in the device configuration-1 register.

Temperature Result MSB Register								Temperature Result LSB Register							

High Precision Format

S	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}

Legacy Format

S	S	S	S	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}

Figure 8-2. Temperature Format

If the format selected is the high precision 16-bit format, the data in the result registers is stored in two's complement form and has a resolution of 0.0078125°C. If the format selected is the legacy 12-bit format, the

data in the result register is stored in sign extended form and has a resolution of 0.0625°C. The temperature register reads as 0°C before the first conversion. Table 8-1 and Table 8-2 show examples of possible binary data that can be read from the temperature result registers and the corresponding hexadecimal and temperature equivalents for both formats.

Table 8-1. Precision (16-Bit) Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (PRECISION FORMAT)	
	BINARY	HEXADECIMAL
150	0100 1011 0000 0000	4B00
127	0011 1111 1000 0000	3F80
100	0011 0010 0000 0000	3200
25	0000 1100 1000 0000	0C80
1	0000 0000 1000 0000	0080
0.125	0000 0000 0001 0000	0010
0.03125	0000 0000 0000 0100	0004
0.0078125	0000 0000 0000 0001	0001
0	0000 0000 0000 0000	0000
–0.0078125	1111 1111 1111 1111	FFFF
–0.03125	1111 1111 1111 1100	FFFC
–0.125	1111 1111 1111 0000	FFF0
–1	1111 1111 1000 0000	FF80
–25	1111 0011 1000 0000	F380
–40	1110 1100 0000 0000	FC00
–55	1110 0100 1000 0000	F480

Table 8-2. Legacy (12-Bit) Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEXADECIMAL
128	0000 0111 1111 1111	07FF
127.9375	0000 0111 1111 1111	07FF
100	0000 0110 0100 0000	0640
25	0000 0001 1001 0000	0190
1	0000 0000 0001 0000	0010
0.125	0000 0000 0000 0010	0002
0	0000 0000 0000 0000	0000
–0.125	1111 1111 1111 1110	FFFE
–1	1111 1111 1111 0000	FFF0
–25	1111 1110 0111 0000	FE70
–40	1111 1101 1000 0000	FD80
–55	1111 1100 1001 0000	FC90

8.3.5 Temperature Offset

The temperature offset has the same format as the temperature result and is stored in the temperature offset registers.

The device, after every temperature conversion, shall apply the offset value before the temperature is stored in the temperature result register. The host write to the registers can be stored in the configuration EEPROM of the device, thereby reducing the overhead as the host does not need to reprogram the values at every power up. The offset features allow the device to achieve better accuracy at the temperature range for the application by performing a single point calibration.

ADVANCE INFORMATION

8.3.6 Temperature Alert

The temperature alert feature uses the temperature alert low registers for low threshold comparison and temperature alert high registers for high threshold comparison. The format of the register is the same as the temperature results.

The device shall compare the result of the last conversion with the alert thresholds. If the temperature result is less than the low limit, or more than the high limits, then the device shall set the appropriate alert status flag for low or high temperature limits, in the status register. The alert status flags are cleared based on the ALERT_MODE setting in the device configuration-1 register.

Additionally, if the IO2/$\overline{\text{ALERT}}$ pin is configured as an alert pin, the alert status is reflected on the pin.

8.3.7 Standard Device Address

Every device comes with a unique 64-bit address that is factory programmed. Additionally the device provides flexible addressing modes that the host controller may use to improve bus throughput. This is described below.

8.3.7.1 Unique 64-Bit Device Address and ID

The device has a hard-coded, 64-bit address which is factory programmed and cannot be altered by the customer application. The unique 64-bit device address is used for device addressing in the end application and for NIST traceability. Figure 8-3 shows the format of the 64-bit address. When the host accesses the device or when the device sends its address, the 64-bit unique address is sent least significant bit first. The unique 64-bit address consists of 3 fields. The lower 8 bits consists of the device family code, followed by a 48-bit unique number and 8-bit CRC checksum on the 56 bits preceding it.

The device family code for TMP1827 shall read as 27h.

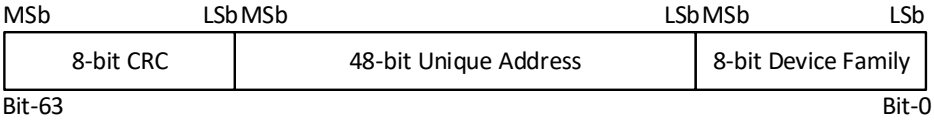


Figure 8-3. 64-Bit Device Address

8.3.8 Flexible Device Address

Depending on the user application case, the TMP1827 provides for some user and application configurable address modes, called flexible address mode. These modes exist along side the standard device address, and is extremely useful for applications that require a combination of faster access and device position identification.

When the flexible device address is used, the short address register is updated. The short address register shall be updated by the host write when the FLEX_ADDR_MODE bits are '00b'. When these bits have a value other than '00b', the resulting decode of the resistor connected on ADDR pin or IOs shall be overlaid on the short address register. This is helpful as the same set of 16 resistors or 16 IO combinations can be used to extend the number of unique flexible address up to 256.

The FLEX_ADDR_MODE is not backed in the configuration EEPROM. Hence after decoding, the host must ensure that copy to configuration EEPROM is performed to make the short address values permanent, without having to decode at every power up.

8.3.8.1 Non-Volatile Short Address

Figure 8-4 shows the user-programmable, 8-bit short address mode of the device. The host must program the 8-bit short address to the underlying non-volatile memory, using a stand-alone programmer, so that at subsequent power up, the device loads the short address and can respond to the host during the address phase of bus communication.

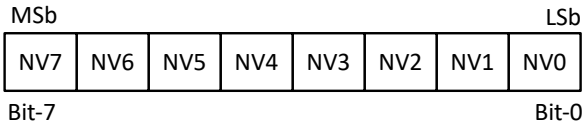


Figure 8-4. Non-Volatile Short Address

8.3.8.2 IO Hardware Address

Figure 8-5 shows the 8-bit IO hardware address mode of the device. This feature is available on packages which have general-purpose pins (IO0-IO3) available. The 8-bit value consists of the lower 4 bits as read values of the pins (IO3 to IO0) that is overlaid on the contents of the short address register to form a 8-bit address. The application may connect the general-purpose pins to either V_{DD}/SDQ for logic '1' or GND for logic '0'.

After power up, the host must set the bits FLEX_ADDR_MODE[1:0] as '01b' in the device configuration-2 register for the device to latch the state of the general-purpose pins.

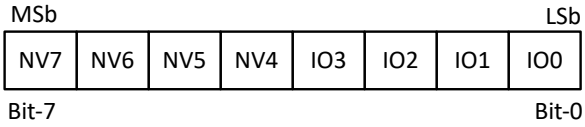


Figure 8-5. IO Hardware Address

Note

If any of the IO0 to IO3 pins are used in output mode, then the respective value shall be latched as '0'.

8.3.8.3 Resistor Address

The resistor address modes uses a 1% tolerance resistor connected between the ADDR pin and ground. Figure 8-6 shows the 8-bit address with the lower 4 bits decoded from the resistor connected, which is overlaid on the contents of the short address register.

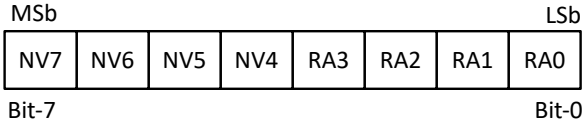


Figure 8-6. Resistor Address

After power up, the host controller sets the bits FLEX_ADDR_MODE[1:0] as '10b' in the device configuration-2 register which enables the device to sample the pin and identify the resistor connected. After writing the device configuration-2 register, the host must idle the bus for t_{RESDET}, for the device to decode the resistor address. Table 8-3 shows the set value of the device address based on the decoded resistor value. If the ADDR pin connected to GND or lower than 6.49 kΩ, then the address decoder shall always decode as '0000b'. Similarly, if the ADDR pin is connected to a resistor higher than 54.9 kΩ, the address decoder shall always decode as '1111b'.

The host controller must ensure that CONV_MODE_SEL[2:0] is set as '000b' when decoding the resistor address.

Table 8-3. Resistor Address Decode

RESISTOR VALUE (kΩ)	ADDRESS DECODE
< 6.49	0h
7.87	1h
9.31	2h
11.0	3h
13.3	4h
15.4	5h

ADVANCE INFORMATION

Table 8-3. Resistor Address Decode (continued)

RESISTOR VALUE (kΩ)	ADDRESS DECODE
17.8	6h
20.5	7h
23.7	8h
26.7	9h
30.1	Ah
33.2	Bh
37.4	Ch
44.2	Dh
47.5	Eh
> 54.9 or floating	Fh

This mode is useful when the application requires placing the TMP1827 on multiple printed circuit boards (PCBs). The Bill of Materials (BOM) component can be changed easily instead of having multiple PCBs fabricated for individual pin connections, thereby reducing the cost of the system.

Note

The ADDR pin if unused, must be connected to GND. The C_{LOAD} for ADDR pin is due to parasitic capacitance depending on the board layout. There is no requirement to place an external capacitor on the ADDR pin.

8.3.8.4 Combined IO and Resistor Address

In the combined IO and resistor address mode, the IO0 and IO1 pin is used along with the resistor connected between ADDR pin and ground. Figure 8-7 shows the 8-bit address with the lower 4 bits decoded from the resistor connected, followed by 2 bits decoded from the IO0 and IO1 pins which may be connected to either VDD/SDQ for logic '1' or GND for logic '0', which is overlaid on the contents of the short address register.

After power up, the host sets the bits FLEX_ADDR_MODE[1:0] as '11b' in the device configuration-2 register which enables the device to sample the ADDR pin to identify the resistor connected, followed by sampling of the IO0 and IO1 to configure the short address. If the bit field value has already been updated in the non-volatile storage, then the device shall automatically latch the pins, run the resistor decoder, and update the value in the short address register on power up.

The host controller must ensure that CONV_MODE_SEL[2:0] is set as '000b' when decoding the resistor address.

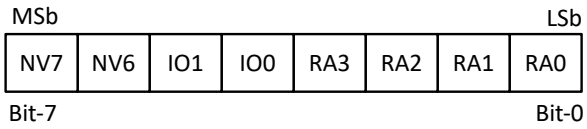


Figure 8-7. Combined IO and Resistor Address

This mode is useful when the application requires placing up to 64 devices on a single PCB, as it allows for easy expansion using a combined approach of IO and resistor decoding while enabling IO2 and IO3 to function as general-purpose input and output pins. This mode may also be used for position identification as no two devices may have the same short address.

Note

If the IO0 or IO1 pins are used in output mode, then the respective value shall be latched as '0'.

ADVANCE INFORMATION

8.3.9 CRC Generation

The TMP1827 implements a cyclic redundancy check (CRC) mechanism for data integrity check and communication robustness. Table 8-4 lists the properties of a 8-bit CRC.

Table 8-4. CRC-8 Rule

CRC-8 Rule	Attributes
CRC width	8 bits
CRC polynomial	$x^8 + x^5 + x^4 + 1$ (0x31)
Initial seed value	00h
Input data reflected	Yes
Output data reflected	Yes
XOR value	00h

When a new transaction is done, the shift register is initialized with the seed value of 00h and the data is shifted in LSB first. The CRC result is always part of the 64-bit unique address and is computed on the 56-bits that precede it. Additionally, when the host writes to the scratchpad-1 for the registers and scratchpad-2 for the memory, the device sends the CRC computed on the data bytes to provide a data integrity check for the host on the transaction. When the host reads the scratchpad-1 for reading the temperature register, the device shall append the CRC after the 8 bytes of scratchpad are sent.

The host must recalculate the CRC and compare it against the received CRC from the device. This is done by shifting the read data from the device along with CRC bits. If there is no bus error, then the shift register at the end of the bit shift will result in 00h. When writing the data to the device, the host must check the CRC received by processing the write data to ensure that there were no transmission errors and take appropriate corrective action before performing the next function.

8.3.10 Functional Register Map

The scratchpad-1 region and the IO register region together are referred to as the functional register map (see Figure 8-8). The scratchpad-1 region is 16 bytes deep, and has temperature result, device status, device configuration, short address, temperature alert limit and temperature offset registers. The IO register region has the IO read and IO configuration registers. Some of the registers can be committed to the configuration EEPROM to ensure that the device settings are restored on power up without the host rewriting the configuration.

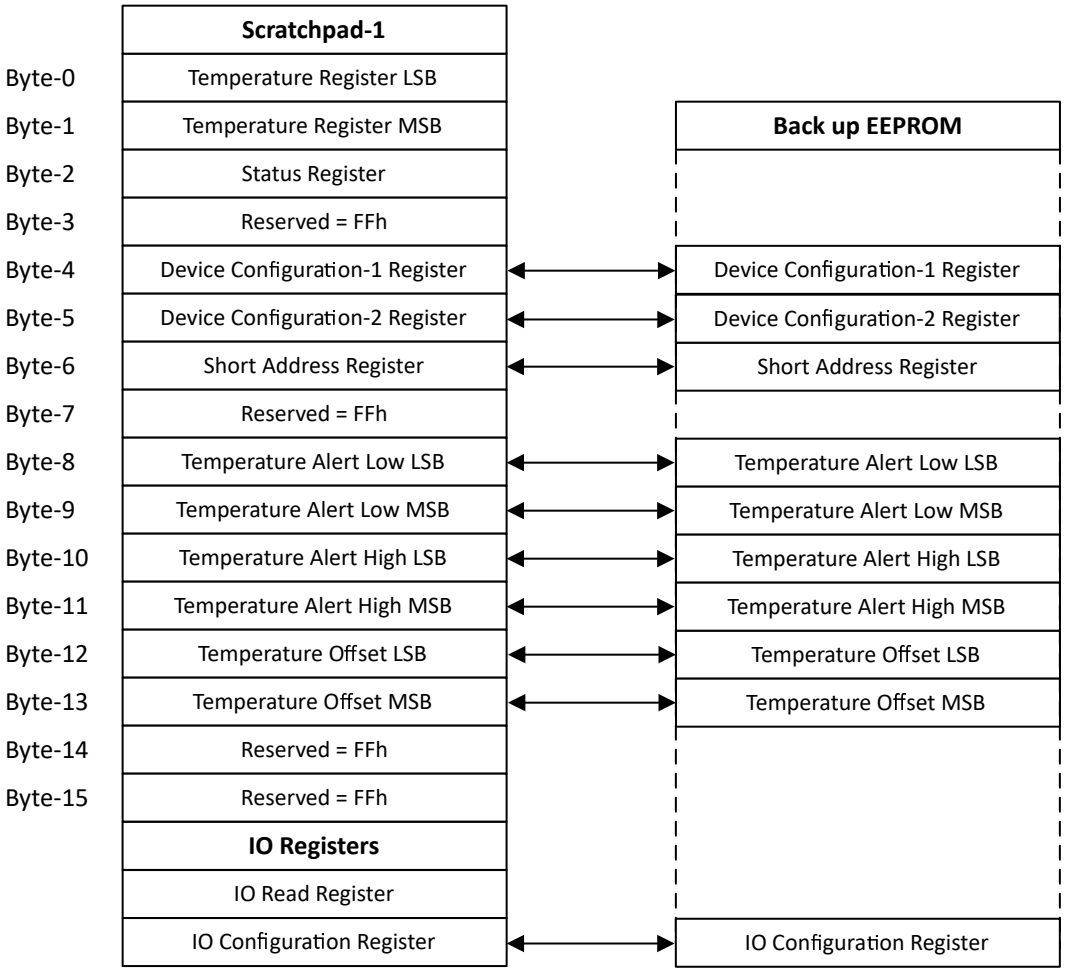


Figure 8-8. Functional Register Map (Scratchpad-1)

8.3.11 User Memory Map

The EEPROM memory is organized as 8 pages of 4 blocks each. Figure 8-9 shows that each block is 8 bytes or 64 bits. This results in a total user memory of 2048 bits. All memory access to the device shall be increments of a block size of 8 bytes. Access to the memory for programming is done through the scratchpad-2 register. The host writes to the scratchpad-2 register, which allows the device to perform a read before committing the content to the memory.

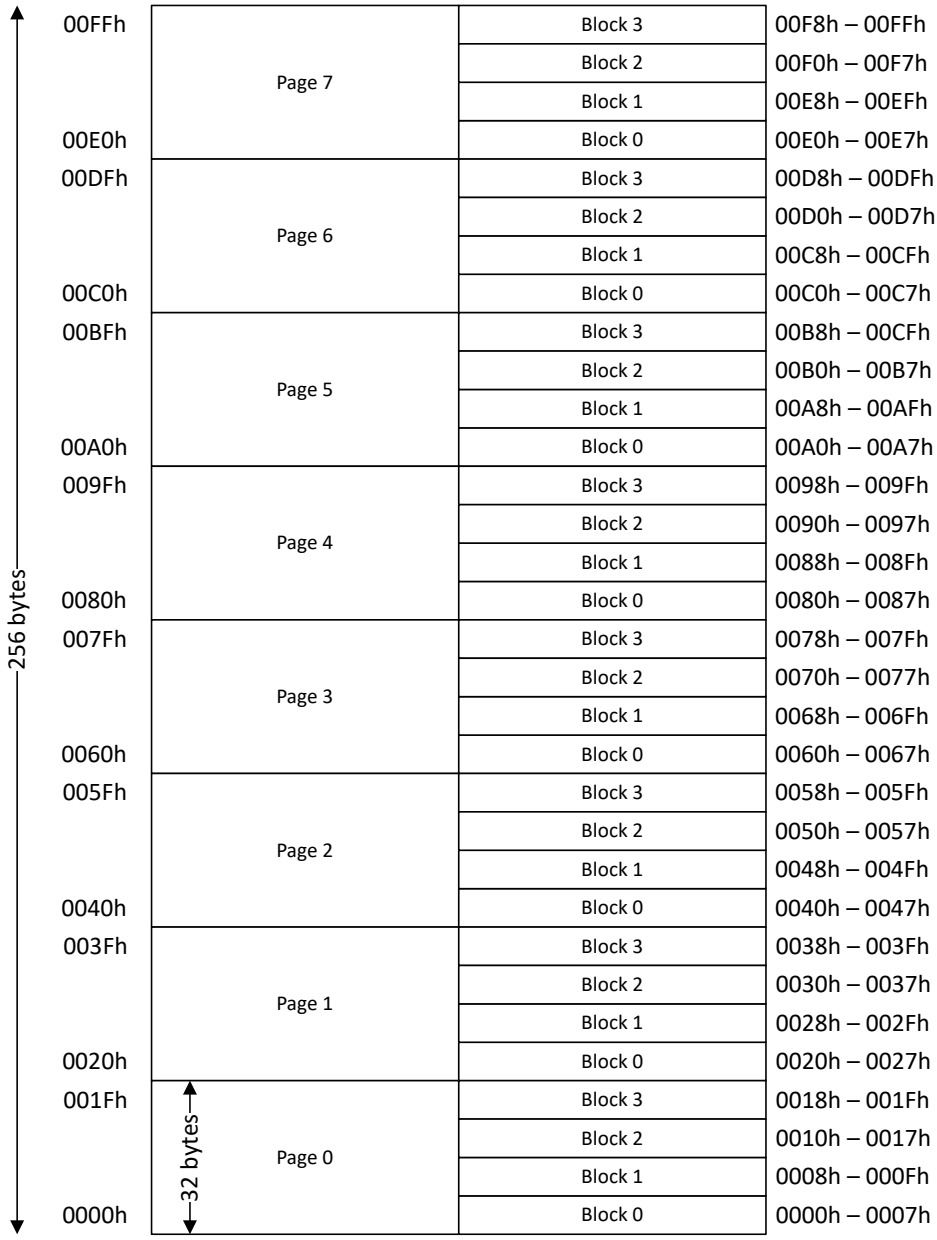


Figure 8-9. Address to EEPROM Page and Block Map

Note

The device shall return "1" for any device read without a CRC if the address is outside the user memory map.

8.3.12 SHA-256-HMAC Authentication Block

The authentication block on the TMP1827 device uses a keyed-hash message authentication code (HMAC) which is FIPS PUB-198-1 compliant SHA-256 hash implementation. The SHA-256 implementation itself is FIPS PUB-180-4 compliant. The HMAC engine does not encrypt the data, but generates a 256-bit hash based on the user programmed keys.

For details on SHA-256-HMAC authentication block, refer to the *TMP1827 Security Programming Guide*.

ADVANCE INFORMATION

8.3.13 Bit Communication

The single-wire interface communication does not have a reference clock, therefore all communication is performed asynchronously with fixed time slot (t_{SLOT}) and variable pulse width to indicate logic '0' and '1'. In idle state, the external pullup resistor holds the line high. All bit communication, whether it is a write or a read, are initiated by the host by driving the data line low to generate a falling edge and the bit value is decoded as the time for which the data line is held low or high after the falling edge.

Even though the communication is one bit at a time, the data exchanged between the host and device is performed at byte boundary. Every byte is sent least significant bit first. The device behavior is not ensured when incomplete bytes are sent.

8.3.13.1 Host Write, Device Read

A host write is the means by which the host sends the command, function, and data to the devices. A host write starts by the host driving the data line low as shown in Figure 8-10. If the host intends to transmit a logic '1', the line is released after t_{WR1L} time. If the host intends to transmit a logic '0', the line is released after t_{WR0L}. After releasing the data, the pullup resistor causes the line to become high till the beginning of the next time slot. The device samples the line after t_{RDV} has elapsed from the falling edge, for a time frame indicated by t_{DSW}. The host must factor the rise time due to the pullup resistor and bus capacitance to determine the release of the data line before the line is sampled by the device and the host drives the next write bit time slot.

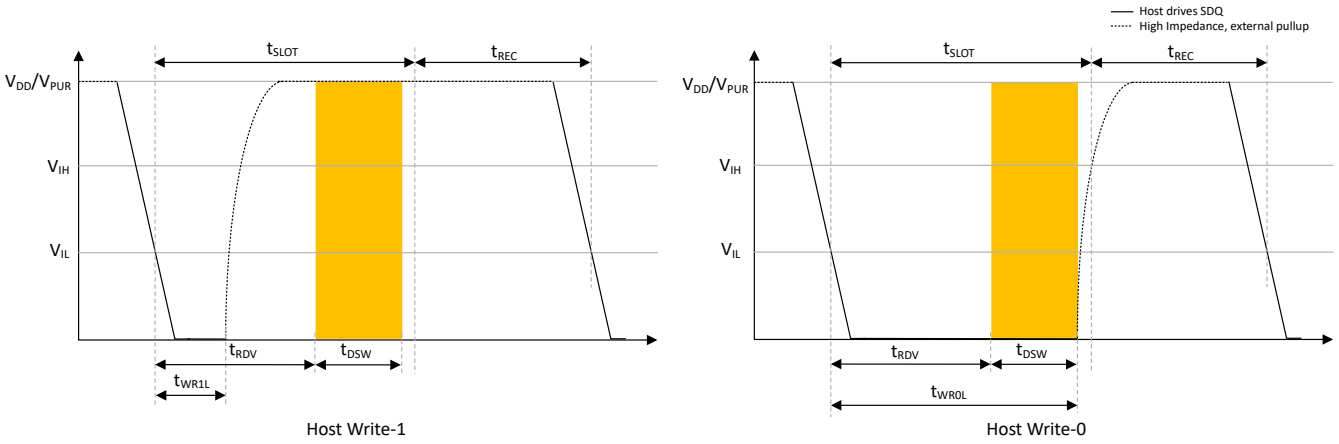


Figure 8-10. Host Write, Device Read

8.3.13.2 Host Read, Device Write

A host read is the means by which the hosts gets the data from the device or the CRC for data integrity check. A host read starts by the host driving the data line low as shown in Figure 8-11. When the device detects the falling edge, the device can drive the line low before the time t_{RL}. The host can release the bus from the side after the time $t_{RL(MIN)}$ elapses. If the device intends to transmit a logic '1', then the bus is released before $t_{RL(MAX)}$ elapses. If the device intends to transmit a logic '0', then the bus is released after $t_{SLOT(MIN)}$. The host must sample the line after the time t_{RWAIT}, for a time frame indicated by t_{MSW}. The host must factor the rise time due to the pullup resistor and bus capacitance to determine the sampling window for the host to sample the bit level sent by the device or to drive the next read bit time slot.

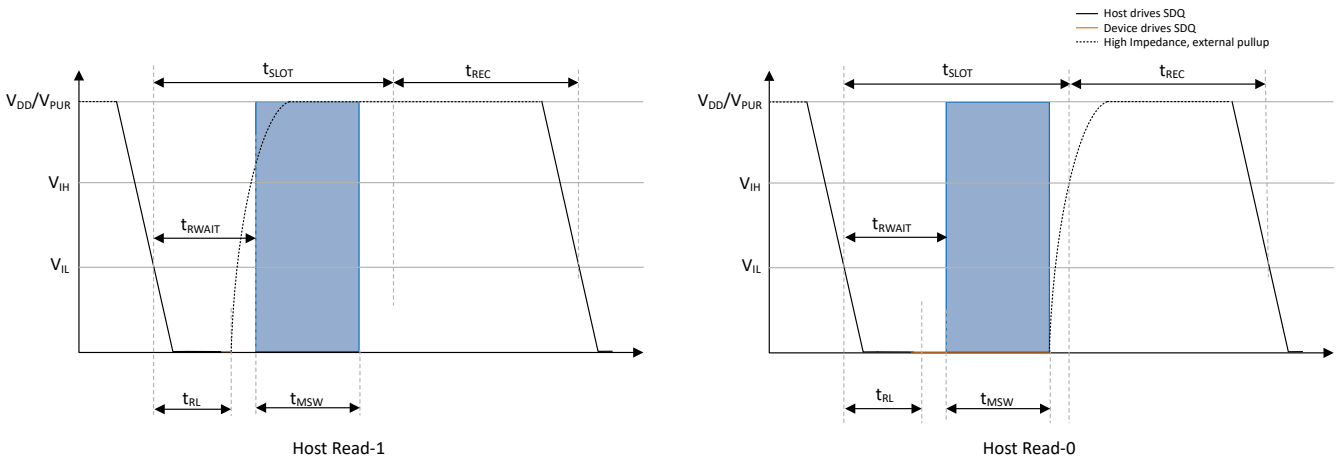


Figure 8-11. Host Read, Device Write

8.3.14 Bus Speed

The device supports both standard speed (8.33 kbps) and overdrive speed (90 kbps) data rates. All devices are factory programmed to start in overdrive speed, to enable higher data throughput. If the host requires the device to operate at standard speed, then it can easily switch the device by issuing a standard speed bus reset. The seamless switch over allows host to leverage better data rates on new designs, while maintaining backward compatibility for older design.

Additionally, the device also provides the flexibility to switch from standard to overdrive speed mode using address phase commands of OVD SKIPADDR and OVD MATCHADDR.

- When host issues OVD SKIPADDR, then all devices on the bus switch from standard speed to overdrive speed.
- When host issues OVD MATCHADDR, then the device whose 64-bit device address matches the address that host sends, will switch from standard to overdrive speed.

8.3.15 NIST Traceability

The accuracy of temperature testing is verified with equipment that is calibrated by an accredited lab that complies with ISO/IEC 17025 policies and procedures. Each device is tested and trimmed to conform to its respective data sheet specification limits.

ADVANCE INFORMATION

8.4 Device Functional Modes

The TMP1827 device features flexible temperature conversion modes along with robust user EEPROM architecture, which is described in the sections below.

8.4.1 Conversion Modes

The TMP1827 supports both one-shot and continuous conversion modes. There are different methods for one-shot conversion modes, that may be used based on single device or multiple device bus network. The continuous conversion mode is only supported in V_{DD} powered mode. Each of the conversion modes are with single temperature sample, but the host can enable 8 samples averages in the device for improved accuracy.

8.4.1.1 Basic One-Shot Conversion Mode

The basic one-shot conversion mode is the default conversion mode. The device goes through a bus reset, address and function phase to initiate the temperature conversion. During the communication, the device is in shutdown mode. When the conversion request is registered by the device, the device starts active conversion and then goes back to low power shutdown mode as shown in Figure 8-12. If the device is in continuous conversion mode, then the one-shot conversion mode request is ignored.

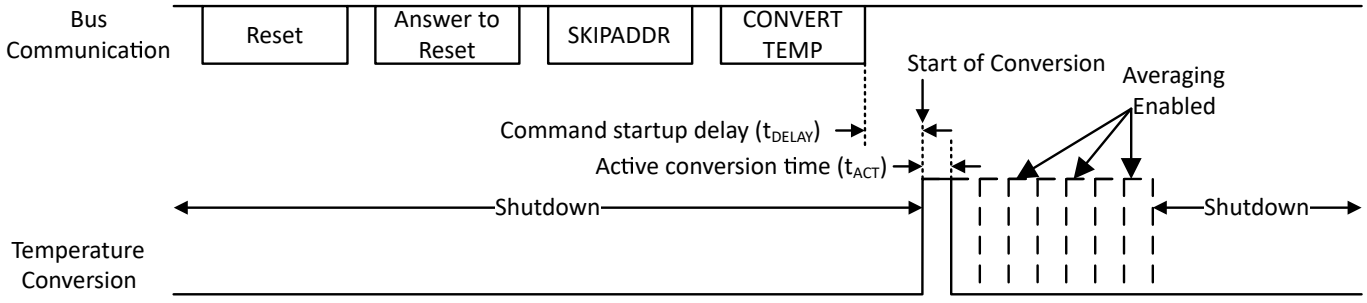


Figure 8-12. One-Shot Conversion Mode

As shown in Figure 8-13, there is no change in how one-shot conversion is performed when there are multiple devices on the bus. However, as there are multiple devices, the combined current drain in bus powered mode of operation may cause the bus voltage to drop. In such use cases, it is required that the host implement a low impedance current path using a FET/transistor switch. This path is switched on so as to meet the current requirement of the bus during an active conversion and after the active conversion duration is complete, it is switched off for bus communication.

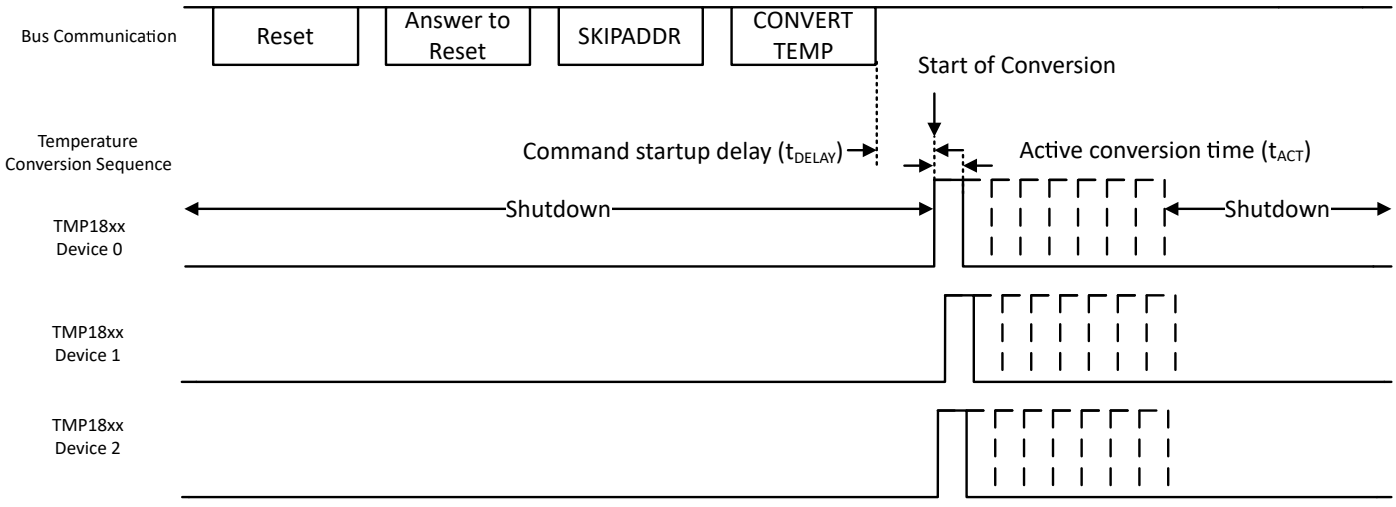


Figure 8-13. Multiple Device One-Shot Conversion Mode

8.4.1.2 Auto Conversion Mode

The auto conversion mode is a programmable feature in bus powered mode that can be enabled by setting the CONV_MODE_SEL as '10b' in the device configuration-1 register. As shown in Figure 8-14, the host can skip the issue of the temperature conversion request and directly read the temperature data from the device when the auto conversion mode is enabled. This enables the application to speed up the temperature conversion and read, because the request command is no longer required. As in the case for multiple device bus, a low impedance current path is required to meet the current requirement of the bus during the active conversions.

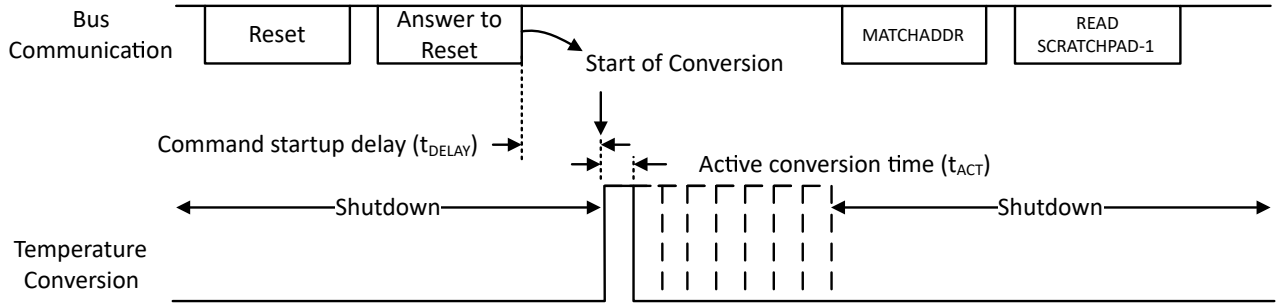
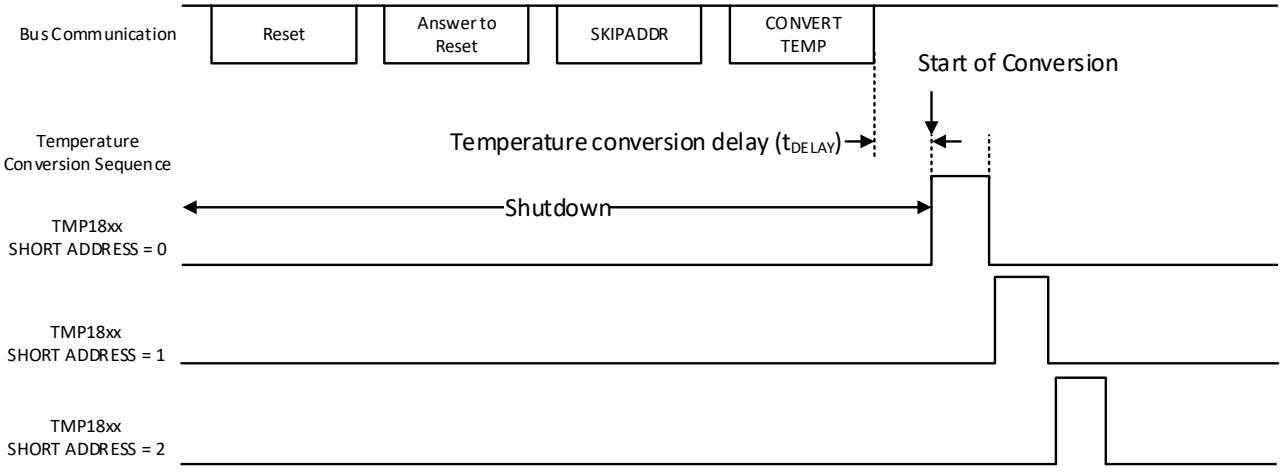


Figure 8-14. Auto Conversion Mode

8.4.1.3 Stacked Conversion Mode

The stacked conversion mode is a programmable feature in bus powered mode that can be enabled by setting CONV_MODE_SEL as '01b' in the device configuration-1 register. As shown in Figure 8-15, the devices can use the address programmed in the short address register to delay the temperature conversion for the devices when the stacked conversion mode is enabled. No more than two devices are actively converting at any given time, therefore the current drain in bus powered configuration is limited. This allows the application to avoid simultaneous temperature conversion by multiple parts and reducing the user system maximal supply current.



Note

The host controller must program all the device with the same setting for CONV_TIME_SEL and AVG_SEL to ensure that no more than two devices are actively converting to use the feature as it is intended.

Figure 8-15. Stacked Conversion Mode

8.4.1.4 Continuous Conversion Mode

The continuous conversion mode is applicable only in V_{DD} powered mode of operation for the device. This mode can be enabled by writing a value other than '000b' to CONV_MODE_SEL bits in the device configuration-1 register. As shown in Figure 8-16, the device can perform periodic conversions at the interval programmed

ADVANCE INFORMATION

by the host and updates the temperature result register when continuous conversion mode is enabled. The device also performs the alert threshold check and sets the flags and alert pin, if configured accordingly. When in continuous conversion mode, the CONVERTTEMP function has no effect on the temperature conversion request. The application can at any time change the rate of conversion or put the device back into one-shot conversion mode, and this takes effect only after the current conversion is complete.

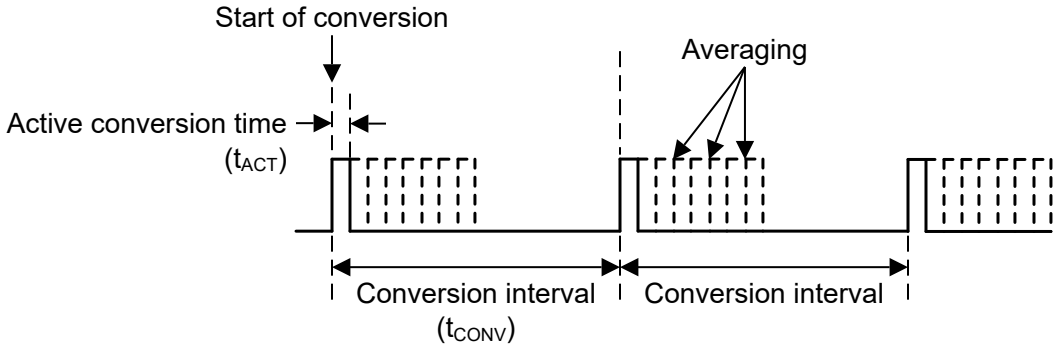


Figure 8-16. Continuous Conversion Mode

If due to any reason, the V_{DD} supply fails without the device going through a brown out, causing the device to move to bus powered mode of operation, the conversion mode automatically reverts to the setting in the configuration EEPROM.

8.4.2 Alert Function

As described earlier, the built-in alert function can be used by the host to check if the temperature has crossed a certain threshold. The alert status bits are available in both bus powered and V_{DD} powered mode. The alert pin is available only in V_{DD} powered mode.

If the device is in V_{DD} powered mode and IO2/$\overline{\text{ALERT}}$ is configured to function as an IO2/$\overline{\text{ALERT}}$ pin, then the pin shall be driven active low when the threshold crossing occurs. The pin is open-drain, and therefore requires a pullup resistor. The IO2/$\overline{\text{ALERT}}$ pin deassertion is based on the setting of the ALERT_MODE setting in the device configuration-1 register.

8.4.2.1 Alert Mode

The device operates in alert mode, when the ALERT_MODE is set as '0b'. In the alert mode of operation, the alert status flag and IO2/$\overline{\text{ALERT}}$ pin are asserted when the last temperature conversion is either higher than the temperature alert high limit or when it is lower than the temperature alert low limit register.

The alert status flag and IO2/$\overline{\text{ALERT}}$ pin are deasserted only when the host reads the status register or performs a successful ALERTSEARCH command as shown in Figure 8-17.

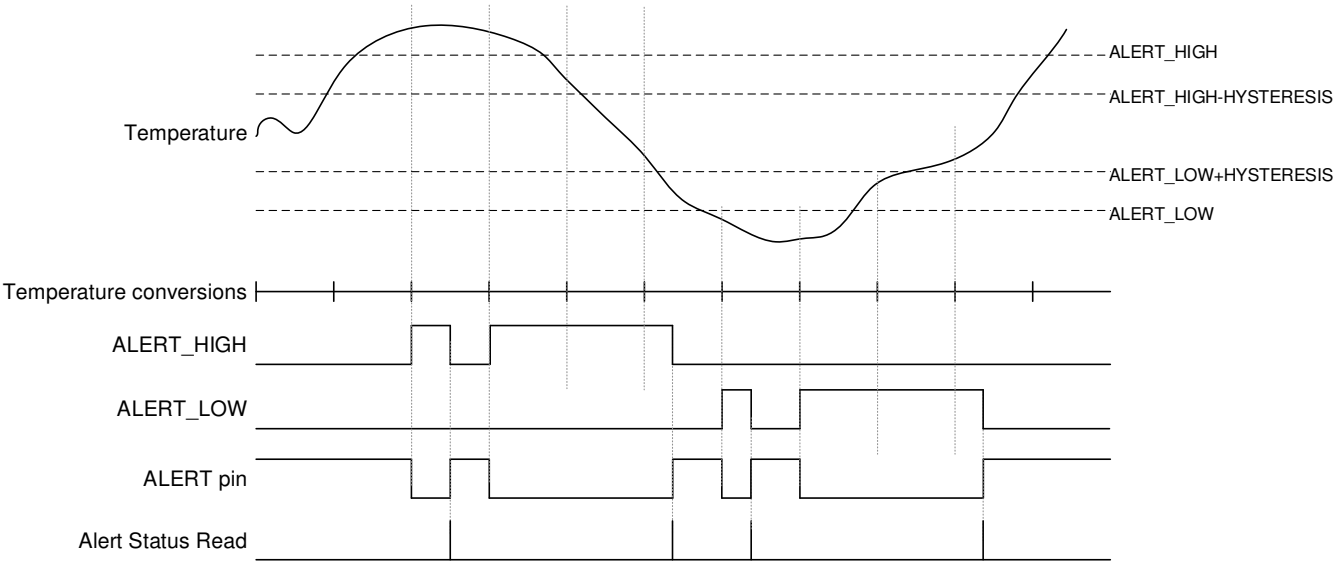


Figure 8-17. Alert Mode Timing Diagram

8.4.2.2 Comparator Mode

The device operates in comparator mode, when the ALERT_MODE is set as '1b'. In the alert mode of operation, the alert status flag and IO2/$\overline{\text{ALERT}}$ pin are asserted when the last temperature conversion is either higher than the temperature alert high limit or when it is lower than the temperature alert low limit register.

The alert status flag and IO2/$\overline{\text{ALERT}}$ pin are deasserted only when the result of the last temperature conversion is less than the temperature alert high limit minus the hysteresis or above the temperature low limit plus the hysteresis as shown in Figure 8-18. The hysteresis is selectable using the HYSTERESIS bit field in the device configuration-2 register.

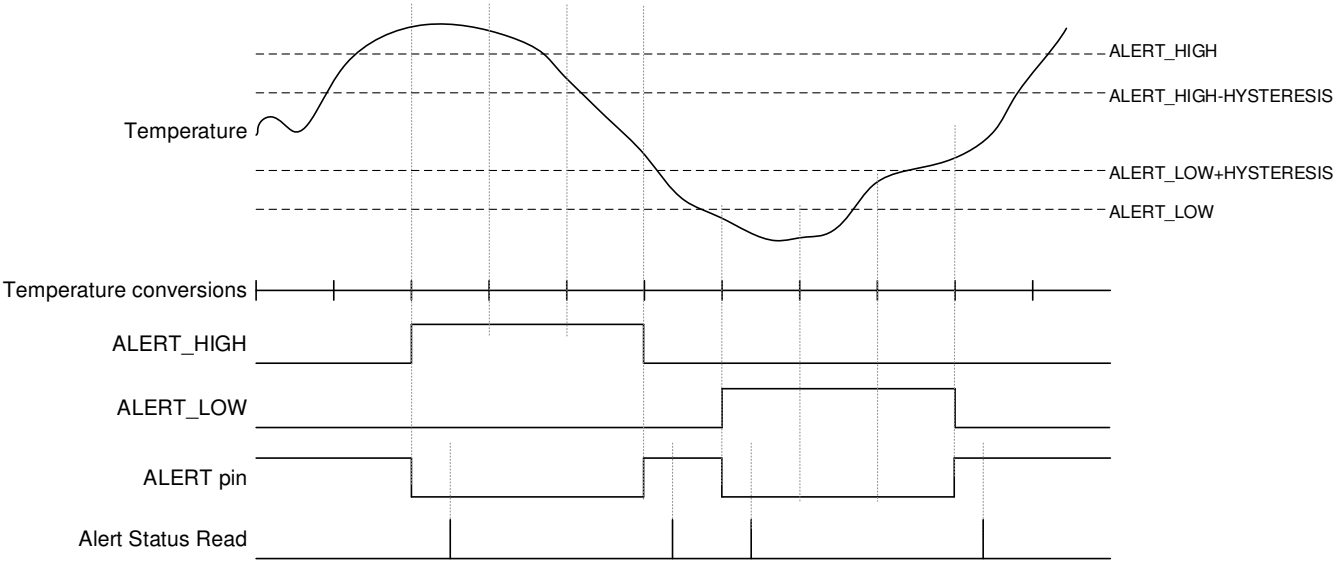


Figure 8-18. Comparator Mode Timing Diagram

8.4.3 Single-Wire Interface Communication

To leverage the features effectively, the device access consists of 3 distinct phases. As shown in Figure 8-19, any bus communication starts with a bus reset condition to which every device on the bus must respond. This is

ADVANCE INFORMATION

followed by a highly configurable address phase, where the host selects the device it wants to access. Finally, there is a function phase where the host provides the selected device(s) the action it wants to take.

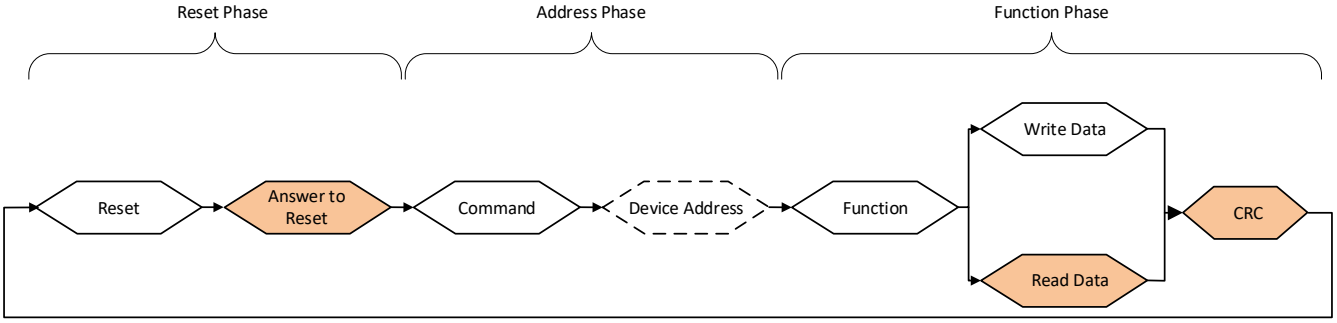


Figure 8-19. Single-Wire Bus Communication

In a single-wire bus, all write and reads are initiated by the host except for the answer to reset which is initiated by the devices on the bus.

8.4.3.1 Bus Reset Phase

The bus reset phase is the beginning of the communication. The phase is initiated by the host by holding the single-wire data line low for a period t_{RSTL}. All devices on the bus, irrespective of their current state shall respond to the bus reset, by reinitializing their internal state and responding to the host initiated bus reset. The devices respond after a minimum of t_{PDH}, by holding the single-wire low for a time period of t_{RSTH} as shown in Figure 7-1.

All devices are configured with the OD_EN bit set as '1' in the device configuration-2 register. If the host sends a bus reset pulse of 48 µs to 80 µs, then only devices operating in overdrive speed shall respond to the bus reset pulse, while devices operating in standard mode shall continue to wait for a standard mode bus reset.

If the host sends a bus reset pulse of minimum t_{RSTL} for standard mode, the device shall reset the OD_EN bit to '0' and respond to the bus reset in standard mode. If the bus consists of mixed standard and overdrive speed devices, then sending a bus reset pulse in standard mode shall reset all devices to standard mode speed of operation.

It is illegal for the host to send the bus reset for a particular speed of operation and then communicate at the other speed mode. Also, if a bus reset pulse is sent which is greater than 80 µs (but less than 480 µs), then the device shall be reset, though the device operation is not ensured.

8.4.3.2 Address Phase

Figure 8-20 shows the address phase that follows the bus reset phase. During this phase, the host presents 8-bit commands which may be followed by either host sending a 64-bit device address, a 8-bit flexible address, or skipping the address. Some of the commands are used to discover the device address, while others are used to select the device.

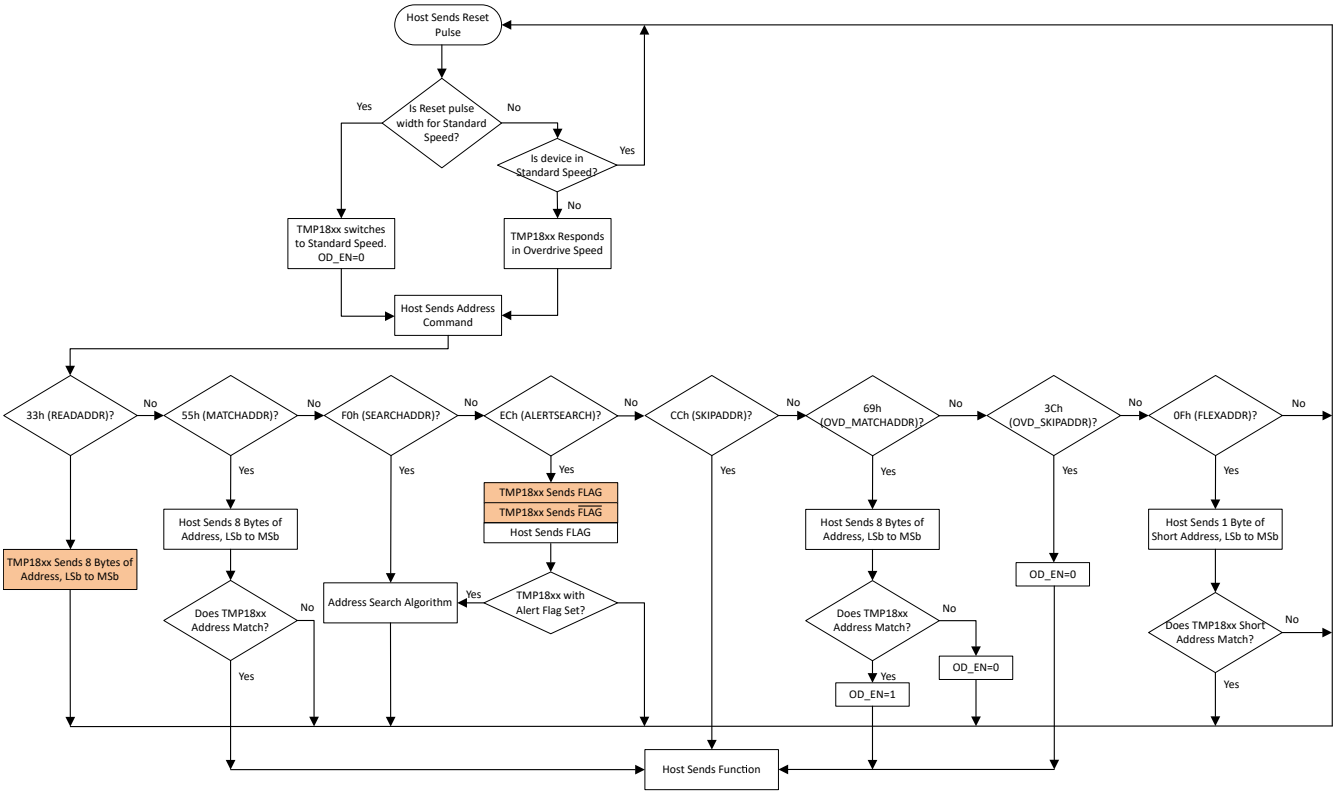


Figure 8-20. Address Phase Flowchart

8.4.3.2.1 READADDR (33h)

The command can be used by the host to read the 64-bit address of the device. This command must only be used when there is one device on the bus, as this command will cause a collision if multiple devices are present on the bus.

8.4.3.2.2 MATCHADDR (55h)

The command is used by the host and is followed by a 64-bit address that is used to select a single device on the bus. The address for each device is unique, therefore only one device can be selected by the command while all other devices continue to wait for a bus reset.

8.4.3.2.3 SEARCHADDR (F0h)

The command is used by the host to identify the 64-bit address of each of the devices on the bus after the system is powered up (see Figure 8-21). Additionally, this command may be run by the host to discover any new devices that may be added to the system later. When there is a single device bus, the host can skip the command and instead use the SKIPADDR command to access the device.

As shown in right side flow of Figure 8-21, when the fast arbitration mode is enabled by setting ARB_MODE bits as '11b' in the device configuration-2 register, the devices check the bus for the transmitted bit. If the device reads a bit value other than what they had transmitted, they no longer respond to the command until the next bus reset. A device that wins the bus continues until the 64th bit, after which it does not respond to the next SEARCHADDR command until the arbitration mode is reenabled. The arbitration function allows the host a fast discovery of the devices without having to go through the complicated, memory intensive and longer discovery method using traditional SEARCHADDR command. At the same time, if the host has an issue on the bus, then it can simply perform a broadcast write to disable and enable the arbitration mode to restart the fast arbitration mode.

The device also features an optimized arbitration mode which is enabled by setting ARB_MODE bits as '10b'. The devices check the transmitted bit, and if the devices detect a logic '0' when they send a logic '1', they do not participate in the SEARCHADDR command until the next SEARCHADDR command is sent. The device that

ADVANCE INFORMATION

is able to send all 64 bits successfully, wins the bus and does not participate in the arbitration till the mode is reenabled. As a result of the optimized arbitration mode, the host does not have to manage the complex memory structure to identify devices on the bus and can still use the legacy software search algorithm.

When the host has received the address of each device on the bus, the host must disable the arbitration mode and only enable it again if the host wants to use the SEARCHADDR command again when new devices are added to an existing bus.

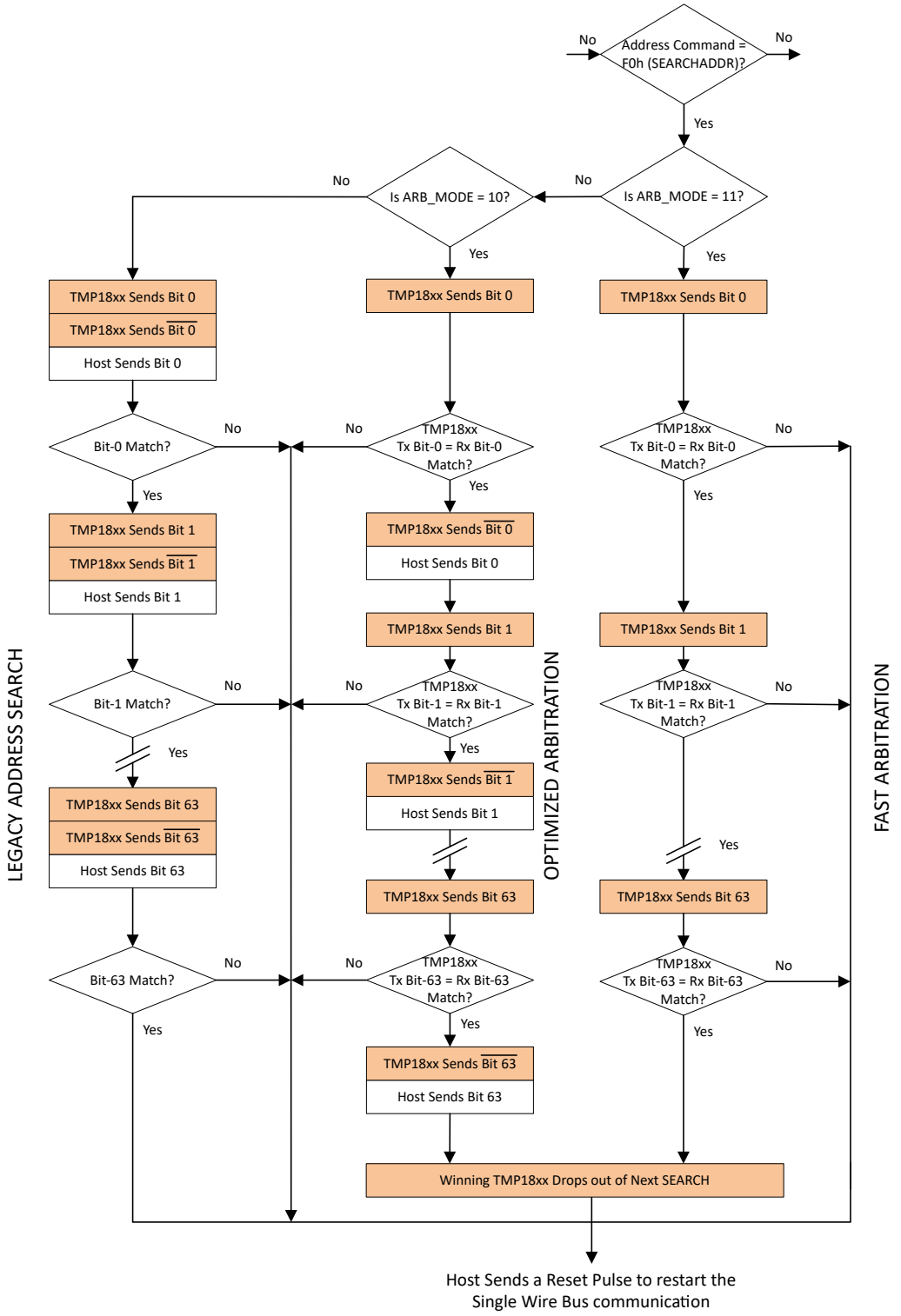


Figure 8-21. Address Search Algorithm Flowchart

8.4.3.2.4 ALERTSEARCH (ECh)

The command is used by the host to identify if any of the devices have an alarm condition that must be serviced. An alarm condition is set by the device when the temperature conversion is performed and the temperature result is higher than alert high temperature register or lower than alert low temperature register. The command uses the same method as the SEARCHADDR command, except that only devices with an alarm condition shall

respond. If none of the devices have an alarm condition, then the host shall get all '1' followed by '1' on the bus and host can send a bus reset subsequently. If the device sends a '1' followed by '0', the host shall interpret it as either one or more devices have an alert condition, or all devices have an alert condition. If there is a bus noise, that causes the line to be sample erroneously, but if no device has an alert condition, then the host shall get all '1' on the bus during the address search phase.

Only devices that have an alert set shall participate when they receive an ALERTSEARCH address command and shall respond by sending its 64-bit address. A device shall no longer participate in the send address phase if it successfully transmits the device address, which automatically clears the internal alert flags, unless another temperature conversion results in the alert condition getting set.

8.4.3.2.5 SKIPADDR (CCh)

The host can issue this command to select all the devices on the bus. This is useful when the host wants to write to the scratchpad-1 or trigger the temperature conversion for all the devices on the bus. Additionally, the host can use the command to increase the overall bus data throughput when there is a single device on the bus.

The host must take care to not issue the command when there are multiple devices on the bus,. If the host intended to read the devices with this command, it would cause a collision on the bus.

8.4.3.2.6 OVD SKIPADDR (3Ch)

The host can issue this command to select all devices which support overdrive speed in a mixed speed bus. This is useful when the host wants to write to the scratchpad-1 or trigger the temperature conversion for all the devices on the bus that support overdrive speeds. Additionally, the host can use the command to increase the overall bus data throughput when there is a single device on the bus. When the command is issued, only devices that support overdrive mode shall set the internal OD flag as '1'.

The host must take care to not issue the command when there are multiple devices on the bus which support overdrive mode. If the host intended to read the devices with this command, it would cause a collision on the bus.

If the host issues a standard mode bus reset at any time, all devices which have OD flag set as '1' shall clear the same and revert back to standard mode speed.

8.4.3.2.7 OVD MATCHADDR (69h)

The command is used by the host and is followed by a 64-bit address that is used to select a single device on the bus in overdrive speed. The address for each device is unique, therefore only one device can be selected by the command while all other devices have to wait for a bus reset. The selected device shall set its internal OD flag as '1', and start all further communication in overdrive speed.

If the host issues a standard mode bus reset at any time, or selects another device using the OVD MATCHADDR, then all other devices which have OD flag set as '1' shall clear the same and revert back to standard mode speed.

8.4.3.2.8 FLEXADDR (0Fh)

The host issues the command to access a device by its short address that is configured in the short address register. The short address itself is decoded by:

- Setting FLEX_ADDR_MODE[1:0] as '01b', for hardware address configured by IO0-IO3 tie off to either V_{DD}/SDQ or GND.
- Setting FLEX_ADDR_MODE[1:0] as '10b', for resistor address by connecting a resistor between ADDR and GND.
- Setting FLEX_ADDR_MODE[1:0] as '11b', for combined IO and resistor address decoding.

Using the command does not affect the 64-bit unique address of the device. This command is followed by one byte, which is the short address of the device, the host wants to select for further communication.

8.4.3.3 Function Phase

Figure 8-22, Figure 8-23 and Figure 8-24 show the function phase that follows the address phase. The host may present different functions during this phase, which is followed by either the host sending data to the device,

ADVANCE INFORMATION

reading device data, or starting a temperature conversion. Some of the functions may be broadcast to all the devices on the bus using SKIPADDR or OVD SKIPADDR. Read functions must always be unicast with a device selected during the address phase using MATCHADDR, FLEXADDR or OVD MATCHADDR. For cases, where there is a single device on the bus, the device address selection may be skipped.

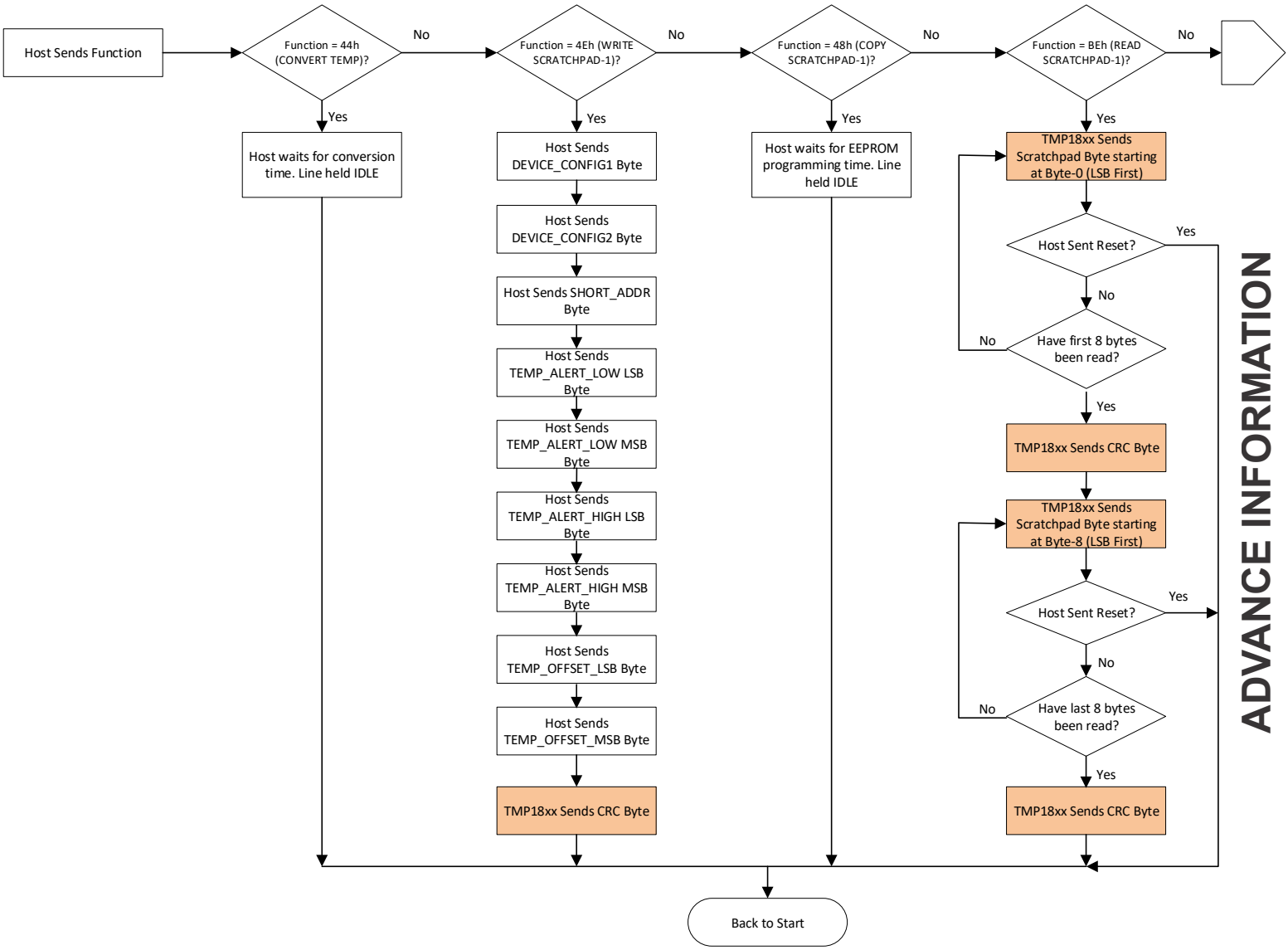


Figure 8-22. Function Phase Flowchart for Register Space

8.4.3.3.1 CONVERTTEMP (44h)

The function is issued by the host when the host wants the temperature sensors on the bus to perform a one-shot temperature conversion.

When the device is bus powered, the host must keep the bus idle for the duration of the active temperature conversion. The active temperature conversion time is dependent on the conversion mode. After temperature conversion has completed, the result is updated in temperature result LSB and temperature result MSB registers.

When automatic temperature conversion mode is enabled in the device configuration-1 register, the command may be skipped altogether, allowing faster access to the temperature result.

8.4.3.3.2 WRITE SCRATCHPAD-1 (4Eh)

The function is issued by the host to write the functional register for the temperature sensor. Following the function byte, the host transmits the device configuration registers, short address register, temperature alert low limit registers, temperature alert high limit registers and temperature offset registers. After sending the 9 bytes, the device shall transmit the CRC computed on the 9 bytes and send the CRC back to the host for quick verification of data integrity.

Additionally, the host can issue a bus reset at any time during the transfer, though it is advised that the same may be done only at byte boundary to ensure that there is no register corrupted due to incomplete transfer.

When the FLEX_ADDR_MODE bits are updated as a non-zero value, the host must hold off on any communication to keep the bus in idle state for either t_{RESDET} or t_{DELAY}, as per the requested flex mode, to allow the device to decode and update the short address. Also when the FLEX_ADDR_MODE bits have a non-zero value, the byte for short address register shall not be updated in the register scratchpad, for any subsequent write scratchpad-1 operations, to avoid the overwrite of the decoded short address.

Note

When updating the OD_EN and/or LOCK_EN bit in the device configuration-2 register, the host controller must send the 9 bytes and wait for the CRC transmission before the change of device speed or write protection of the register scratchpad can take effect. If the host terminates the transfer before the complete CRC transmission, then any update to OD_EN and/or LOCK_EN shall not take effect.

8.4.3.3.3 READ SCRATCHPAD-1 (BEh)

The function is issued by the host to read the temperature result, status bits, and functional registers from the register scratchpad. The selected device transmits the first 8 bytes of the register scratchpad followed by CRC of the 8 bytes. If the host wants to continue the read operation, the host will receive the next 8 bytes along with CRC for the last 8 bytes. The host can terminate the function at any point by issuing a bus reset.

8.4.3.3.4 COPY SCRATCHPAD-1 (48h)

The function is issued by the host to copy the functional registers content to the EEPROM. As shown in Figure 8-22, the temperature alert registers, configuration register, short address register, and temperature offset registers are stored in the configuration EEPROM. There are 9 bytes being copied from the register space to

ADVANCE INFORMATION

the NVM, therefore the host must hold the bus in idle state for twice the EEPROM programming time before it performs the next access.

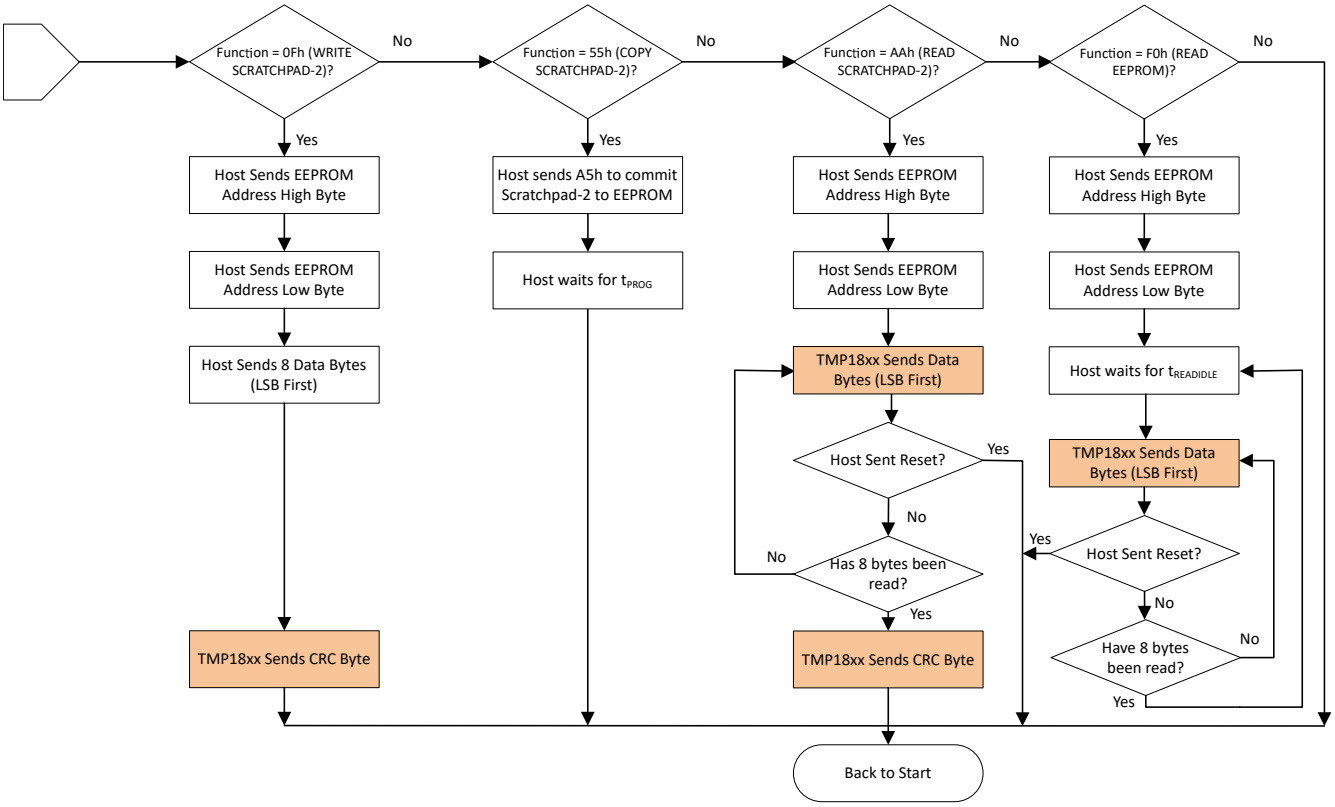


Figure 8-23. Function Phase Flowchart for Memory Access

8.4.3.3.5 WRITE SCRATCHPAD-2 (0Fh)

The function is issued by the host to prepare data write to the EEPROM using memory scratchpad.

Figure 8-23 shows that the host first sends 2 bytes for the EEPROM address, followed by 8 data bytes. On receiving the 8 data bytes, the device computes the CRC for total of 10 bytes of address and data received from the host for data integrity check. The function only copies the data to the memory scratchpad, to enable the host to change data, before the final EEPROM erase and program. Additionally, the host may use the memory scratchpad as a 8-byte volatile buffer.

The device does not support byte wise access for EEPROM. All access to the scratchpad are done in increments of 8 bytes. Hence the host must send the address at the 8-byte block boundary. Figure 8-9 shows that any attempt to write data at a non-block boundary will result in data corruption for the corresponding EEPROM page and block.

8.4.3.3.6 READ SCRATCHPAD-2 (AAh)

The function is issued by the host to read the content of the memory scratchpad.

The host first sends the 2 bytes for the EEPROM address (see Figure 8-23). If the 2 bytes of address matches the address sent during the last WRITE SCRATCHPAD-2, the device responds by sending the 8 bytes of data that was written to the scratchpad-2 buffer earlier. The host can send a bus reset any time during the transfer. If the device sends all 8 bytes and no bus reset is received,the device transmits the CRC computed on the 2 byte of address sent by the host and 8 bytes of data sent by the device to the host for data integrity check.

If there is a mismatch in the address, the device shall go back to the start and wait for a bus reset to restart communication, and the host shall receive '1' on the bus for any subsequent read. This mechanism ensures that the host can detect an address byte corruption during both WRITE SCRATCHPAD-2 and READ SCRATCHPAD-2, as both the data bytes and CRC byte will read back as FFh.

ADVANCE INFORMATION

8.4.3.3.7 COPY SCRATCHPAD-2 (55h)

The function is issued by the host to copy the contents of scratchpad-2 to the EEPROM. The EEPROM current is higher during the erase and program, therefore the application must size the external pullup resistor to ensure that there is sufficient current drawn by the multiple devices or implement a low impedance current path using an external FET/transistor switch parallel to the bus pullup resistor.

The host application must ensure that only WRITE SCRATCHPAD-2 or READ SCRATCHPAD-2, with address of the intended location in the user EEPROM, are issued before COPY SCRATCHPAD-2 is sent. The device stores and uses the address sent during WRITE SCRATCHPAD-2 to identify the location in the user EEPROM where the copy operation shall be performed. The host only needs to send one byte with A5h to initiate the copy of the memory content from scratchpad-2 to the user EEPROM, at the address location already specified, when performing the commit operation. The host must hold the bus in idle state for the EEPROM programming time before starting any new access on the bus.

8.4.3.3.8 READ EEPROM (F0h)

The function is issued by the host to read the EEPROM memory directly.

The host sends 2 bytes for the address of the EEPROM location, that it wants to read. The device then sends the data bytes starting from that location until the internal address pointer does not reach the end of the EEPROM or host does not issue a bus reset. If the internal address pointer reaches end of the EEPROM location, the device shall send 1's on the bus. After sending the 2 bytes for the address of the EEPROM location to access, and when moving between block boundary, the host must idle the bus for t_{IDLE} as specified in the EEPROM characteristics. Additionally, there is no CRC provided in the response from the device during the READ EEPROM function.

The device does not support byte wise access for EEPROM. All access to the memory is done in increments of 8 bytes. Hence the host must send the address at the 8-byte block boundary. If the address is sent for a non-block boundary, the device shall send data from the start of the corresponding block as shown in Figure 8-9.

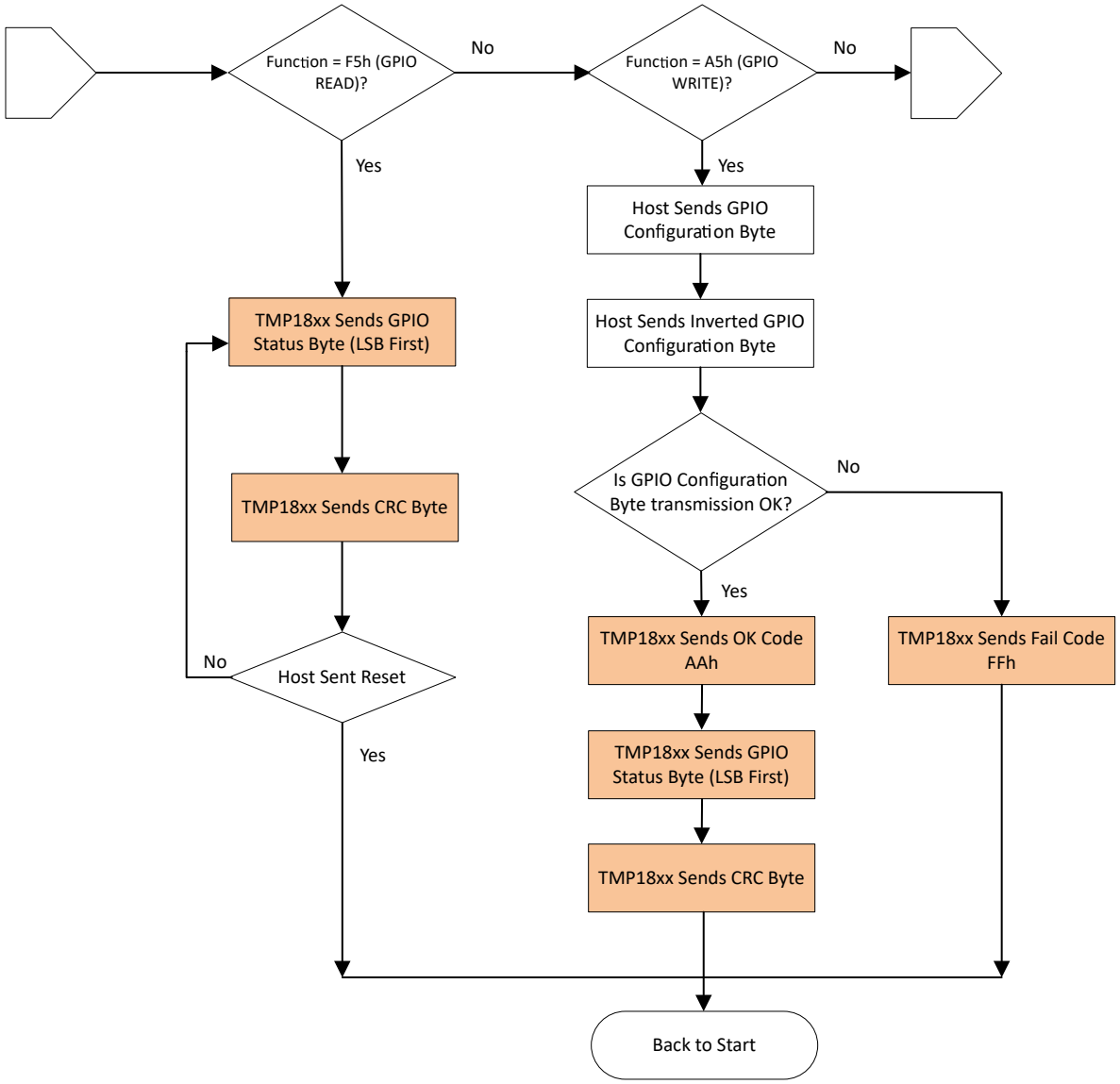


Figure 8-24. Function Phase Flowchart for IO Access

8.4.3.3.9 GPIO WRITE (A5h)

The function is issued by the host to configure and read the GPIO.

The host sends the IO configuration byte, followed by the inverted IO configuration byte value. This enables the device to check for bit error due to bus noise. If there errors detected, then the device shall transmit a fail code of FFh to the host, for the host to retry. If there are no errors detected, then the device shall transmit the success code of AAh. The host may issue a bus reset and terminate the transaction or may proceed to read of the IO state, where the device shall send the IO read byte, followed by the CRC byte for the IO status byte.

The host must send a bus reset to terminate the function and bring the device back to its idle state.

8.4.3.3.10 GPIO READ (F5h)

The function is issued by the host to read the GPIO.

ADVANCE INFORMATION

After issuing the function, the device sends a byte which has the corresponding IO status, followed by the CRC for the IO status byte. The host may repeat the sequence or may send a bus reset to terminate the function.

8.4.4 NVM Operations

The TMP1827 device follows a common procedure for programming of keys, programming user data and enabling the memory protection for user data and keys.

8.4.4.1 Programming User Data

Programming of user data to the memory use the functions WRITE SCRATCHPAD-2, READ SCRATCHPAD-2 and COPY SCRATCHPAD-2 as described earlier. The application must use the address in the provided functional memory map to write user data to the device.

1. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
2. Host issues a WRITE SCRATCHPAD-2 with the address as per the functional memory map and the 8 bytes of data.
3. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
4. Host issues a READ SCARTCHPAD-2 with the address as per the functional memory map, then reads the 8 bytes of data to ensure that it is same as what was written in the earlier step.
5. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
6. Host issues a COPY SCRATCHPAD-2 with the data bytes as A5h to commit the data to user EEPROM.

8.4.4.2 Register and Memory Protection

The TMP1827 provides user configurable protection for both the register scratchpad and the memory region as described below.

8.4.4.2.1 Register Protection

The device provides for a one-time write protection for the entire register map. All the writable registers, except for IO configuration, can be write-protected. To enable the write protection permanently, the host controller must set LOCK_EN bit in the device configuration-2 register, then copy the register to the configuration EEPROM. When the configuration EEPROM is programmed, the change is permanent and irreversible.

Additionally, the device provides temporary write protection mechanism. If the LOCK_EN bit is not committed to configuration EEPROM, the device shall prevent any write to the register scratchpad-1 region as long as power is applied. If the device goes through a POR, then the LOCK_EN bit shall be cleared to allow the host to update the register scratchpad-1.

8.4.4.2.2 User Memory Protection

For additional details on user memory protection, refer to the *TMP1827 Security Programming Guide*.

ADVANCE INFORMATION

8.5 Programming

The TMP1827 has multiple methods in which an application can access the device functions for temperature conversion and EEPROM programming. When accessing multiple device the MATCHADDR command along with the 64-bit device address must be used. If the short address has been programmed uniquely, then the host may use the FLEXADDR command along with the 8-bit short address must be used.

The sections below describe the sequences that must be followed to access the device functions properly.

8.5.1 Single Device Temperature Conversion and Read

Figure 8-25 shows the program flow that the host MCU must execute for temperature conversion and subsequent read of the temperature result. As the temperature results are the first two bytes of the register scratchpad, the host may optionally stop the read after the device transmits the first two bytes by performing a bus reset.

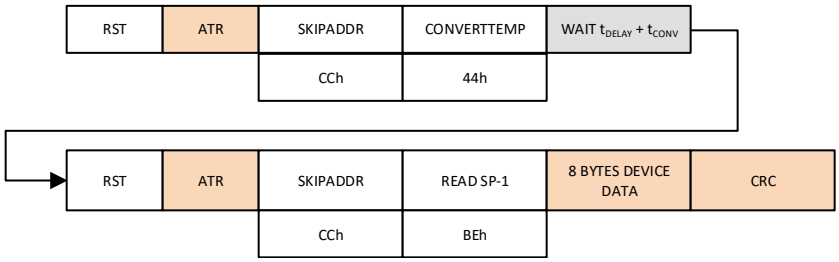


Figure 8-25. Single Device Temperature Conversion and Read Programming Flow

8.5.2 Multiple Device Temperature Conversion and Read

Figure 8-26 shows the program flow that the host MCU must execute for temperature conversion and subsequent read of the temperature result for multiple devices. The host must use the MATCHADDR command **or the FLEXADDR command** to address each device on the bus, because the devices do not arbitrate on a read function.

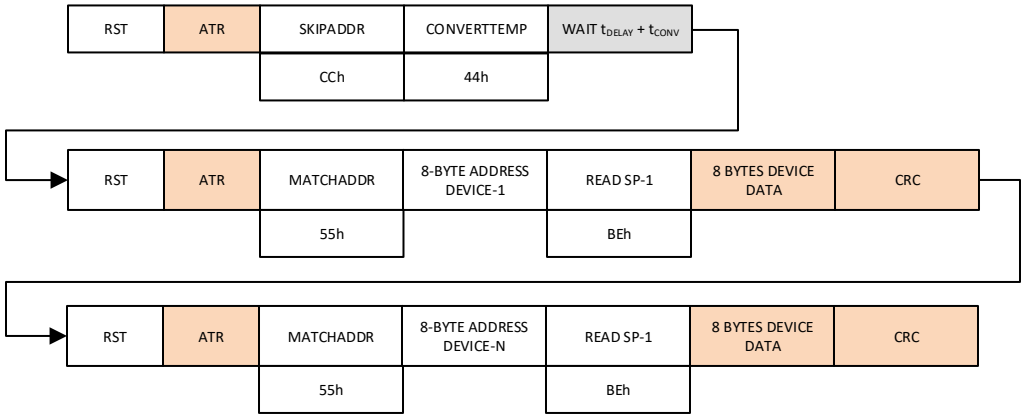


Figure 8-26. Multiple Device Temperature Conversion and Read Programming Flow

8.5.3 Register Scratchpad Update and Commit

Figure 8-27 shows the sequence the host must execute to update the register scratchpad and commit to the configuration EEPROM. The host must read the scratchpad to ensure it can perform the correct read modify write to the register locations, before it commits the same to the configuration EEPROM.

If the host has only one device, or if the application can guarantee no bus corruption, then it may use SKIPADDR command to globally update and commit the register scratchpad region. However once committed and locked, it is not possible for the host to update the locations anymore, and hence TI strongly advises that the host still read the locations before running the commit operation.

ADVANCE INFORMATION

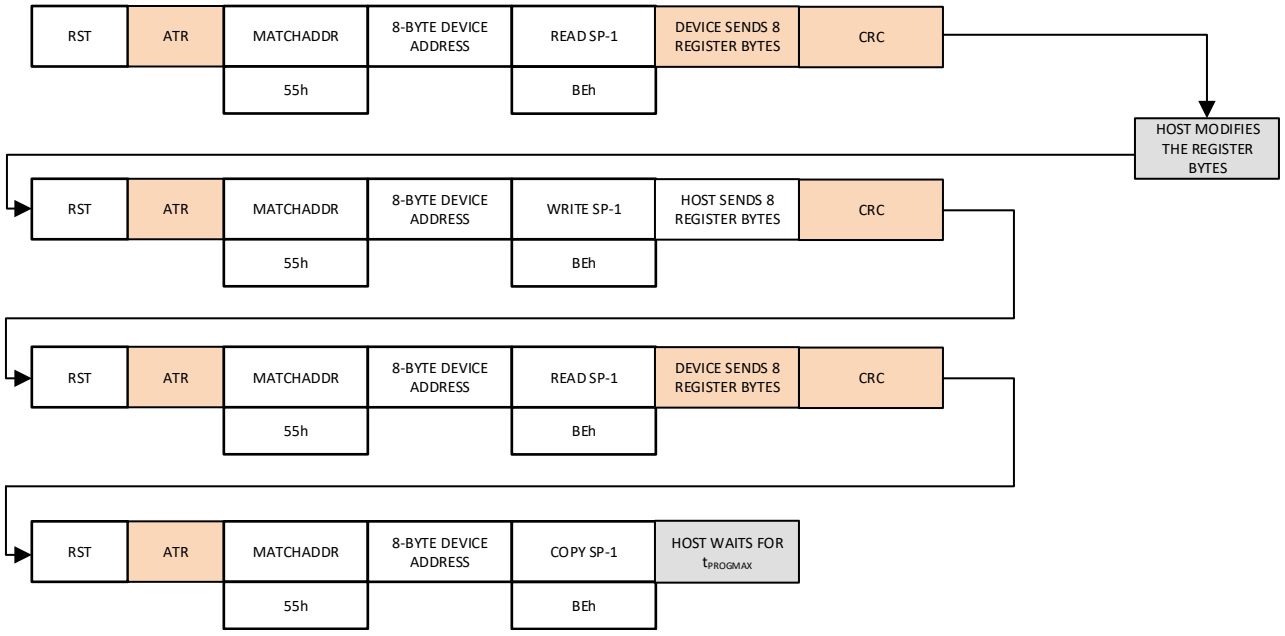


Figure 8-27. Register Scratchpad Update and Commit Programming Flow

8.5.4 Single Device EEPROM Programming and Verify

Figure 8-28 shows the correct procedure the host must execute to update the EEPROM. When communicating with a single device, the host may use the SKIPADDR command. However when communicating with multiple devices, the host must use the MATCHADDR command or the FLEXADDR command to address the correct device. The host writes to the EEPROM scratchpad first, then reads it back to verify the content before it commits the same to the user EEPROM. Once verified the copy command is issued with the qualifier byte A5h and the bus is held idle for the duration of erase and program of the EEPROM. The host shall repeat the sequence for every 8 byte page. After the locations are programmed, the host may issue an READ EEPROM function with the start address to read all the bytes. The device shall read back the bytes in page size and put a CRC byte after every page to ensure that the host shall be able to identify bit corruption using the CRC over a smaller data packet.

As long as the host continues the read operation, the device shall read back 8 bytes of data followed by a CRC byte. When the device reaches the end of the EEPROM block, the device shall return all 1's to the host.

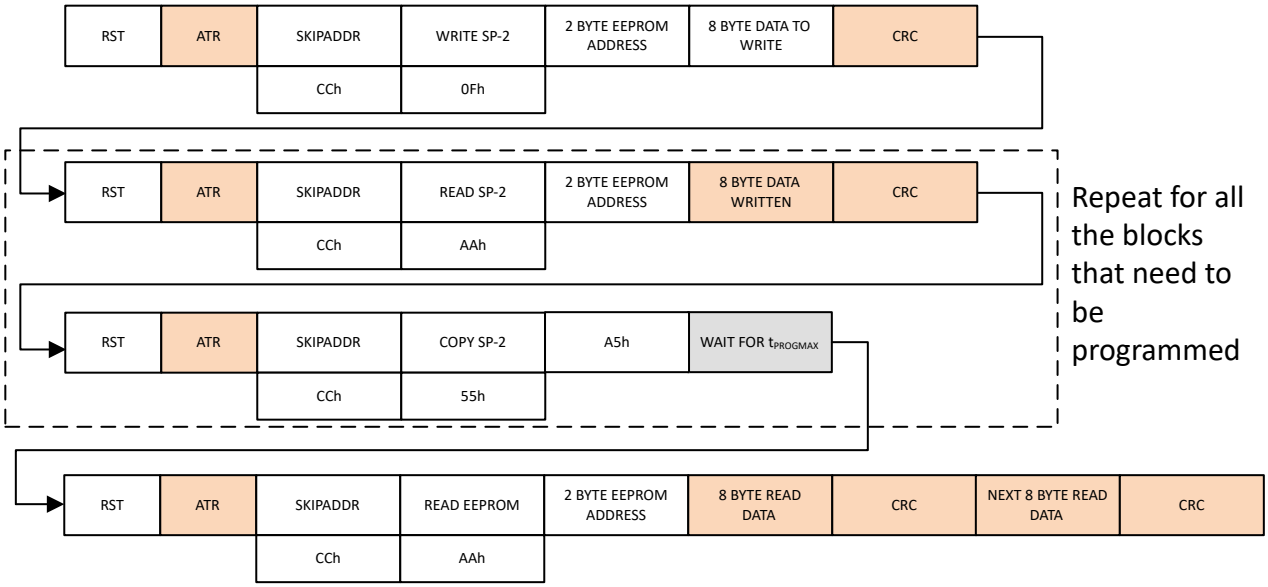


Figure 8-28. Single Device EEPROM Programming and Verify Flow

8.5.5 Single Device EEPROM Lock Operation

When the device EEPROM is successfully programmed as shown in Figure 8-28, the host shall execute the sequence, as shown in Figure 8-29, to write-protect the EEPROM block.

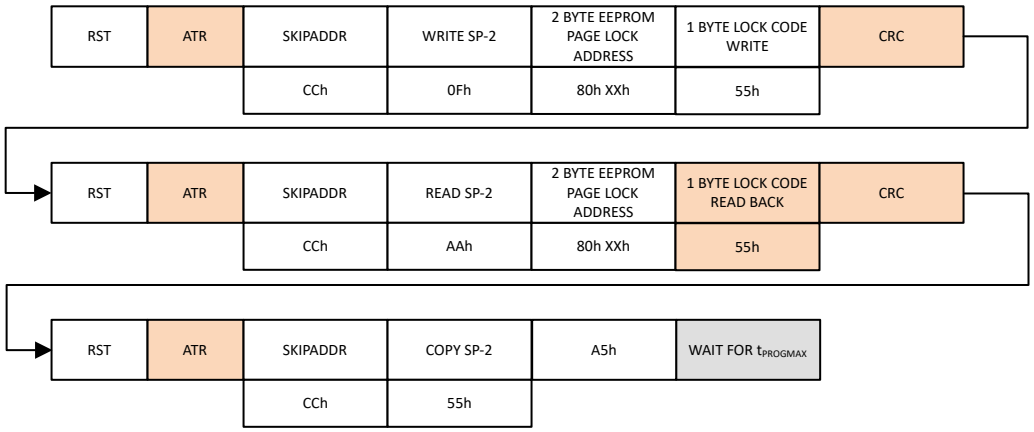


Figure 8-29. Single Device EEPROM Lock Operation Flow

8.5.6 Multiple Device IO Read

Figure 8-30 shows the program flow that the host MCU must execute for reading the IO from a device. The host selects the device it wants to communicate with and issues the GPIO READ function. The host must wait for the time it takes for the device to sample the IO, by keeping the bus idle, before the device returns the IO read register value along with the CRC for the byte. The device at this point shall again sample the IOs. If the host issues a bus reset during the sampling time, the device shall terminate the update process and it will hold the last sampled value. If the host continues, then the new sampled values shall be sent back by the device.

ADVANCE INFORMATION

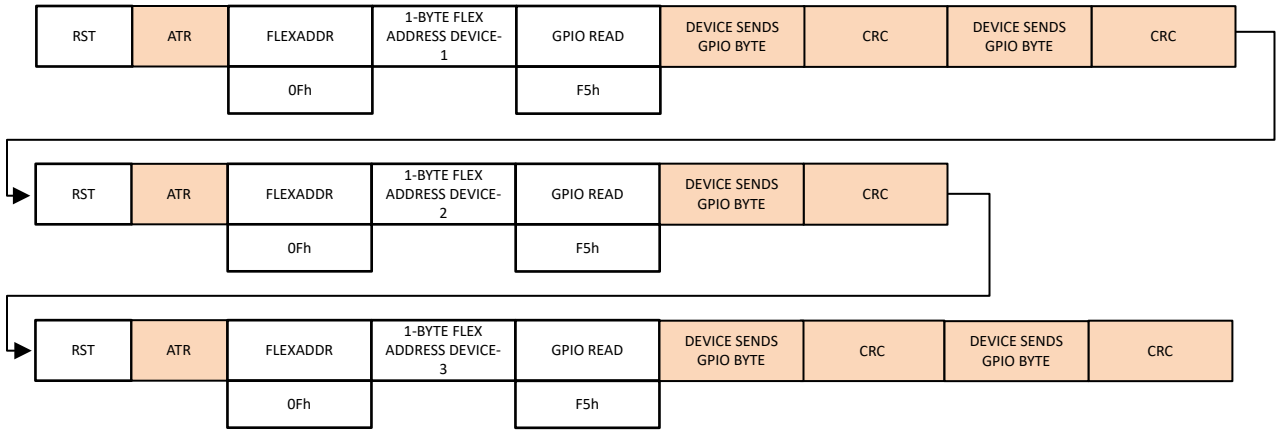


Figure 8-30. Multiple Device GPIO Read Flow

8.5.7 Multiple Device IO Write and Read

Figure 8-31 shows the program flow that the host MCU must execute for configuring the and reading the IO from a device. The host selects the device it wants to communicate with and issues the GPIO WRITE function. The host shall then send the IO configuration register followed by an inverted value, that allows the device to check for any bus transmission error. If the host receives a return code any other than AAh, it must terminate the transaction by sending a bus reset. When the host gets the return code of AAh from the device, it shall wait for the device to sample the bus and then read back the IO read register along with a CRC. If the host plans to read the device continuously, then it must send a bus reset and initiate a GPIO READ function.

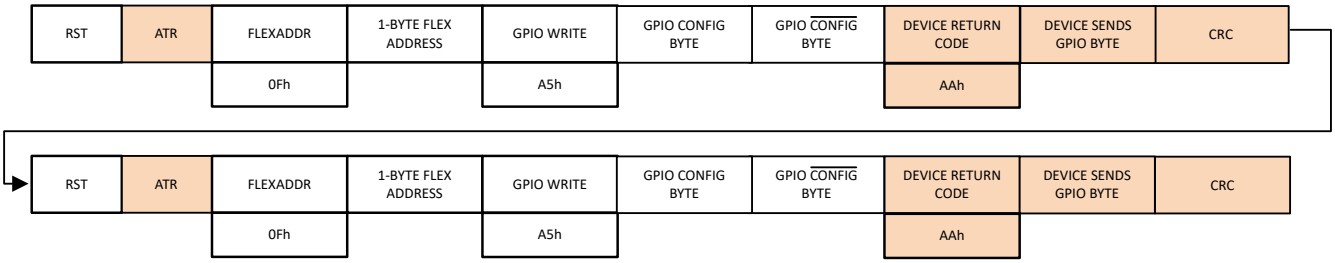


Figure 8-31. Multiple Device GPIO Write and Read Flow

ADVANCE INFORMATION

8.6 Register Maps

Table 8-5. Register Map

SCRATCHPAD-1 BYTE	TYPE	RESET	REGISTER NAME	REGISTER DESCRIPTION	SECTION
00h	RO	00h	TEMP_RESULT_L	Temperature result LSB register	Go
01h	RO	00h	TEMP_RESULT_H	Temperature result MSB register	Go
02h	RO	3xh	STATUS_REG	Status register	Go
03h	RO	FFh	Reserved	Reserved	
04h	R/W	70h	CONFIG_REG1	Device Configuration-1 register	Go
05h	R/W	80h	CONFIG_REG2	Device Configuration-2 register	Go
06h	R/W	00h	SHORT_ADDR	Short address register	Go
07h	RO	FFh	Reserved	Reserved	
08h	R/W	00h	TEMP_ALERT_LOW_L	Temperature alert low limit LSB	Go
09h	R/W	00h	TEMP_ALERT_LOW_H	Temperature alert low limit MSB	Go
0Ah	R/W	F0h	TEMP_ALERT_HIGH_L	Temperature alert high limit LSB	Go
0Bh	R/W	07h	TEMP_ALERT_HIGH_H	Temperature alert high limit MSB	Go
0Ch	R/W	00h	TEMP_OFFSET_L	Temperature offset calibration LSB register	Go
0Dh	R/W	00h	TEMP_OFFSET_H	Temperature offset calibration MSB register	Go
0Eh	RO	FFh	Reserved	Reserved	
0Fh	RO	FFh	Reserved	Reserved	
—	RO	F0h	IO_READ	IO read register	Go
—	RW	00h	IO_CONFIG	IO configuration register	Go

Table 8-6. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

ADVANCE INFORMATION

8.6.1 Temperature Result LSB Register (Scratchpad-1 offset = 00h) [reset = 00h]

The register is part of the 16-bit temperature result readout that stores the least significant byte of the output of the most recent conversion. Following a power up, the register has the value 00h until the first conversion is complete.

Return to Register Map.

Figure 8-32. Temperature Result LSB Register

7	6	5	4	3	2	1	0
TEMP_RESULT[7:0]							
R-00h							

Table 8-7. Temperature Result LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_RESULT[7:0]	R	00h	Stores the LSB of the most recent temperature conversion results.

8.6.2 Temperature Result MSB Register (Scratchpad-1 offset = 01h) [reset = 00h]

The register is part of the 16-bit temperature result readout that stores the most significant byte of the output of the most recent conversion. Following a power up, the register has the value 00h until the first conversion is complete.

Return to Register Map.

Figure 8-33. Temperature Result MSB Register

7	6	5	4	3	2	1	0
TEMP_RESULT[15:8]							
R-00h							

Table 8-8. Temperature Result MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_RESULT[15:8]	R	00h	Stores the MSB of the most recent temperature conversion results.

8.6.3 Status Register (Scratchpad-1 offset = 02h) [reset = 3Ch]

This register provides status of the alert flags, data ready, power mode, arbitration completion, and device lock. The lock flag is set after the device configuration EEPROM is locked by the application. The arbitration done flag is set after the device successfully sends its device address and is cleared only when the ARB_MODE bits in the configuration register are cleared. The power mode status flag value is decided based on the powering technique used for the device detected at power up.

The alert flags are set after the most recent conversion results are available and cleared when the status register is read by the host application. If the alert flag is set, it cannot be cleared by the device even if the result of the last conversion is between the alert limits.

The data ready flag is set after a conversion is completed. It is automatically cleared when the host controller reads the status register.

Return to Register Map.

Figure 8-34. Status Register

7	6	5	4	3	2	1	0
ALERT_HIGH	ALERT_LOW	Reserved		DATA_READY	POWER_MODE	ARB_DONE	LOCK_STATUS
RC-0b	RC-0b	R-11b		R-0b	R-xb	R-0b	R-0b

Table 8-9. Status Register Field Description

Bit	Field	Type	Reset	Description
7	ALERT_HIGH	RC	0b	Alert high status flag 0b = Last temperature conversion result is less than alert high limit 1b = Last temperature conversion result is more than or equal to alert high limit Alert high status flag is available on the IO2 pin when the pin is configured for alert function
6	ALERT_LOW	RC	0b	Alert low status flag 0b = Last temperature conversion result is more than alert low limit 1b = Last temperature conversion result is less than or equal to alert low limit Alert low status flag is available on the IO2 pin when the pin is configured for alert function
5:4	Reserved	R	11b	Reserved
3	DATA_READY	R	0b	Data ready status flag 0b = No update in temperature result register 1b = Temperature result register updated after conversion The data ready flag is automatically cleared when the host controller reads the status register
2	POWER_MODE	R	xb	Device power mode flag. 0b = V_{DD} powered mode 1b = Bus powered mode
1	ARB_DONE	R	0b	Arbitration complete flag 0b = Arbitration is not complete or not enabled 1b = Arbitration is complete
0	LOCK_STATUS	R	0b	Lock status flag. 0b = Device configuration registers can be updated 1b = Device configuration registers cannot be updated

ADVANCE INFORMATION

8.6.4 Device Configuration-1 Register (Scratchpad-1 offset = 04h) [reset = 70h]

The register is used to configure the device functions like the number of valid bits in temperature readout, alert mode, averaging, and conversion type (one-shot, auto and stacked conversion in bus powered mode and one-shot or continuous conversion in V_{DD} powered mode). The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 8-35. Device Configuration-1 Register

7	6	5	4	3	2	1	0
TEMP_FMT	Reserved	CONV_TIME_SEL	ALERT_MODE	AVG_SEL	CONV_MODE_SEL[2:0]		
RW-0b	RW-1b	RW-1b	RW-1b	RW-0b	RW-000b		

Table 8-10. Device Configuration-1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TEMP_FMT	RW	0b	Selects the temperature format. 0b = 12-bit legacy format 1b = 16-bit high precision format
6	Reserved	RW	1b	Reserved
5	CONV_TIME_SEL	RW	1b	Selects the ADC conversion time 0b = 3 ms / 1b = 5.5 ms
4	ALERT_MODE	RW	1b	Alert pin function only available in V_{DD} powered mode 0b = Alert pin works in Alert Mode 1b = Alert pin works in Comparator Mode
3	AVG_SEL	RW	0b	Conversion averaging selection 0b = No averaging 1b = Averaging of 8 conversions
2:0	CONV_MODE_SEL[2:0]	RW	000b	Conversion mode selection bits. When device is in bus powered mode: 000b = Default one shot conversion mode using CONVERT TEMP function 001b = Stacked conversion mode is enabled. When enabled, the short address is used to stagger the actual conversion start with respect to the conversion request. 010b = Auto temperature conversion mode is enabled 011b - 111b = Reserved. Device behavior is unspecified. When device is in V_{DD} powered mode: 000b = Default one shot conversion mode using CONVERT TEMP function 001b = One conversion every 8 seconds 010b = One conversion every 4 seconds 011b = One conversion every 2 seconds 100b = One conversion every 1 second 101b = One conversion every 0.5 second 110b = One conversion every 0.25 second 111b = One conversion every 0.125 second

ADVANCE INFORMATION

8.6.5 Device Configuration-2 Register (Scratchpad-1 offset = 05h) [reset = 80h]

This register is used to configure the overdrive enable, flexible address mode, arbitration mode during address discovery, and the hysteresis for alert status or pin (available only in V_{DD} powered mode for alert pin). The register can be used to lock the writable registers for the device. All register bits except FLEX_ADDR_MODE can be stored in the configuration EEPROM using the COPY SCRATCHPAD-1 function command and restored at power-on reset.

Note

1. When setting the overdrive enable or lock enable bits, the application must send all the scratchpad-1 data bytes and read the CRC from the device before the change of overdrive bit takes effect.
2. When FLEX_ADDR_MODE is selected to decode resistor or IO, the bus must be put in idle state after the device configuration-2 register byte is transmitted for t_{RESDET}.

Return to Register Map.

Figure 8-36. Device Configuration-2 Register

7	6	5	4	3	2	1	0
OD_EN	FLEX_ADDR_MODE[1:0]		ARB_MODE[1:0]		HYSTERSIS[1:0]		LOCK_EN
RO-1b	RW-00b		RW-00b		RW-00b		RW-0b

Table 8-11. Device Configuration-2 Register Field Description

Bit	Field	Type	Reset	Description
7	OD_EN	RO	1b	Overdrive mode enable 0b = Overdrive speed is disabled 1b = Overdrive speed is enabled The bit when set cannot be cleared by host write and will automatically be cleared only by a standard speed reset signal. See Note-1 above.
6:5	FLEX_ADDR_MODE[1:0]	RW	00b	Flexible address mode selection. 00b = Short address register is updated by host 01b = Short address register is updated by IO pin decode 10b = Short address register is updated by Resistor decode 11b = Short address register is updated by combined IO and resistor address decode Flexible address mode selection takes effect only when there is a change detected in the bit setting.
4:3	ARB_MODE[1:0]	RW	00b	Arbitration mode 00b = Arbitration by device is disabled 01b = Reserved 10bh = Arbitration by device is enabled in software compatible mode 11b = Fast Arbitration mode is enabled The arbitration feature is applicable only when address command is SEARCHADDR. Other commands and functions are not affected by the ARB_MODE bit.
2:1	HYSTERSIS[1:0]	RW	00b	Alert hysteresis selection 00b = 5 °C hysteresis 01b = 10 °C hysteresis 10b = 15 °C hysteresis 11b = 20 °C hysteresis

ADVANCE INFORMATION

Table 8-11. Device Configuration-2 Register Field Description (continued)

Bit	Field	Type	Reset	Description
0	LOCK_EN	RW	0b	Register lock protection enable/disable bit 0b = The register protection is disabled 1b = The register protection is enabled. When set the bit cannot be cleared by writing to the register to unlock the register protection. The feature when enabled, prevents application write to the temperature offset, temperature alert low, temperature alert high, short address and device configuration registers. See Note-1 above.

8.6.6 Short Address Register (Scratchpad-1 offset = 06h) [reset = 00h]

The register is used to program the short address for the device. The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM. As described in Flexible Device Address, the specific short address decoded value is overlaid on the non-volatile memory content restored to the short address register.

The short address register can only be updated by the application when the FLEX_ADDR_MODE bits have the value '00b'. Any write to register when the FLEX_ADDR_MODE bits are not '00b' shall be ignored by the device.

Return to Register Map.

Figure 8-37. Short Address Register

7	6	5	4	3	2	1	0
SHORT_ADDRESS[7:0]							
RW-00h							

Table 8-12. Short Address Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SHORT_ADDRESS[7:0]	RW	00h	Stores the short address for the device which may be used to access the device without sending the 64-bit Unique Device Address. When FLEX_ADDR_MODE[1:0] = 0h, the 8-bit value of the register is used as is. When FLEX_ADDR_MODE[1:0] = 1h or 2h, the upper 4-bit of the register is updated from the value committed to the non-volatile memory, while the lower 4-bit are decoded based on IO0-IO3 connection on the board or address decoding based on the resistor connected to ADDR pin, respectively. When FLEX_ADDR_MODE[1:0] = 3h, the upper 2-bit of the register is updated from the value committed to the non volatile memory, the next 2-bit are decoded from IO1 and IO0, and the last 4-bit is decoded from the resistor connected to ADDR pin. The short address is also used during stacked conversion mode to stagger the active conversion.

ADVANCE INFORMATION

8.6.7 Temperature Alert Low LSB Register (Scratchpad-1 offset = 08h) [reset = 00h]

This register provides the LSB for the low temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is less than the threshold set, then the device shall update the alert low status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 8-38. Temperature Alert Low Register

7	6	5	4	3	2	1	0
ALERT_LOW[7:0]							
RW-00h							

Table 8-13. Temperature Alert Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ALERT_LOW[7:0]	RW	00h	Stores the LSB of the alert low limit for comparison with the last temperature conversion result

8.6.8 Temperature Alert Low MSB Register (Scratchpad-1 offset = 09h) [reset = 00h]

This register provides the MSB for the low temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is less than the threshold set, then the device shall update the alert low status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Table 8-14.

7	6	5	4	3	2	1	0
ALERT_LOW[15:8]							
RW-00h							

Table 8-15.

Bit	Field	Type	Reset	Description
7:0	ALERT_LOW[15:8]	RW	00h	Stores the MSB of the alert low limit for comparison with the last temperature conversion result

8.6.9 Temperature Alert High LSB Register (Scratchpad-1 offset = 0Ah) [reset = F0h]

This register provides the LSB for the high temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is more than the threshold set, then the device shall update the alert high status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 8-39. Temperature Alert High Register

7	6	5	4	3	2	1	0
ALERT_HIGH[7:0]							
RW-F0h							

Table 8-16. Temperature Alert High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ALERT_HIGH[7:0]	RW	F0h	Stores the LSB of the alert high limit for comparison with the last temperature conversion result

8.6.10 Temperature Alert High MSB Register (Scratchpad-1 offset = 0Bh) [reset = 07h]

This register provides the MSB for the high temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is more than the threshold set, then the device shall update the alert high status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 8-40. Temperature Alert High MSB Register

7	6	5	4	3	2	1	0
ALERT_HIGH[15:8]							
RW-07h							

Table 8-17. Temperature Alert High MSB Register Field Description

Bit	Field	Type	Reset	Description
7:0	ALERT_HIGH[15:8]	RW	07h	Stores the MSB of the alert high limit for comparison with the last temperature conversion result

ADVANCE INFORMATION

8.6.11 Temperature Offset LSB Register (Scratchpad-1 offset = 0Ch) [reset = 00h]

The register is used to store the LSB of the offset calibration for the temperature sensor. The register on the first power up has the temperature offset set in legacy format. If there is a change of format, then the application must update the register in the new format. After every temperature conversion, the offset calibration is automatically applied to the temperature result, before being stored in the TEMP_RESULT_L and TEMP_RESULT_H registers.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 8-41. Temperature Offset LSB Register

7	6	5	4	3	2	1	0
TEMP_OFFSET_L[7:0]							
RW-00h							

Table 8-18. Temperature Offset LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_OFFSET_L[7:0]	RW	00h	Stores the offset correction LSB for the temperature result

8.6.12 Temperature Offset MSB Register (Scratchpad-1 offset = 0Dh) [reset = 00h]

The register is used to store the MSB of the offset calibration for the temperature sensor. The register on the first power up has the temperature offset set in legacy format. If there is a change of format, then the application must update the register in the new format. After every temperature conversion, the offset calibration is automatically applied to the temperature result, before being stored in the TEMP_RESULT_L and TEMP_RESULT_H registers.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 8-42. Temperature Offset MSB Register

7	6	5	4	3	2	1	0
TEMP_OFFSET_H[15:8]							
RW-00h							

Table 8-19. Temperature Offset MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_OFFSET_H[15:8]	RW	00h	Stores the offset correction MSB for the temperature result

8.6.13 IO Read Register [reset = F0h]

The register is used to read the state of the IO0 to IO3 pin. The register values are updated when the GPIO READ function is issued by the host or when the GPIO configuration is written using the GPIO WRITE function. When IO2 is configured to function as an alert pin, it provides a status of the alert pin.

Return to Register Map.

Figure 8-43. IO Read Register

7	6	5	4	3	2	1	0
nIO3_STATE	nIO2_STATE	nIO1_STATE	nIO0_STATE	IO3_STATE	IO2_STATE	IO1_STATE	IO0_STATE
R-1b	R-1b	R-1b	R-1b	R-0b	R-0b	R-0b	R-0b

Table 8-20. IO Read Register Field Descriptions

Bit	Field	Type	Reset	Description
7	nIO3_STATE	R	1b	Read inverted value of the IO3 pin when configured as a digital input or output
6	nIO2_STATE	R	1b	Read inverted value of the IO2 pin when configured as a digital input or output
5	nIO1_STATE	R	1b	Read inverted value of the IO1 pin when configured as a digital input or output
4	nIO0_STATE	R	1b	Read inverted value of the IO0 pin when configured as a digital input or output
3	IO3_STATE	R	0b	Read value of the IO3 pin when configured as a digital input or output
2	IO2_STATE	R	0b	Read value of the IO2 pin when configured as a digital input or output
1	IO1_STATE	R	0b	Read value of the IO1 pin when configured as a digital input or output
0	IO0_STATE	R	0b	Read value of the IO0 pin when configured as a digital input or output

8.6.14 IO Configuration Register [reset = 00h]

The register is used to select the IO function for the pins marked IO0-IO3 on the device. When selected to function as a digital open-drain output, the pin shall be able to drive a 0 or 1 externally for controlling the gate or base of a transistor on IO0 to IO3 pin. In bus powered mode, IOs tied to SDQ and used for short address must not be configured as output as this may cause the SDQ line to be driven low.

Return to Register Map.

Figure 8-44. IO Configuration Register

7	6	5	4	3	2	1	0
IO3_SEL[1:0]		IO2_SEL[1:0]		IO1_SEL[1:0]		IO0_SEL[1:0]	
RW-00b		RW-00b		RW-00b		RW-00b	

Table 8-21. IO Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	IO3_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO3 is configured as input buffer and can be read 01b = Reserved 10b = IO3 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO3 is configured as an output in open drain mode and the IO is driven as '1'

ADVANCE INFORMATION

Table 8-21. IO Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	IO2_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO2 is configured as input buffer and can be read 01b = IO2 is configured as an open drain active low alert 10b = IO2 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO2 is configured as an output in open drain mode and the IO is driven as '1'
3:2	IO1_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO1 is configured as input buffer and can be read 01b = Reserved 10b = IO1 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO1 is configured as an output in open drain mode and the IO is driven as '1'
1:0	IO0_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO0 is configured as input buffer and can be read 01b = Reserved 10b = IO0 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO0 is configured as an output in open drain mode and the IO is driven as '1'

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMP1827 can operate as a single-wire half duplex bus, either in supply or bus powered mode. The TMP1827 features a thermal sensor with an integrated 2-kbit user EEPROM and SHA-256-HMAC authentication for applications requiring identification with lesser number of components due to space constraints. The device also features an integrated CRC that may be used for ensuring data integrity during communication.

The bus powered mode is designed for applications working without a dedicated power supply pin and can reduce cabling costs. As the device current consumption during thermal conversion and EEPROM operations is low, the device may not require a low impedance current path, thereby reducing the need for additional FET or load switch and current limiting resistor to bypass the bus pullup resistor. The pullup resistor used during bus powered mode must be correctly sized to ensure that sufficient current can be supplied during a thermal conversion and EEPROM operation, and input pin voltage does not fall below the $V_{IH(MIN)}$.

Additionally, if the host needs to reset the device when operating in bus powered mode, the host must pull the communication line low for at least 100 ms. This allows the internal capacitor of the device to discharge and prepare the device for power on reset.

9.2 Typical Applications

9.2.1 Bus Powered Application

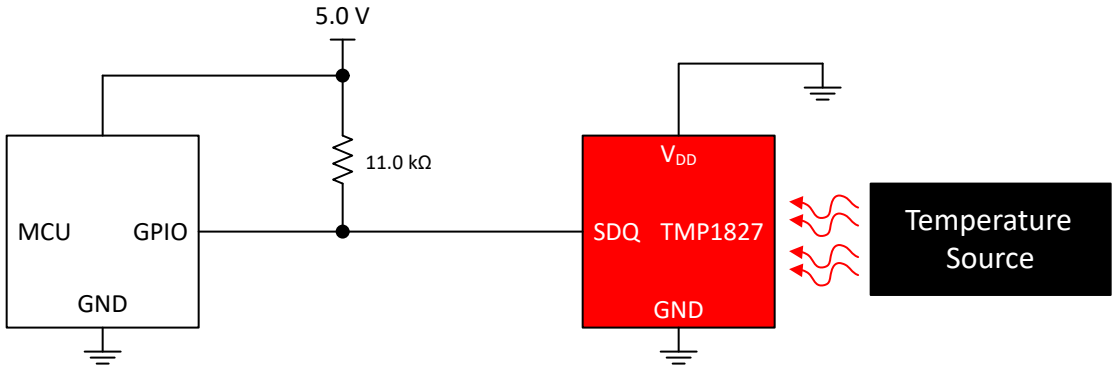


Figure 9-1. Bus Powered Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed below:

Table 9-1. Design Parameters

PARAMETER	VALUE
Power mode	Bus Powered
Supply (V_{DD})	5.0 V
Pullup resistor range (R_{PUR})	1.2 kΩ to 11.0 kΩ

ADVANCE INFORMATION

9.2.1.2 Detailed Design Procedure

To reduce the wire count, the bus powered mode for TMP1827 is the primary mode of operation. The V_{DD} pin of the device must be connected to GND and the SDQ pin of the device must be connected to the host GPIO with a pullup resistor.

To calculate the pullup resistor range, substitute the value for V_{PUR}, $V_{OL(MAX)}$ and $I_{PU(MIN)}$ in Equation 1.

$$\frac{(5.0\ -\ 0.4)}{4\ \times\ 10^{-3}} < R_{PUR} < \frac{(5.0\ -\ 1.6)}{300 \times 10^{-6}} \quad (2)$$

$$1.15\ k\Omega\ < R_{PUR} < 11.333\ k\Omega \quad (3)$$

The actual value of the pullup resistor can then be adjusted based on the speed of communication and bus or cable parasitic capacitance.

When the V_{DD} is activated, the TMP1827 draws current through the pullup resistor to charge its internal capacitors. When the internal capacitor is charged to the pullup voltage, the host can start communication. The bus idle state is high, which is maintained by the pullup resistor, when the host puts its GPIO in high impedance state.

The TMP1827 uses the stored charge to operate when the SDQ pin is low and measures the low period to decode bus reset, logic high and logic low sent by the host. Similarly, when the host reads data from the TMP1827, it changes the state of the bus from high to low and releases the bus. Depending on whether the device has to send a logic low or logic high, the device shall either hold the bus low or release the bus immediately.

9.2.2 Supply Powered Application

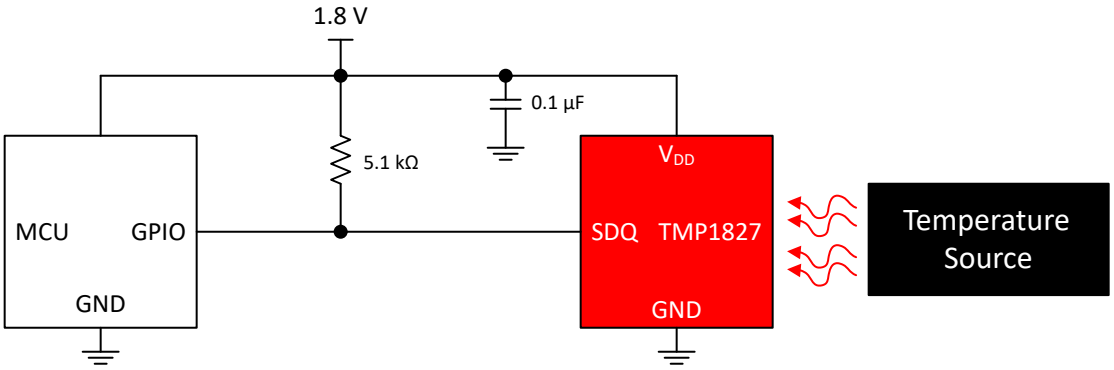


Figure 9-2. Supply Powered Application

9.2.2.1 Design Requirements

For this design example, use the parameters listed below:

Table 9-2. Design Parameters

PARAMETER	VALUE
Power mode	V_{DD} Powered
Supply (V_{DD})	1.8 V
Pullup resistor (R_{PUR})	5.1 kΩ

9.2.2.2 Detailed Design Procedure

The supply powered mode uses the V_{DD} pin connected to the same supply rail as the host and pullup resistor. TI recommends to put a 0.1-µF bypass capacitor close to the V_{DD} pin of the TMP1827.

ADVANCE INFORMATION

The pullup resistor value of 5.1 kΩ, is large enough to provide proper communication with standard speed and avoid V_{OL} violation when the device is sending data to the host. The user may change the value based on the total bus load and application operating requirements.

The communication protocol for supply powered mode is same as that for bus powered mode, which allows the entire software stack to be reused. This mode of operation is useful for onboard thermal sensing applications as it provides for continuous conversion and alert function.

9.2.3 UART Interface for Communication

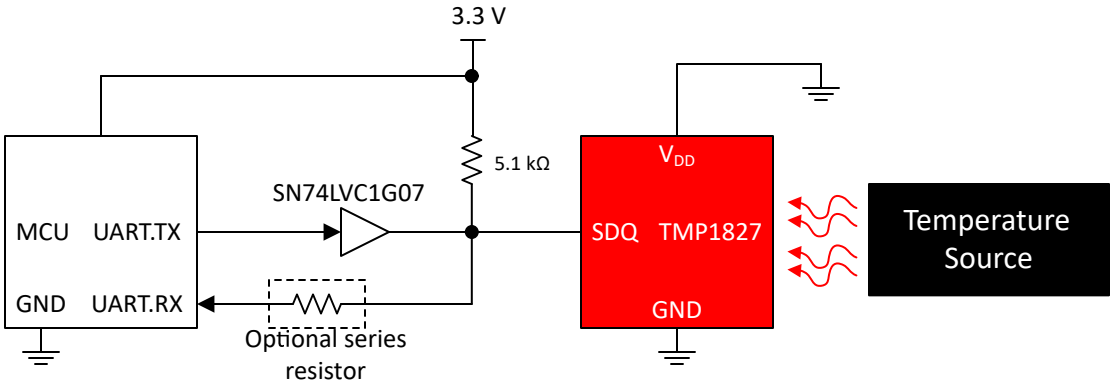


Figure 9-3. Using UART to interface TMP1827

9.2.3.1 Design Requirements

For this design example, use the parameters listed below:

Table 9-3. Design Parameters

PARAMETER	VALUE
Power Mode	Bus powered
Supply (V_{DD})	3.3 V
Pullup resistor range (R_{PUR})	750 Ω to 5.1 kΩ

9.2.3.2 Detailed Design Procedure

If using GPIO for communication is not possible due to any reason, it is also possible to use UART peripheral that is available on most host controllers to interface with the TMP1827. UART is a push-pull full duplex bus and to interface with TMP1827, it requires a buffer with open-drain driver like the SN74LVC1G07.

The input of the buffer is connected to the UART transmit pin and the output of the buffer is connected to the SDQ pin on the TMP1827. The output of the buffer is also connected to the UART receive pin on the host. As the output is open-drain, it requires a pullup resistor which can be calculated in Equation 1. Substituting the value for V_{PUR} = 3.3 V, $V_{OL(MAX)}$ = 0.4 V and $I_{PU(MIN)}$ = 300 µA, the R_{PUR} value selected must be greater than 725 Ω and less than 5.67 kΩ.

In software, the application must adjust its baud rate so that it can send bus reset to the device by sending 00h. The start bit of the UART frame which is always 0, provides the required falling edge for data sent to the TMP1827. When sending a logic high to the device, the UART shall send FFh to the TMP1827 and, when sending a logic low to the device, the UART shall send C0h. As UART is a full duplex bus, the host must flush its receive buffers during a transmit operation.

When receiving data from the TMP1827, the host shall send FFh and the device when transmitting a logic high will detect and release the bus, while when transmitting a logic low will detect and hold the bus. As a result, the host shall receive a FFh for a logic high and F0h for a logic low depending on the baud rate configured.

ADVANCE INFORMATION

9.3 Power Supply Recommendations

The TMP1827 operates with a power supply in the range of 1.7 V to 5.5 V in both V_{DD} powered and bus powered modes. When operating in V_{DD} powered mode, a power-supply bypass capacitor is required for precision and stability. Place this power-supply bypass capacitor as close to the supply and ground pins of the device as possible. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require a bigger bypass capacitor to reject power-supply noise.

In bus powered mode, the V_{DD} pin must be connected to ground. The internal capacitor in the device is sufficient to provide power during bus communication. The internal capacitor is recharged through the external pullup resistor during the recovery period. In cases, where there is a long bus length or at higher temperatures, it may be necessary for the host to provide additional time for bus recovery or to use the overdrive speed in which the part uses the internal capacitor charge less.

When using IO pins to control external circuits, take care that currents to these pins do not heat the part and offset temperature measurements.

9.4 Layout

9.4.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins when in supply powered mode. The recommended value of the capacitor is 0.1 µF. The open-drain SDQ pin requires an external pullup resistor which must not be higher than R_{PUR}.

When in bus powered mode, only the external pullup resistor is required for the open-drain SDQ pin.

To achieve a high precision temperature reading for a rigid PCB, do not solder the thermal pad. For a flexible PCB, the user may solder the thermal pad to the increase board level reliability. If the thermal pad is soldered, then it should be connected to the ground.

9.4.2 Layout Example

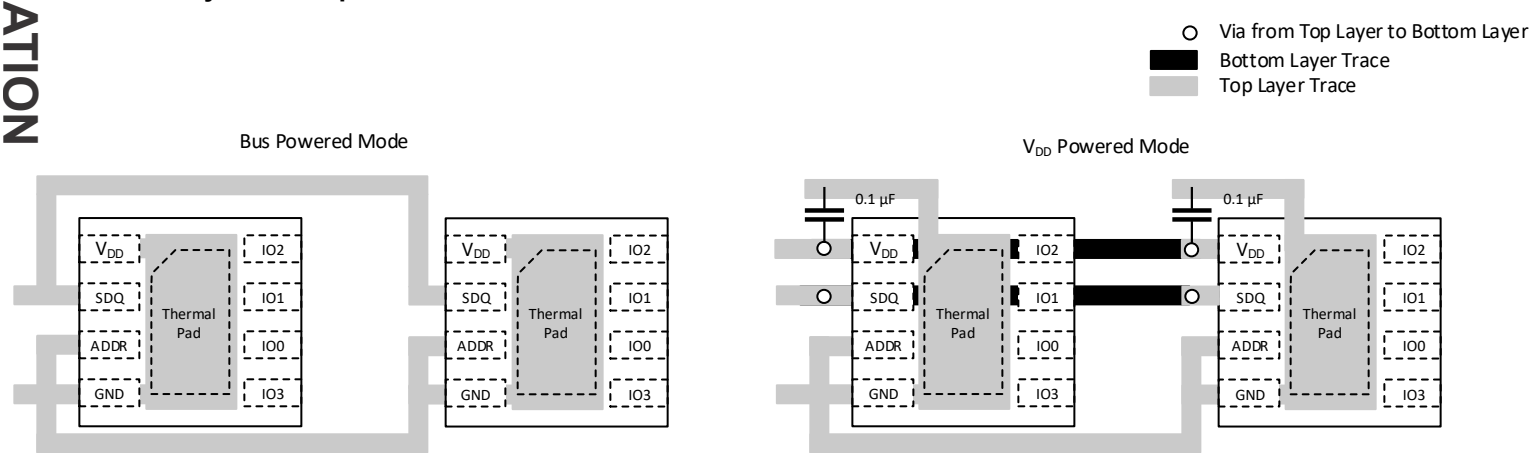


Figure 9-4. Layout Example

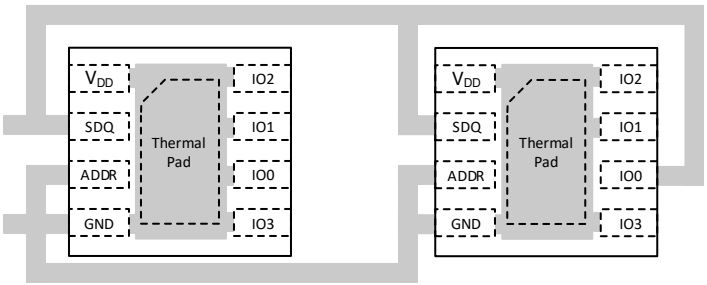


Figure 9-5. IO Hardware Address in Bus Powered Mode

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- TMP1827 EVM User's Guide (SBOU294)
- TMP1827 Security Programming Guide (SBOU270)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

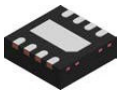
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

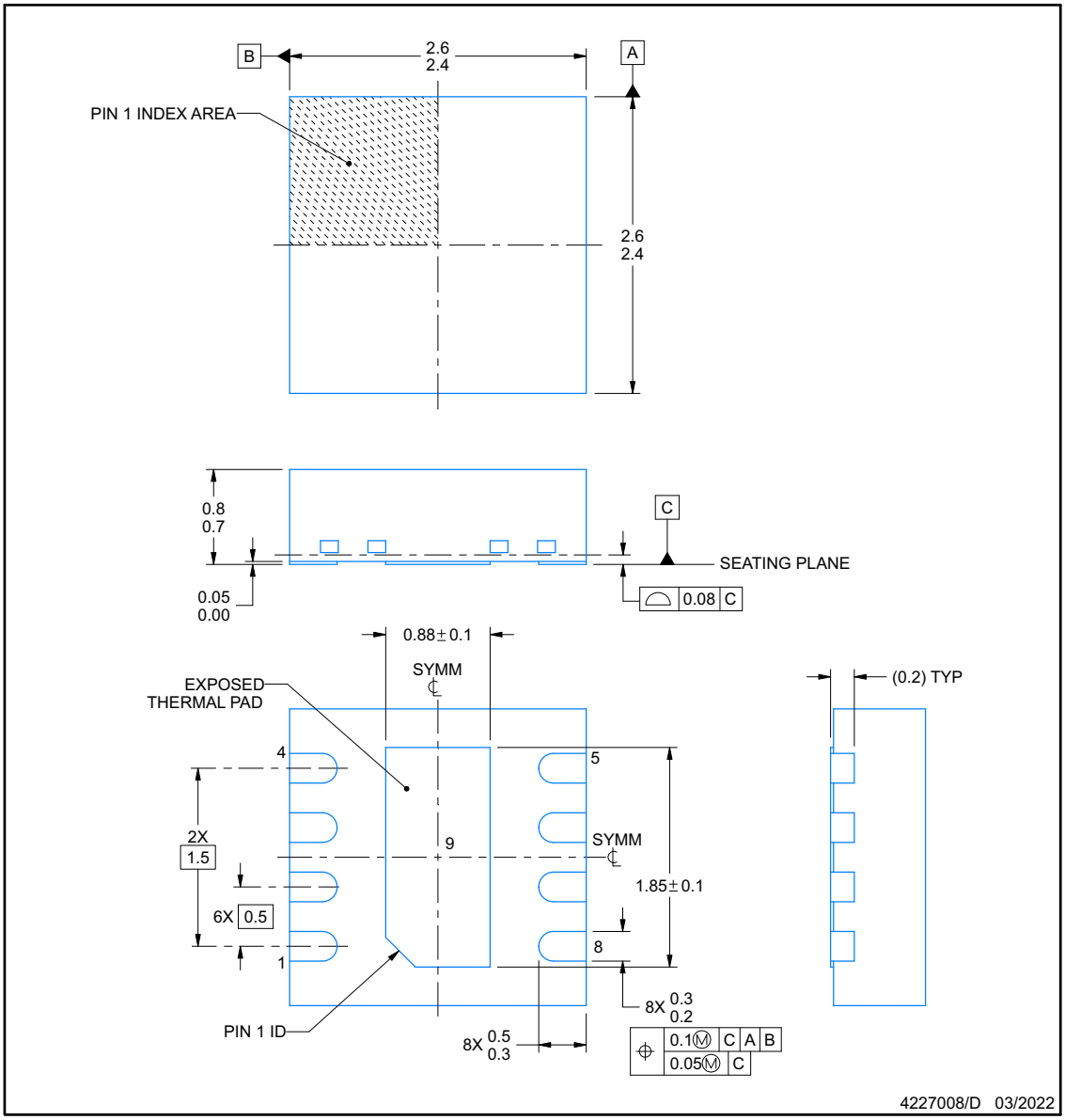
PACKAGE OUTLINE

NGR0008C



WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

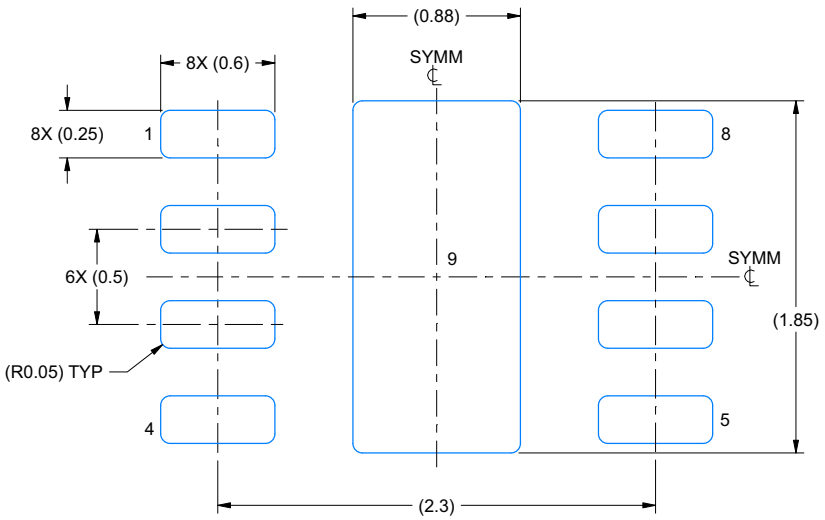
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

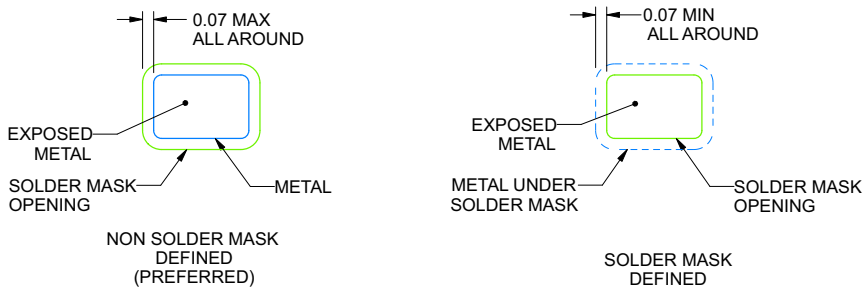
NGR0008C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4227008/D 03/2022

NOTES: (continued)

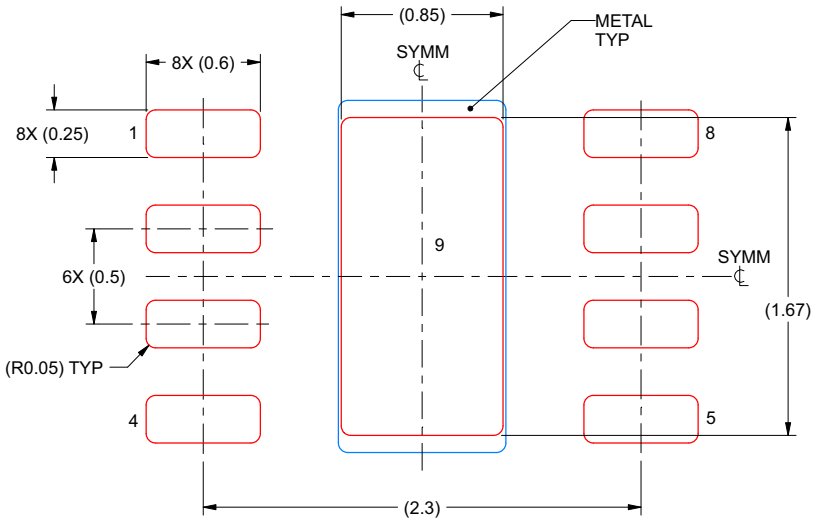
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

NGR0008C — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4227008/D 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

11.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PTMP1827NGRT	ACTIVE	WSON	NGR	8	250	TBD	Call TI	Call TI	-55 to 150	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

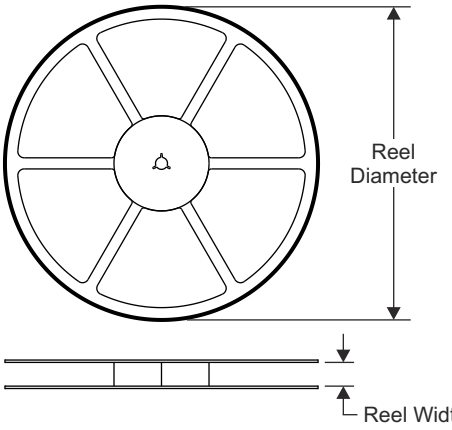
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

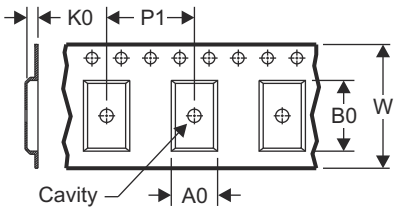
ADVANCE INFORMATION

11.2 Tape and Reel Information

REEL DIMENSIONS

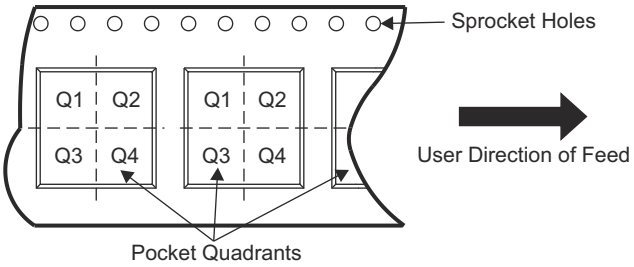


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

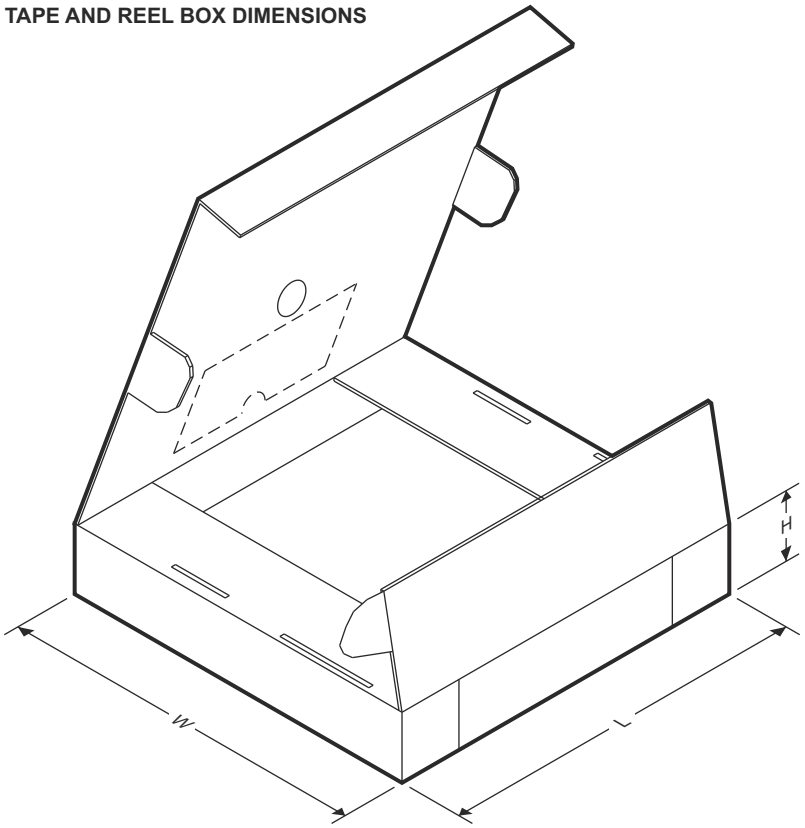
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTMP1827NGRT	WSON	NGR	8	250	178	8.4	2.75	2.75	0.95	4	8	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTMP1827NGRT	WSON	NGR	8	250	205	200	33

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMP1827NGRT	ACTIVE	WSON	NGR	8	250	TBD	Call TI	Call TI	-55 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

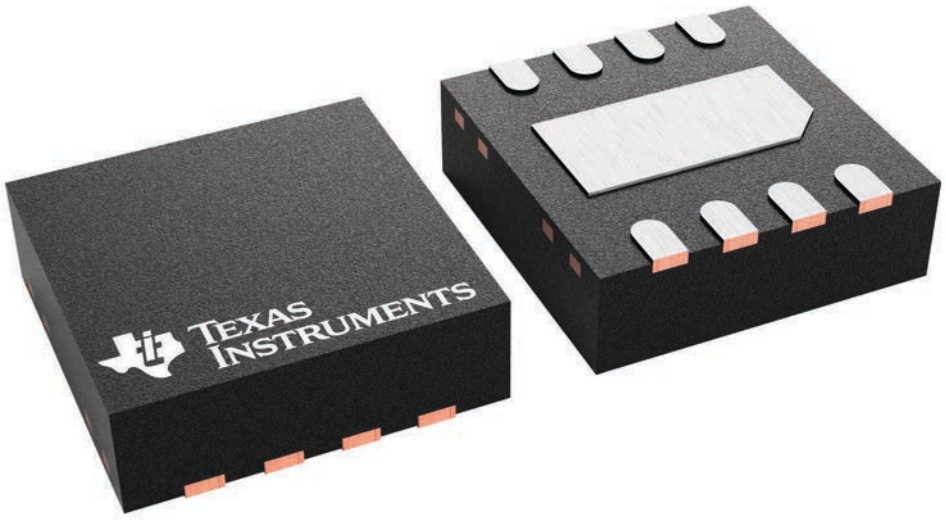
NGR 8

WSON - 0.8 mm max height

2.5 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227146/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265