TMP64-Q1 ±1% 47-kΩ Automotive Grade Linear Thermistor with 0402 and 0603 Package Options

1 Features

- Automotive Qualifications
- Temperature Options:
  - AEC-Q100 Grade 1: –40 °C to 125 °C
  - AEC-Q100 Grade 0 (DYA): –40 °C to 150 °C
- Silicon-based thermistor with a positive temperature coefficient (PTC)
- Linear resistance change across temperature
- 47-kΩ nominal resistance at 25 °C (R25)
  - ±1% maximum (0 °C to 70 °C)
- Consistent sensitivity across temperature
  - 6400 ppm/°C TCR (25 °C)
  - 0.2% typical TCR tolerance across temperature range
- Fast thermal response time of 0.6 s (DEC)
- Long lifetime and robust performance
  - Built-in fail-safe in case of short-circuit failures
  - 0.5% typical long term sensor drift

2 Applications

- Thermal compensation
  - Display backlight
  - Battery management systems
- Thermal threshold detection
  - Motor control
  - On-board chargers & DC-DC converters

3 Description

Get started today with the Thermistor Design Tool, offering complete resistance vs temperature table (R-T table) computation, other helpful methods to derive temperature and example C-code.

Linear thermistors offer linearity and consistent sensitivity across temperature to enable simple and accurate methods for temperature conversion. Low power consumption and a small thermal mass minimize the impact of self-heating. With built-in failsafe behavior at high temperatures and powerful immunity to environmental variation, these devices are designed for a long lifetime of high performance. The small size of the TMP6 series also allows for close placement to heat sources and quick response times.

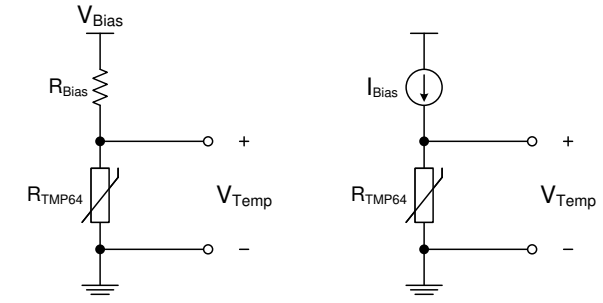
Take advantage of benefits over NTC thermistors such as no extra linearization circuitry, minimized calibration, less resistance tolerance variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory in the processor.

The TMP64-Q1 is currently available in a 0402 footprint-compatible X1SON package and a 0603 footprint-compatible SOT-5X3 package.

Device Information (1)

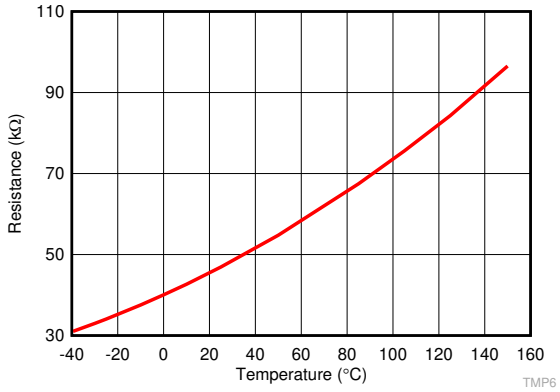
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP64-Q1	X1SON	0.60 mm × 1.00 mm
	SOT-5X3	0.60 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



$$V_{Temp} = \frac{V_{Bias} * R_{TMP64}}{R_{Bias} + R_{TMP64}} \qquad V_{Temp} = I_{Bias} * R_{TMP64}$$

Typical Implementation Circuits



Typical Resistances vs Ambient Temperature

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2020) to Revision B (November 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added AEC-Q100 Temperature Grade 0 rating for SOT-5X3/DYA package	1
• Moved HBM and CDM ESD classification levels to *ESD Ratings* table	1
• Added DYA (SOT-5X3) package	1
• Updated DYA maximum temperature rating to 150 °C in device comparison table	3
• Changed Junction temperature from 150 °C to 155 °C in *Absolute Maximum Ratings* Table	5
• Changed Storage temperature from 150 °C to 155 °C in *Absolute Maximum Ratings* Table	5
• Added DYA Ambient Temperature Rating to *Recommended Operating Conditions* Table	5
• Added DYA Long Term Drift specifications	6
• Changed *Typical Characteristics* section	7
• Added *Application Curve* section	16

Changes from Revision Original (March 2019) to Revision A (June 2020)	Page
• Changed data sheet status from: Advanced Information to: Production Data	1
• Added Device Comparison table	3

5 Device Comparison Table

PART NUMBER	R25 TYP	R25 %TOL	RATING	T_A	PACKAGE OPTIONS
TMP61	10k	1%	Catalog	–40 °C to 125 °C	X1SON / DEC (0402)
				–40 °C to 150 °C	SOT-5X3 / DYA (0603)
					TO-92S / LPG
TMP61-Q1	10k	1%	Automotive Grade-1	–40 °C to 125 °C	X1SON / DEC (0402)
			Automotive Grade-0	-40 °C to 150 °C	SOT-5X3 / DYA (0603)
				–40 °C to 170 °C	TO-92S / LPG
TMP63	100k	1%	Catalog	–40 °C to 125 °C	X1SON / DEC (0402)
				-40 °C to 150 °C	SOT-5X3 / DYA (0603)
TMP63-Q1	100k	1%	Automotive Grade-1	–40 °C to 125 °C	X1SON / DEC (0402)
			Automotive Grade-0	-40 °C to 150 °C	SOT-5X3 / DYA (0603)
TMP64	47k	1%	Catalog	–40 °C to 125 °C	X1SON / DEC (0402)
				-40 °C to 150 °C	SOT-5X3 / DYA (0603)
TMP64-Q1	47k	1%	Automotive Grade-1	–40 °C to 125 °C	X1SON / DEC (0402)
			Automotive Grade-0	-40 °C to 150 °C	SOT-5X3 / DYA (0603)

6 Pin Configuration and Functions

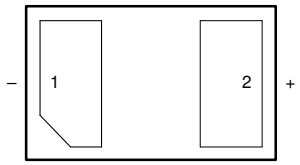


Figure 6-1. DEC Package 2-Pin X1SON Bottom View

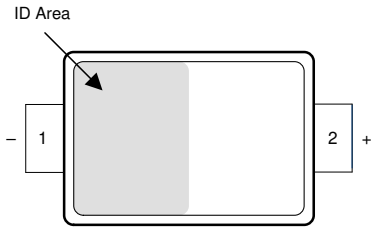


Figure 6-2. DYA Package 2-Pin SOT-5X3 Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
–	1	—	Thermistor (–) and (+) terminals. For proper operation, ensure a positive bias where the + terminal is at a higher voltage potential than the – terminal.
+	2		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage across pins 2 (+) and 1 (–)		6	V
Current through the device		450	µA
Junction temperature (T_J)	–65	155	°C
Storage temperature (T_{stg})	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C6	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{Sns}	Voltage across pins 2 (+) and 1 (–)	0		5.5	V
I_{Sns}	Current passing through the device	0		100	µA
T_A	Operating free-air temperature (X1SON/DEC Package)	–40		125	°C
	Operating free-air temperature (SOT-5X3/DYA Package)	–40		150	°C

7.4 Thermal Information

THERMAL METRIC (1)		TMP64-Q1		Units
		DEC (X1SON)	DYA (SOT-5X3)	
		2 PINS	2 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2) (3)	443.4	749.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	195.7	315.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	254.6	506.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	109.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	254.5	500.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) The junction to ambient thermal resistance ($R\theta_{JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.

(3) Changes in output due to self heating can be computed by multiplying the internal dissipation by the thermal resistance.

7.5 Electrical Characteristics

T_A = -40 °C - 125 °C, I_{Sns} = 42.553 µA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{25}	Thermistor Resistance at 25 °C	T_A = 25 °C	46.53	47	47.47	kΩ
R_{TOL}	Resistance Tolerance	T_A = 25 °C	–1		1	%
		T_A = 0 °C - 70 °C	–1		1	
		T_A = -40 °C - 125 °C	–1.5		1.5	
TCR_{-35}	Temperature Coefficient of Resistance	T1 = -40 °C, T2 = -30 °C		+6220		ppm/°C
TCR_{25}		T1 = 20 °C, T2 = 30 °C		+6400		
TCR_{85}		T1 = 80 °C, T2 = 90 °C		+5910		
TCR_{-35} %	Temperature Coefficient of Resistance Tolerance	T1 = -40 °C, T2 = -30 °C		±0.4		%
TCR_{25} %		T1 = 20 °C, T2 = 30 °C		±0.2		
TCR_{85} %		T1 = 80 °C, T2 = 90 °C		±0.3		
ΔR	Sensor Long Term Drift (Reliability)	96 hours continuous operation at RH = 85% and T_A = 130 °C V_{Bias} = 5.5 V, DEC Package	-1	±0.1	1	%
		96 hours continuous operation at RH = 85%, T_A = 130 °C, V_{Bias} = 5.5 V DYA Package	-1	+/-0.14	1	
		600 hours continuous operation at T_A = 150 °C V_{Bias} = 5.5V DEC Package	-1	0.5	1.8	
		600 hours continuous operation at T_A = 150 °C V_{Bias} = 5.5 V, DYA Package	-1.5	+/-0.2	1.5	
		1000 hours continuous operation at T_A = 150°C V_{Bias} = 5.5 V, DYA Package	-1.8	+/-0.3	1.8	
t_{RES} (stirred liquid)	Thermal response to 63%	T1 = 25 °C in Still Air to T2 = 125 °C in Stirred Liquid		0.6		s
t_{RES} (still air)	Thermal response to 63%	T1 = 25 °C to T2 = 70 °C in Still Air		3.2		s

7.6 Typical Characteristics

at T_A = 25 °C, (unless otherwise noted)

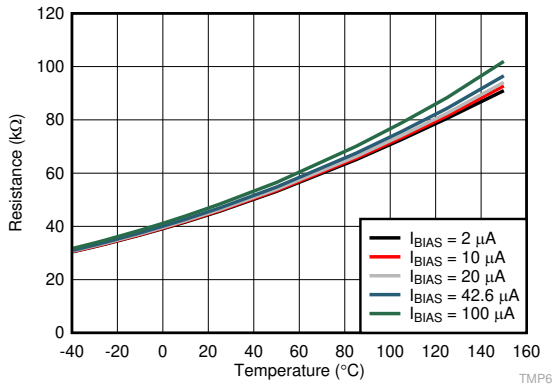
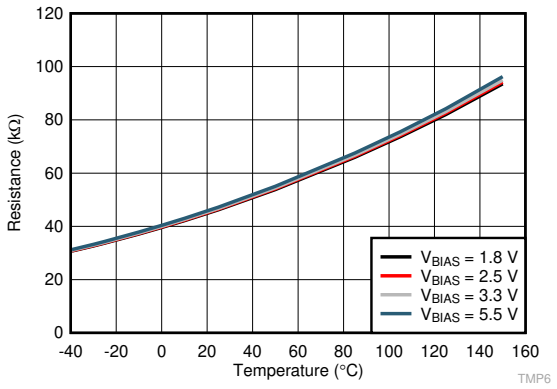


Figure 7-1. Resistance vs. Ambient Temperature Using Multiple Bias Currents



R_{Bias} = 47 kΩ with ±0.01 % Tolerance

Figure 7-2. Resistance vs. Ambient Temperature Using Multiple Bias Voltages

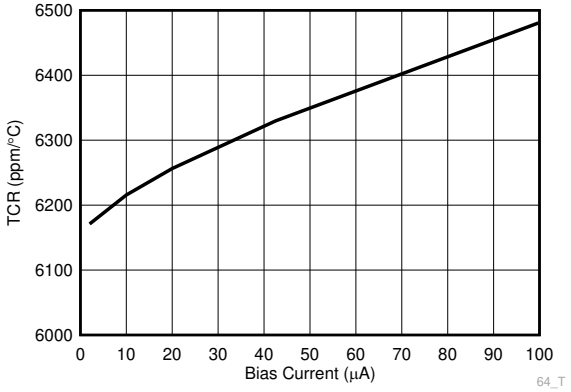
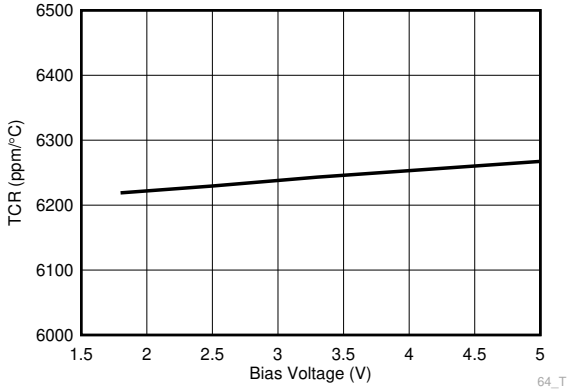


Figure 7-3. TCR as a Function of Sense Current, I SNS



R_{Bias} = 47 kΩ with ±0.01% Tolerance

Figure 7-4. TCR as a Function of Sense Voltage, V SNS

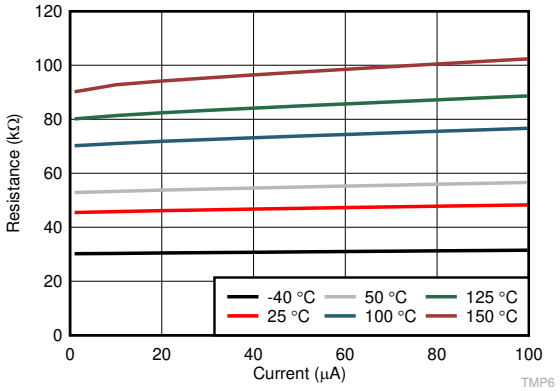
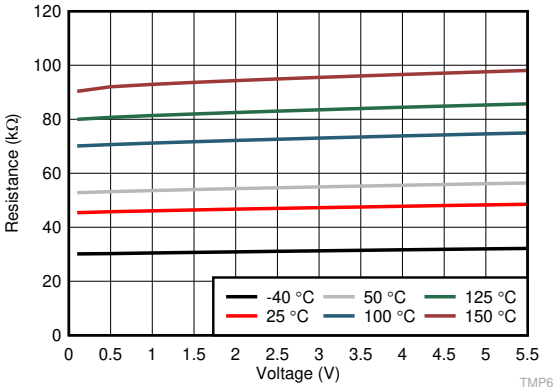
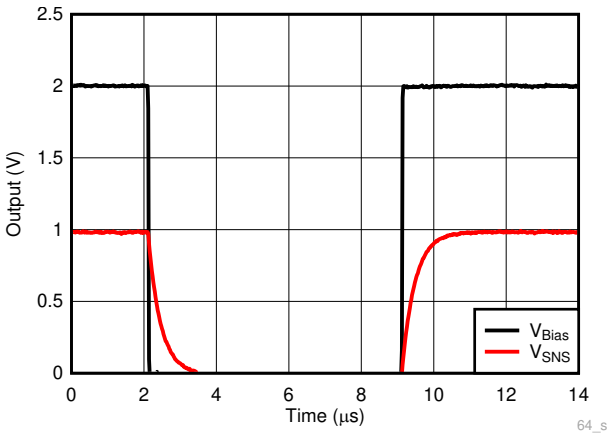


Figure 7-5. Supply Dependence Resistance vs. Bias Current



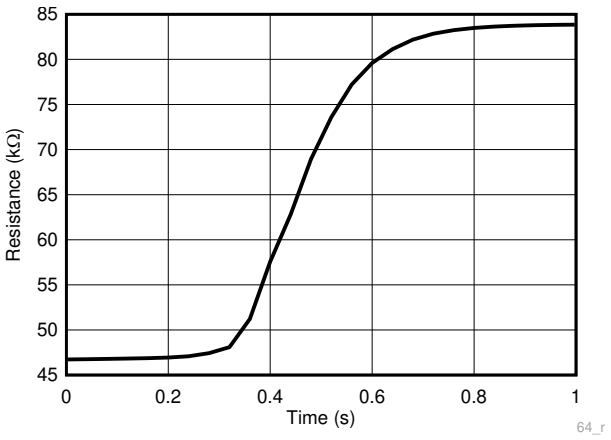
R_{Bias} = 47 kΩ with ±0.01% Tolerance

Figure 7-6. Supply Dependence R vs. V_{Bias}



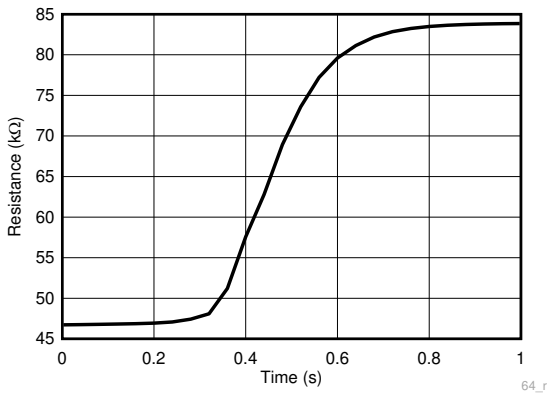
TMP64-Q1: V_{SNS} = 1 V

Figure 7-7. Step Response



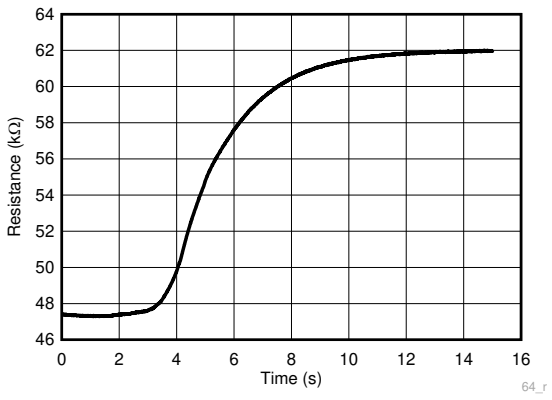
TMP64-Q1: Stirred Liquid. Temperature: 25 °C to 125 °C

Figure 7-8. DEC Thermal Response Time



TMP64-Q1: Stirred Liquid. Temperature: 25 °C to 125 °C

Figure 7-9. DYA Thermal Response Time



TMP64-Q1: Still Air

Figure 7-10. Thermal Response Time

8 Detailed Description

8.1 Overview

The TMP64-Q1 silicon linear thermistor has a linear positive temperature coefficient (PTC) that results in a uniform and consistent temperature coefficient resistance (TCR) across a wide operating temperature range. TI uses a special silicon process where the the doping level and active region areas devices control the key characteristics (the temperature coefficient resistance (TCR) and nominal resistance (R25)) . The device has an active area and a substrate due to the polarized terminals. Connect the positive terminal to the highest voltage potential. Connect the negative terminal to the lowest voltage potential.

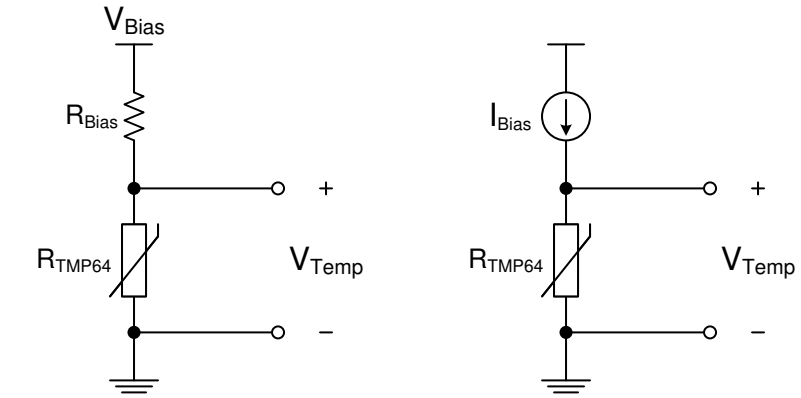
Unlike an NTC, which is a purely resistive device, the TMP64-Q1 resistance is affected by the current across the device and the resistance changes when the temperature changes. In a voltage divider circuit, it is recommended to maintain the top resistor value at 47 kΩ. Changing the top resistor value or the V_{BIAS} value changes the resistance vs temperature table (R-T table) of the TMP64-Q1, and subsequently the polynomials as described in Section 9.2.1.1. Consult Section 8.3.1 for more information.

$$TCR\ (ppm/°C) = (R_{T2} – R_{T1}) / ((T_2 – T_1) \times R_{(T2+T1)/2}) \quad (1)$$

Below are the definitions of the key terms used throughout this document:

- I_{SNS}: Current flowing through the TMP64-Q1.
- V_{SNS}: Voltage across the two TMP64-Q1 terminals.
- I_{Bias}: Current supplied by the biasing circuit.
- V_{Bias}: Voltage supplied by the biasing circuit.
- V_{Temp}: Output voltage that corresponds to the measured temperature. Note that this is different from V_{Sns}. In the use case of a voltage divider circuit with the TMP64-Q1 in the high side, V_{Temp} is taken across R_{Bias}.

8.2 Functional Block Diagram



$$V_{Temp} = \frac{V_{Bias} * R_{TMP64}}{R_{Bias} + R_{TMP64}} \qquad V_{Temp} = I_{Bias} * R_{TMP64}$$

Figure 8-1. Typical Implementation Circuits

8.3 Feature Description

8.3.1 TMP64-Q1 R-T table

The TMP64-Q1 R-T table must be re-calculated for any change in the bias voltage, bias resistor, or bias current. TI provides a Thermistor Design Tool to calculate the R-T table. The system designer should always validate the calculations provided.

8.3.2 Linear resistance curve

The TMP64-Q1 has good linear behavior across the whole temperature range as shown in Figure 7-1. This range allows a simpler resistance-to-temperature conversion method that reduces look-up table memory requirements. The linearization circuitry or midpoint calibration associated with traditional NTCs is not necessary with the device.

The linear resistance across the entire temperature range allows the device to maintain sensitivity at higher operating temperatures.

8.3.3 Positive Temperature Coefficient (PTC)

The TMP64-Q1 has a positive temperature coefficient. As temperature increases the device resistance increases leading to a reduction in power consumption of the bias circuit. In comparison, a negative coefficient system increases power consumption with temperature as the resistance decreases.

The TMP64-Q1 benefits from the reduced power consumption of the bias circuit with less self-heating than a typical NTC system.

8.3.4 Built-In Fail Safe

The TMP6 family feature a positive tempeature coefficient. During a short-to-supply condition, the thermistor will have increased current and power dissipated. Due to the positive temperature slope, the TMP6 will increase resistance and limit self-heating by design.

In contrast, a NTC would continually reduce resistance due to self-heating leading to a positive feedback of increasing power dissipation and decreasing resistance.

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMP64-Q1 is a positive temperature coefficient (PTC) linear silicon thermistor. The device behaves like a temperature-dependent resistor, and may be configured in a variety of ways to monitor temperature based on the system-level requirements. The TMP64-Q1 has a nominal resistance at 25 °C (R25) of 47 kΩ , a maximum operating voltage of 5.5 V (V_{Sns}), and maximum supply current of 100 µA (I_{Sns}). This device may be used in a variety of applications to monitor temperature close to a heat source with the very small DEC package option compatible with the typical 0402 (inch) footprint. Some of the factors that influence the total measurement error include the ADC resolution (if applicable), the tolerance of the bias current or voltage, the tolerance of the bias resistance in the case of a voltage divider configuration, and the location of the sensor with respect to the heat source.

9.2 Typical Application

9.2.1 Thermistor Biasing Circuits

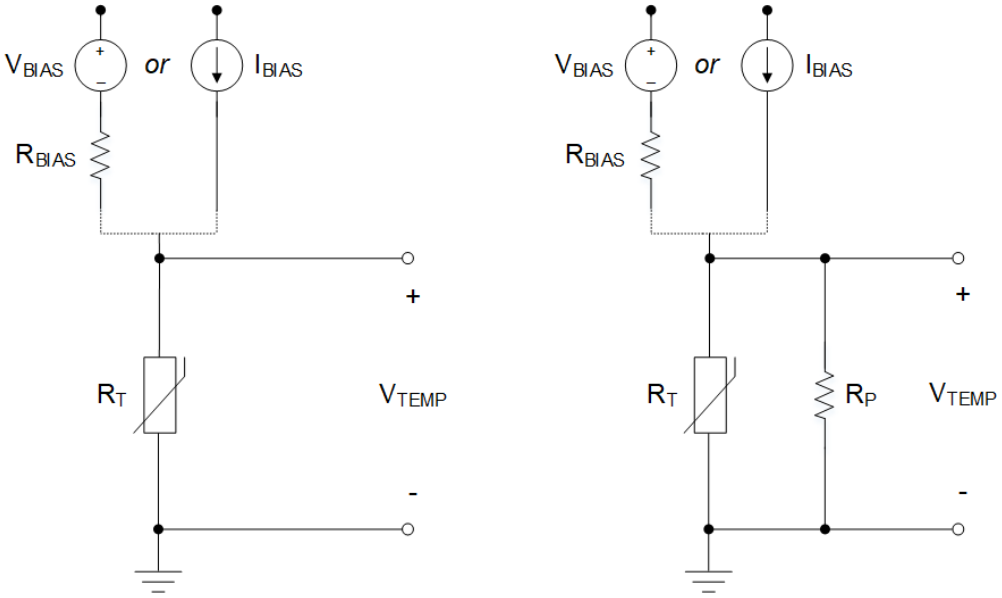


Figure 9-1. Biasing Circuit Implementations With Linear Thermistor (Left) vs. Non-Linear Thermistor (Right)

9.2.1.1 Design Requirements

Existing thermistors, in general, have a non-linear temperature vs. resistance curve. To linearize the thermistor response, the engineer can use a voltage linearization circuit with a voltage divider configuration, or a resistance linearization circuit by adding another resistance in parallel with the thermistor, R_P. Section 9.2.1 highlights the two implementations where R_T is the thermistor resistance. To generate an output voltage across the thermistor, the engineer can use a voltage divider circuit with the thermistor placed at either the high side (close to supply) or low side (close to ground), depending on the desired voltage response (negative or positive). Alternatively, the thermistor can be biased directly using a precision current source (yielding the highest accuracy and voltage gain). It is common to use a voltage divider with thermistors because of its simple implementation and lower cost. The TMP64-Q1, on the other hand, has a linear positive temperature coefficient (PTC) of resistance such

that the voltage measured across it increases linearly with temperature. As such, the need for a linearization circuits is no longer a requirement, and a simple current source or a voltage divider circuit can be used to generate the temperature voltage.

This output voltage can be interpreted using a comparator against a voltage reference to trigger a temperature trip point that is either tied directly to an ADC to monitor temperature across a wider range or used as feedback input for an active feedback control circuit.

The voltage across the TMP64-Q1, as described in Equation 2, can be translated to temperature using either a lookup table method (LUT) or a fitting polynomial, V(T). The Thermistor Design Tool must be used to translate Vtemp to Temperature. The temperature voltage must first be digitized using an ADC. The necessary resolution of this ADC is dependent on the biasing method used. Additionally, for best accuracy, the bias voltage (V_{BIAS}) should be tied to the reference voltage of the ADC to create a measurement where the difference in tolerance between the bias voltage and the reference voltage cancels out. The engineer can also implement a low-pass filter to reject system level noise, and the user should place the filter as close to the ADC input as possible.

9.2.1.2 Detailed Design Procedure

The resistive circuit divider method produces an output voltage (V_{TEMP}) scaled according to the bias voltage (V_{BIAS}). When V_{BIAS} is also used as the reference voltage of the ADC, any fluctuations or tolerance error due to the voltage supply is canceled and does not affect the temperature accuracy. This type of configuration is shown in Figure 9-2. Equation 2 describes the output voltage (V_{TEMP}) based on the variable resistance of the TMP64-Q1 ($R_{TMP64-Q1}$) and bias resistor (R_{BIAS}). The ADC code that corresponds to that output voltage, ADC full-scale range, and ADC resolution is given in Equation 3.

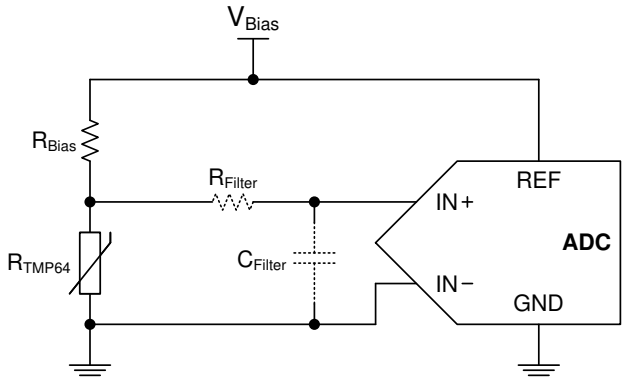


Figure 9-2. TMP64-Q1 Voltage Divider With an ADC

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right) \quad (2)$$

$$\text{ADC Code} = \left(\frac{V_{TEMP}}{FSR} \right) \times 2^{n} \quad (3)$$

where

- FSR is the full-scale range of the ADC, which is the voltage at REF to GND (V_{REF})
- n is the resolution of the ADC

Equation 4 shows whenever $V_{REF} = V_{BIAS}$, V_{BIAS} cancels out.

$$\text{ADC Code} = \left(\frac{V_{BIAS} \times \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right)}{V_{BIAS}} \right) \times 2^n = \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right) \times 2^n \quad (4)$$

The engineer can use a polynomial equation or a LUT to extract the temperature reading based on the ADC code read in the microcontroller. The Thermistor Design Tool should be used to translate the TMP64-Q1 resistance to temperature.

The cancellation of V_{BIAS} is one benefit to using a voltage-divider (ratiometric approach), but the sensitivity of the output voltage of the divider circuit cannot increase much. Therefore, not all of the ADC codes are used due to the small voltage output range compared to the FSR. This application is very common, however, and is simple to implement.

The engineer can use a current source-based circuit, like the one shown in Figure 9-3, to have better control over the sensitivity of the output voltage and achieve higher accuracy. In this case, the output voltage is simply V = I × R. For example, if a current source of 100 µA is used with the TMP64-Q1, the output voltage spans approximately 5.5 V and has a gain up to 40 mV/°C. Having control over the voltage range and sensitivity allows for full utilization of the ADC codes and full-scale range. Similar to the ratiometric approach above, if the ADC has a built-in current source that shares the same bias as the reference voltage of the ADC, the tolerance of the supply current cancels out. In this case, a precision ADC is not required. This method yields the best accuracy, but can increase the system implementation cost.

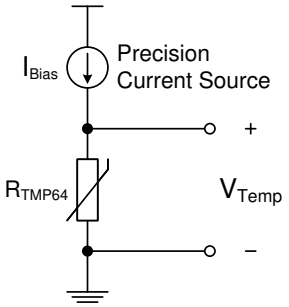


Figure 9-3. TMP64-Q1 Biasing Circuit With Current Source

In comparison to the non-linear NTC thermistor in a voltage divider, the TMP64-Q1 has an enhanced linear output characteristic. The two voltage divider circuits with and without a linearization parallel resistor, R_P, are shown in Figure 9-4. Consider an example where V_{BIAS} = 5 V, R_{BIAS} = 47 kΩ, and a parallel resistor (R_P) is used with the NTC thermistor (R_{NTC}) to linearize the output voltage with an additional 47-kΩ resistor. The TMP64-Q1 produces a linear curve across the entire temperature range while the NTC curve is only linear across a small temperature region. When the parallel resistor (R_P) is added to the NTC circuit, the added resistor makes the curve much more linear but greatly affects the output voltage range.

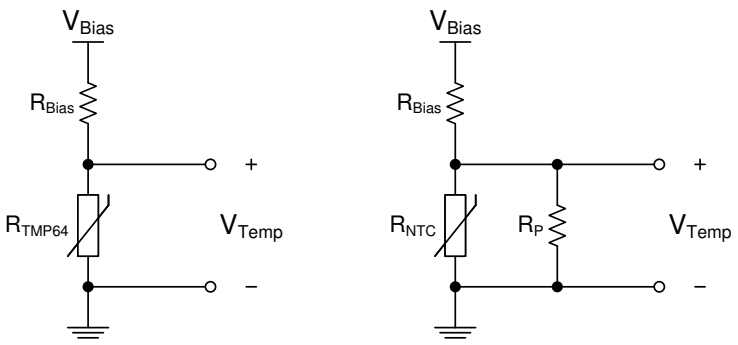


Figure 9-4. TMP64-Q1 vs. NTC With Linearization Resistor (R_P) Voltage Divider Circuits

9.2.1.2.1 Thermal Protection With Comparator

The engineer can use the TMP64-Q1, a voltage reference, and a comparator to program the thermal protection. As shown in Figure 9-5, the output of the comparator remains low until the voltage of the thermistor divider, with R_{BIAS} and $R_{TMP64-Q1}$, rises above the threshold voltage set by R_1 and R_2. When the output goes high, the comparator signals an overtemperature warning signal. The engineer can also program the hysteresis to prevent the output from continuously toggling around the temperature threshold when the output returns low. Either a comparator with built-in hysteresis or feedback resistors may be used.

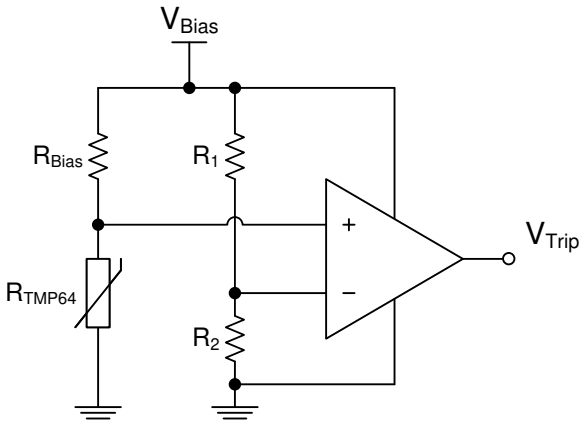


Figure 9-5. Temperature Switch Using TMP64-Q1 Voltage Divider and a Comparator

9.2.1.2.2 Thermal Foldback

One application that uses the output voltage of the TMP64-Q1 in an active control circuit is thermal foldback. This is performed to reduce, or fold back, the current driving a string of LEDs, for example. At high temperatures, the LEDs begin to heat up due to environmental conditions and self heating. Thus, at a certain temperature threshold based on the LED's safe operating area, the driving current must be reduced to cool down the LEDs and prevent thermal runaway. The TMP64-Q1 voltage output increases with temperature when the output is in the lower position of the voltage divider and can provide a response used to fold back the current. Typically, the current is held at a specified level until a high temperature is reached, known as the knee point, where the current must be rapidly reduced. To better control the temperature/voltage sensitivity of the TMP64-Q1, a rail-to-rail operational amplifier is used. In the example shown in Figure 9-6, the temperature “knee” where the foldback begins is set by the reference voltage (2.5 V) at the positive input, and the feedback resistors set the response of the foldback curve. The foldback knee point may be chosen based on the output of the voltage divider and the corresponding temperature from Equation 5 (like 110 °C, for example). A buffer is used in-between the voltage divider with $R_{TMP64-Q1}$ and the input to the op amp to prevent loading and variations in V_{TEMP}.

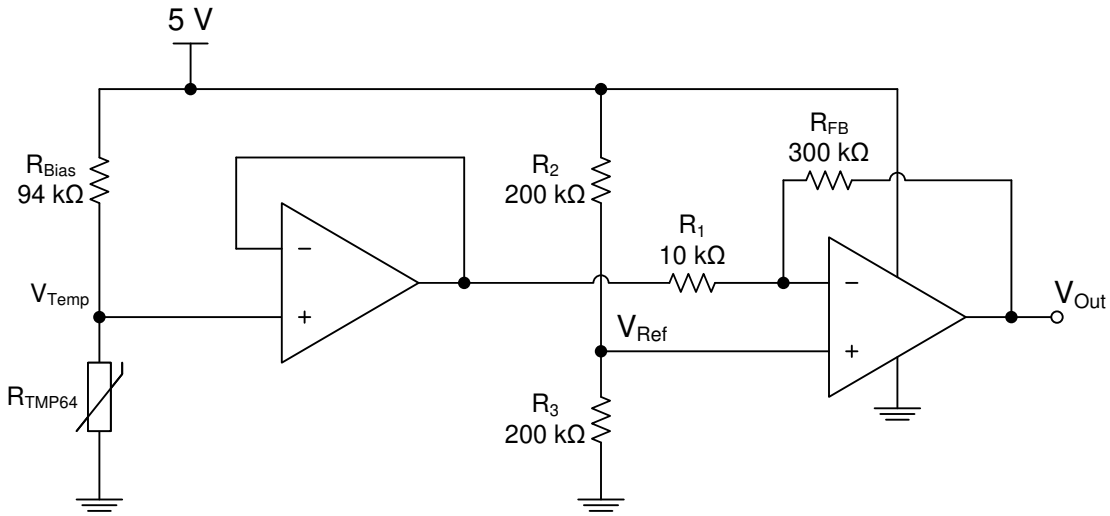


Figure 9-6. Thermal Foldback Using TMP64-Q1 Voltage Divider and a Rail-to-Rail Op Amp

The op amp remains high as long as the voltage output is below V_{Ref}. When the temperature goes above 110 °C, then the output swings low to the 0-V rail of the op amp. The rate at which the foldback occurs is dependent on the feedback network, R_{FB} and R_1, which varies the gain of the op amp, G, given by Equation 6. This in return controls the voltage/temperature sensitivity of the circuit. This voltage output is fed into a LED driver IC that adjusts output current accordingly. The final output voltage used for thermal foldback is V_{OUT}, and is given in Equation 7. In this example where the knee point is set at 110 °C, the output voltage curve is as shown in Figure 9-7.

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right) \tag{5}$$

$$G = \frac{R_{FB}}{R_1} \tag{6}$$

$$V_{OUT} = -G \times V_{TEMP} + (1 + G) \times V_{REF} \tag{7}$$

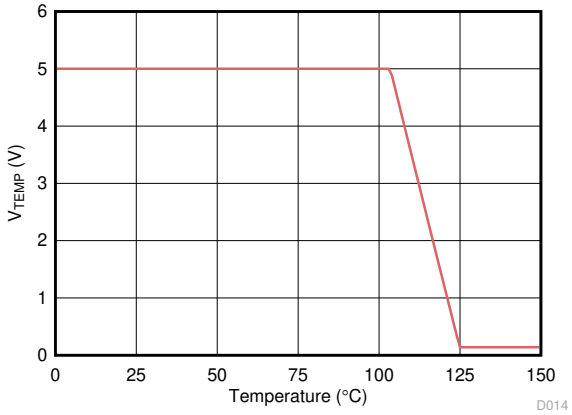


Figure 9-7. Thermal Foldback Voltage Output Curve

9.2.1.3 Application Curve

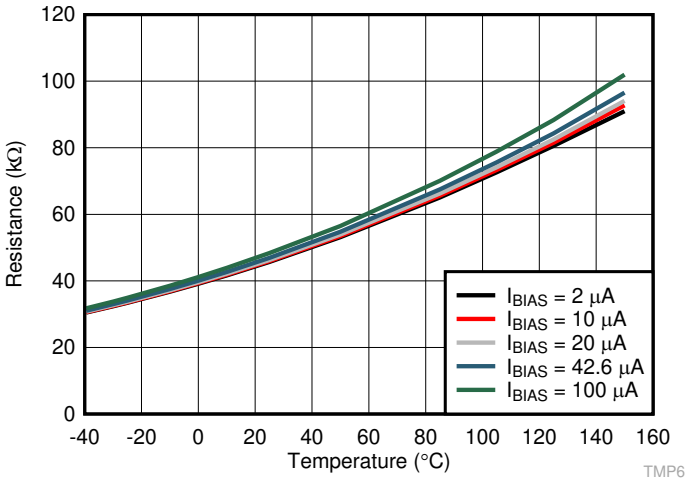


Figure 9-8. TMP64-Q1 Temperature Voltage With Varying Current Sources

10 Power Supply Recommendations

The maximum recommended operating voltage of the TMP64-Q1 is 5.5 V (V_{Sns}), and the maximum current through the device is 100 µA (I_{Sns}).

11 Layout

11.1 Layout Guidelines

The layout of the TMP64-Q1 is similar to that of a passive component. If the device is biased with a current source, the positive pin 2 is connected to the source, while the negative pin 1 is connected to ground. If the circuit is biased with a voltage source, and the device is placed on the lower side of the resistor divider, V– is connected to ground, and V+ is connected to the output (V_{TEMP}). If the device is placed on the upper side of the divider, V+ is connected to the voltage source and V– is connected to the output voltage (V_{TEMP}). Figure 11-1 shows the device layout.

11.2 Layout Example

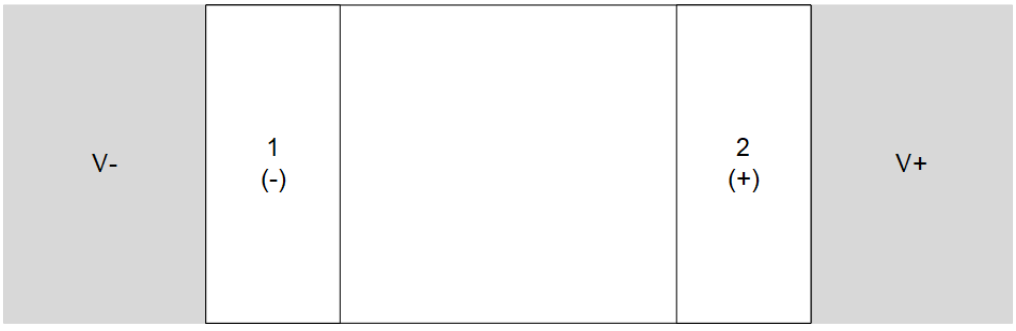


Figure 11-1. Recommended Layout: DEC Package

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP6431QDECRQ1	ACTIVE	X1SON	DEC	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TMP6431QDECTQ1	ACTIVE	X1SON	DEC	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TMP6431QDYARQ1	ACTIVE	SOT-5X3	DYA	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	1HH	Samples
TMP6431QDYATQ1	ACTIVE	SOT-5X3	DYA	2	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	1HH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP64-Q1 :

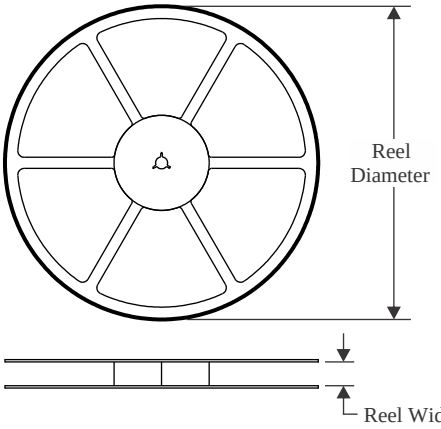
- Catalog: TMP64

NOTE: Qualified Version Definitions:

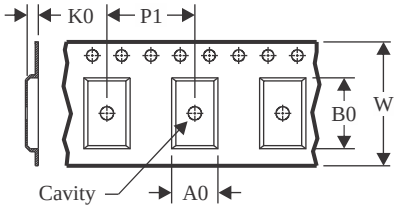
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

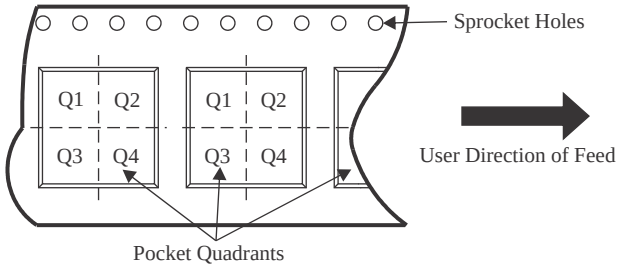


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

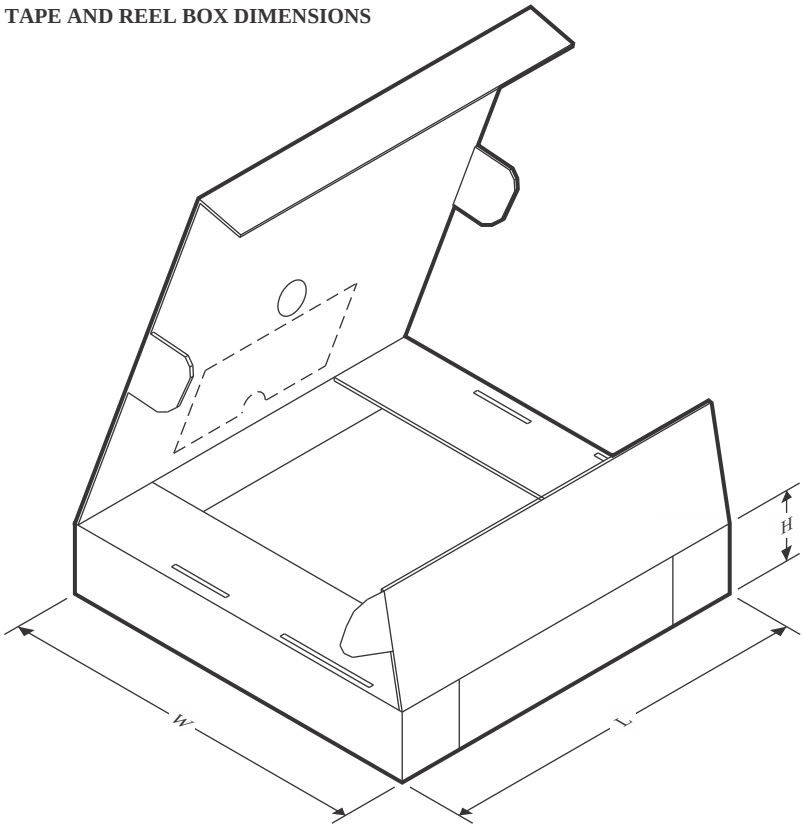
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP6431QDECRQ1	X1SON	DEC	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TMP6431QDECTQ1	X1SON	DEC	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TMP6431QDYARQ1	SOT-5X3	DYA	2	3000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1
TMP6431QDYATQ1	SOT-5X3	DYA	2	250	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

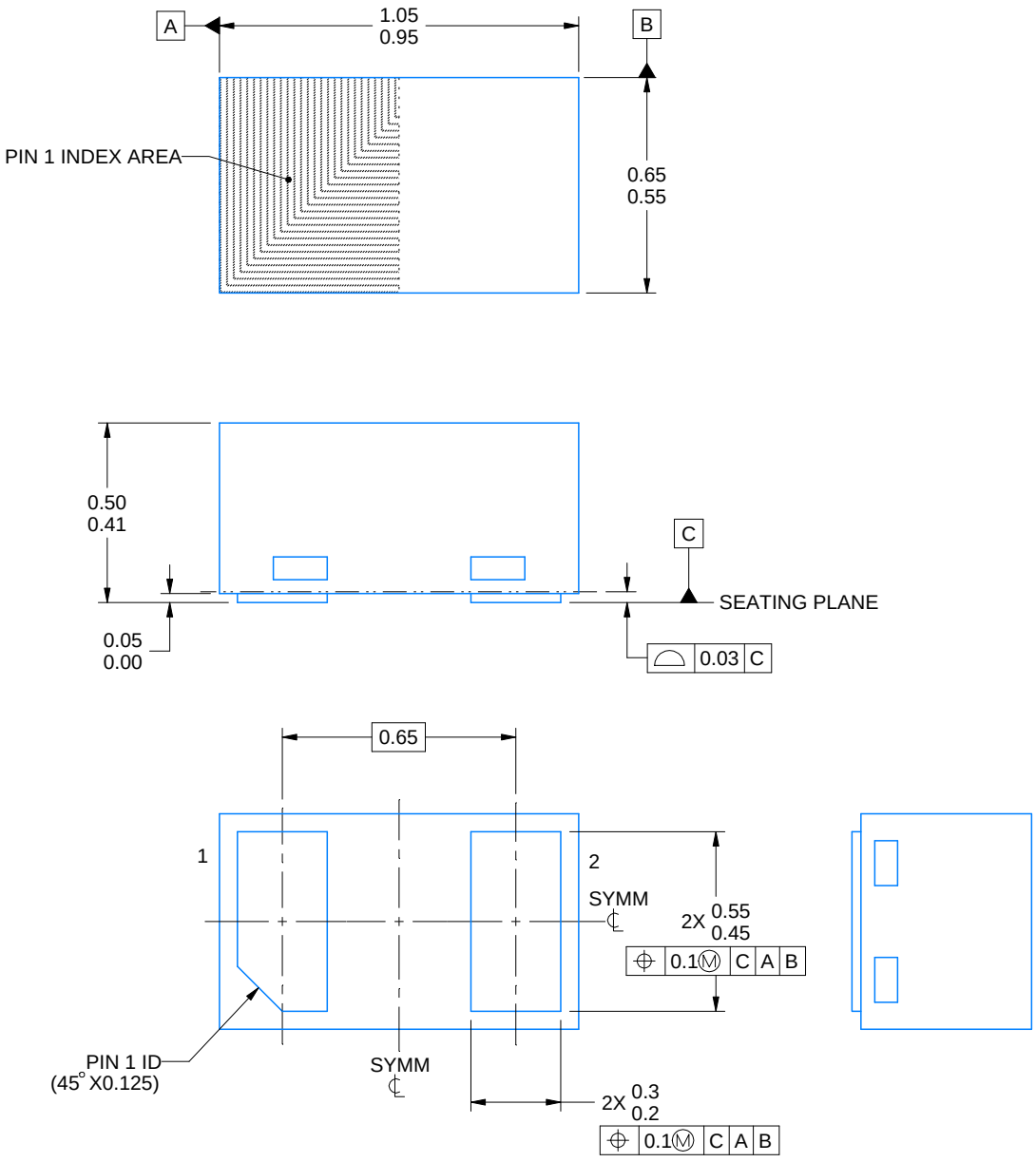
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP6431QDECRQ1	X1SON	DEC	2	10000	205.0	200.0	33.0
TMP6431QDECTQ1	X1SON	DEC	2	250	205.0	200.0	33.0
TMP6431QDYARQ1	SOT-5X3	DYA	2	3000	210.0	200.0	42.0
TMP6431QDYATQ1	SOT-5X3	DYA	2	250	210.0	200.0	42.0

PACKAGE OUTLINE

DEC0002A

X1SON - 0.5 mm max height

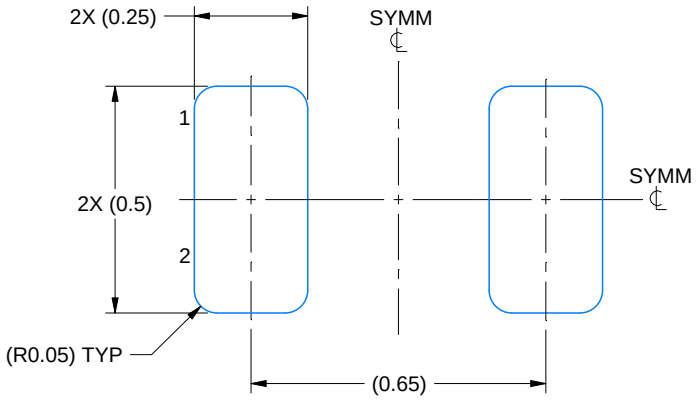
PLASTIC SMALL OUTLINE - NO LEAD



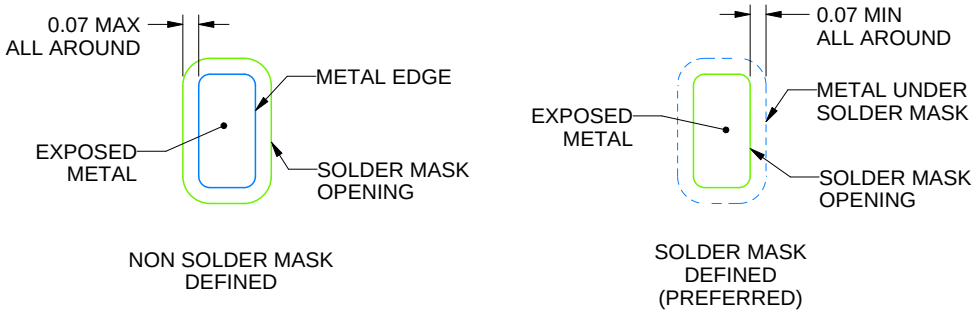
4224506/A 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

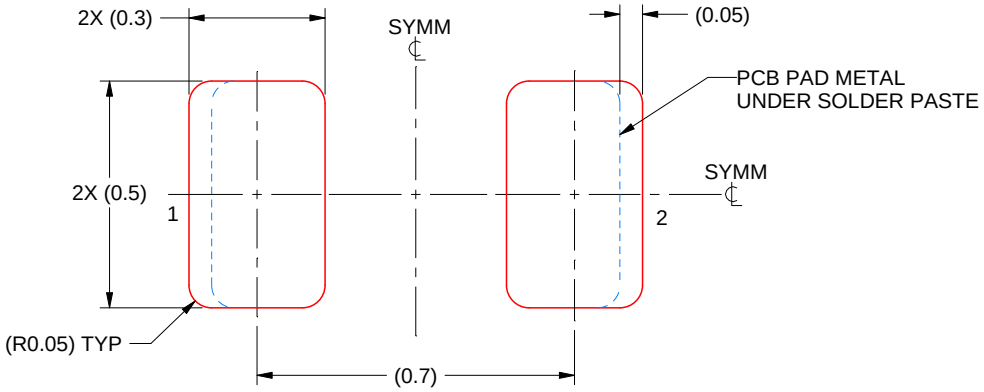


SOLDER MASK DETAILS

4224506/A 08/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224506/A 08/2018

NOTES: (continued)

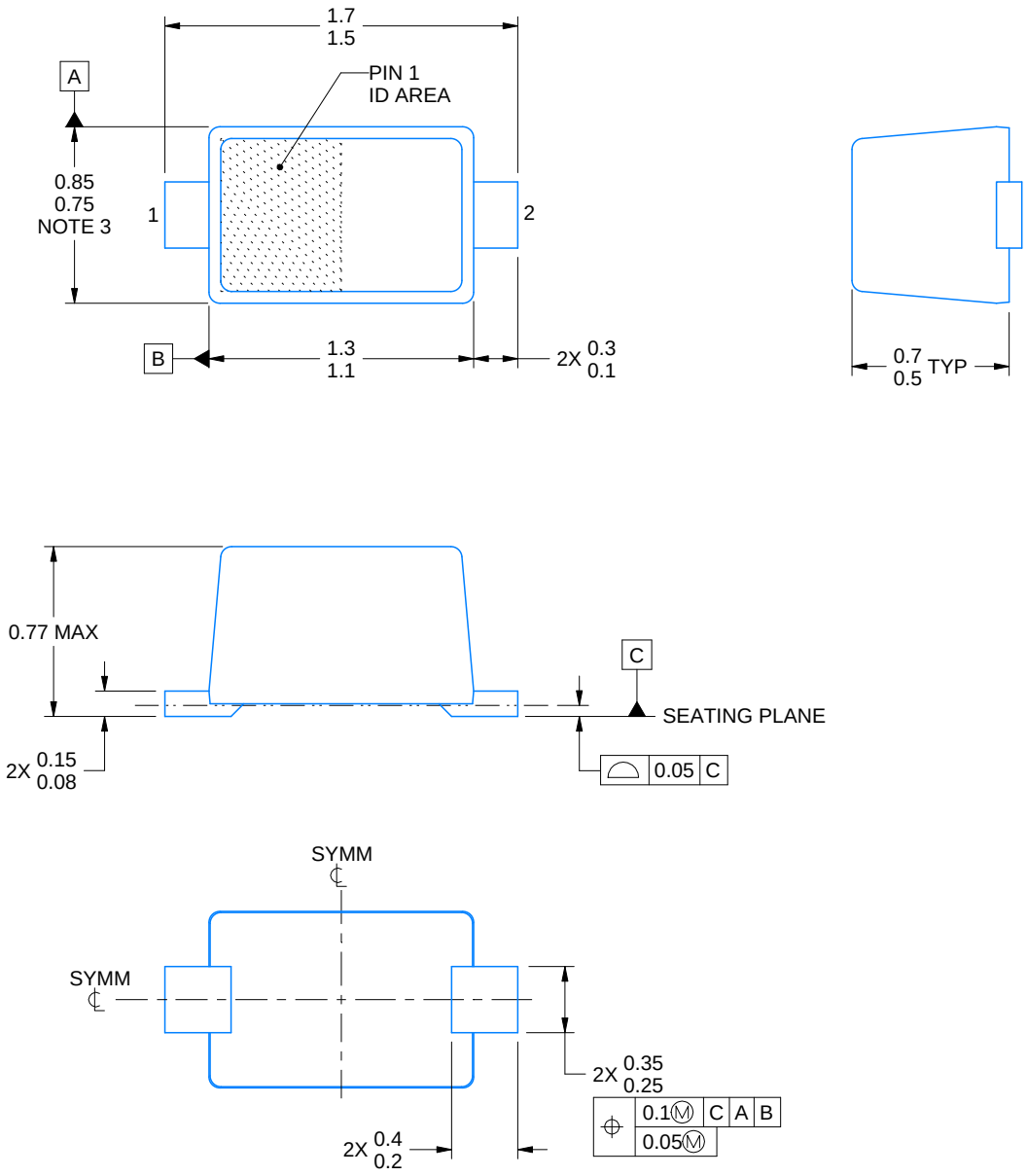
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

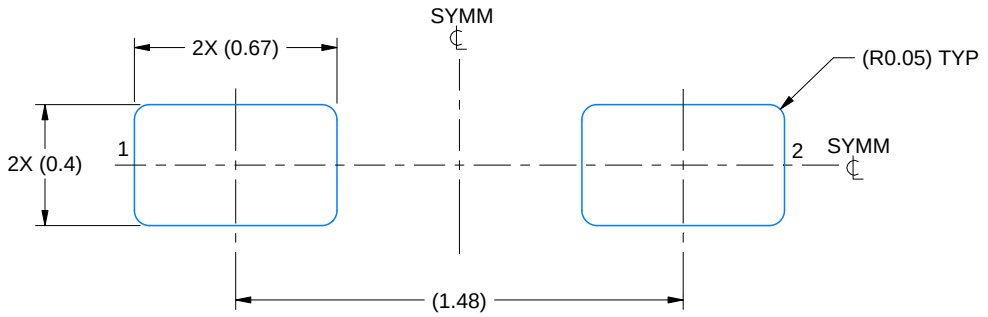
PLASTIC SMALL OUTLINE



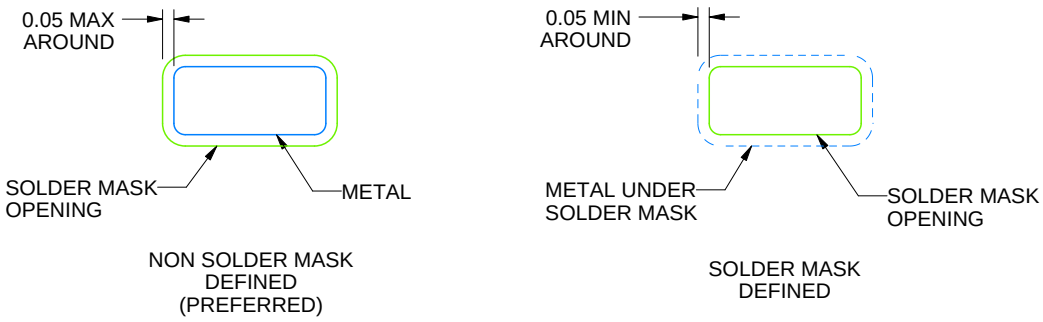
4224978/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

4224978/B 09/2021

NOTES: (continued)

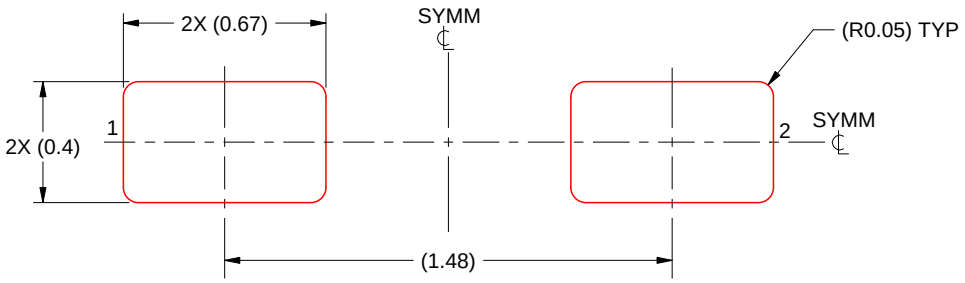
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/B 09/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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