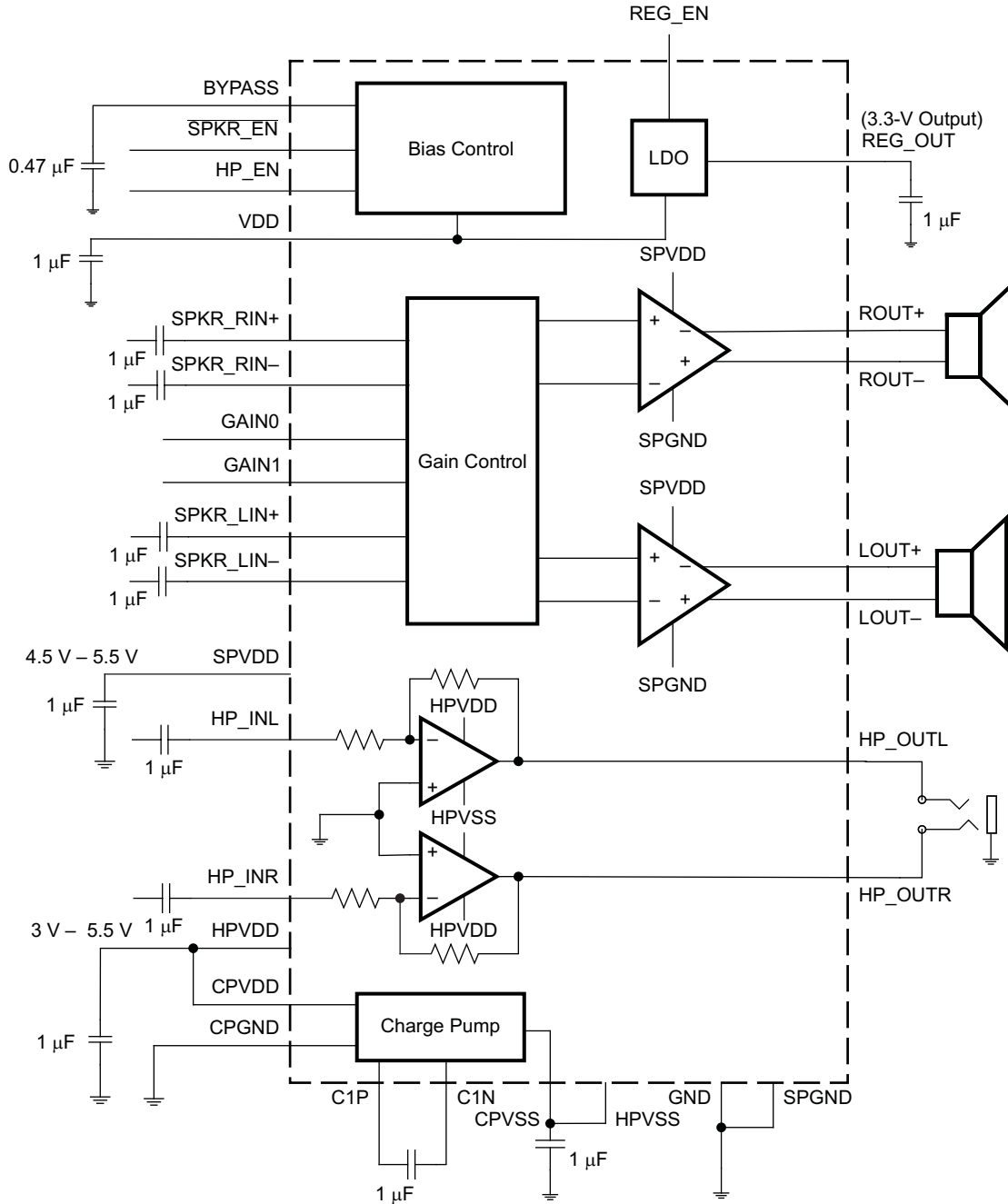






These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Functional Block Diagram

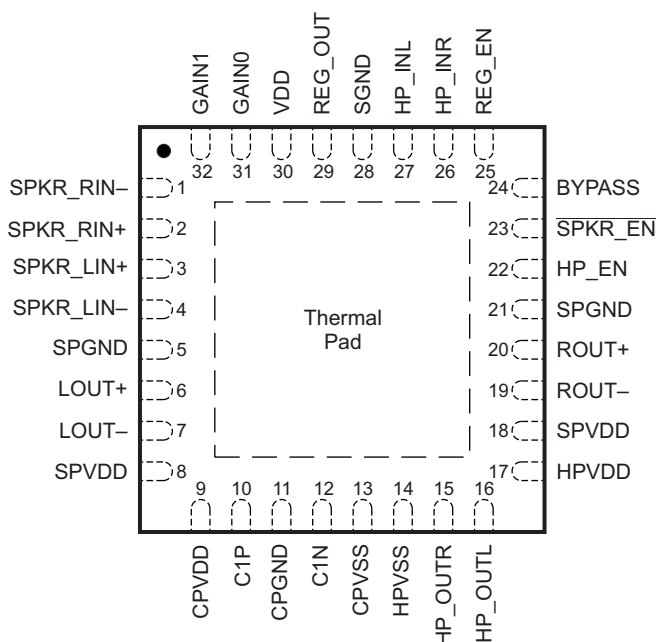


AVAILABLE PACKAGE OPTIONS

T <sub>A</sub>	PACKAGED DEVICE <sup>(1)(2)</sup> 32-Pin QFN (RHB)	SYMBOL
–40°C to 85°C	TPA6043A4RHB	RHB

- (1) The RHB package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6043A4RHBR).
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

TPA6043A4RHB  
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL NAME	NO.	I/O/P	DESCRIPTION
SPKR_RIN–	1	I	Right-channel negative differential audio input for speaker amplifier
SPKR_RIN+	2	I	Right-channel positive differential audio input for speaker amplifier
SPKR_LIN+	3	I	Left-channel positive differential audio input for speaker amplifier
SPKR_LIN–	4	I	Left-channel negative differential audio input for speaker amplifier
SPGND	5, 21	P	Speaker power ground
LOU+	6	O	Left-channel positive audio output
LOU–	7	O	Left-channel negative audio output
SPVDD	8, 18	P	Supply voltage terminal for speaker amplifier
CPVDD	9	P	Charge pump positive supply, connect to HPVDD via star connection
C1P	10	I/O	Charge pump flying capacitor positive terminal
CPGND	11	P	Charge pump ground
C1N	12	I/O	Charge pump flying capacitor negative terminal
CPVSS	13	P	Charge pump output (negative supply for headphone amplifier), connect to HPVSS
HPVSS	14	P	Headphone amplifier negative supply, connect to CPVSS
HP_OUTR	15	O	Right-channel capacitor-free headphone output
HP_OUTL	16	O	Left-channel capacitor-free headphone output
HPVDD	17	P	Headphone amplifier supply voltage, connect to CPVDD
ROUT–	19	O	Right-channel negative audio output

**TERMINAL FUNCTIONS (continued)**

TERMINAL		I/O/P	DESCRIPTION
NAME	NO.		
ROUT+	20	O	Right-channel positive audio output
HP_EN	22	I	Headphone channel enable logic input; active high enable. HIGH=ENABLE.
SPKR_EN	23	I	Speaker channel enable logic input; active low enable. LOW=ENABLE.
BYPASS	24	P	Common-mode bias voltage for speaker preamplifiers
REG_EN	25	I	Enable pin (Active HIGH) for turning on/off LDO. HIGH=ENABLE
HP_INR	26	I	Headphone right-channel audio input
HP_INL	27	I	Headphone left-channel audio input
SGND	28	P	Signal ground, connect to CPGND and SPGND
REG_OUT	29	O	Regulated 3.3-V output
VDD	30	P	Positive power supply
GAIN0	31	I	Bit 0, MSB, of gain select bits
GAIN1	32	I	Bit 1, LSB, of gain select bits
Thermal Pad	Die Pad	P	Solder the thermal pad on the bottom of the QFN package to the GND plane of the PCB. It is required for mechanical stability and will enhance thermal performance.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT
Supply voltage	HPVDD, VDD, SPVDD, CPVDD	–0.3 to 6	V
V <sub>I</sub> Input voltage	SPKR_LIN+, SPKR_LIN-, SPKR_RIN+, SPKR_RIN-, HP_EN, GAIN0, GAIN1, SPK_EN, REG_EN	–0.3 to 6.3	V
	HP_INL, HP_INR HP Enabled	–3.5 to 3.5	
	HP_INL, HP_INR HP not Enabled	–0.3 to 3.5	
Continuous total power dissipation		See Dissipation Rating Table	
T <sub>A</sub> Operating free-air temperature range		–40 to 85	°C
T <sub>J</sub> Operating junction temperature range		–40 to 150	°C
T <sub>stg</sub> Storage temperature range		–65 to 150	°C
Electrostatic discharge	HBM for HP_OUTL and HP_OUTR	8	kV
Electrostatic discharge, all other pins	CDM	500	V
	HBM	2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATINGS**

PACKAGE <sup>(1)</sup>	T <sub>A</sub> ≤ 25°C	DERATING FACTOR	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C
RHB	5.06 W	40 mW/°C	4.04 W	3.23 W

(1) The PowerPAD™ must be soldered to a thermal land on the printed-circuit board. See the Texas Instruments document, PowerPAD™ Thermally Enhanced Package application report (literature number [SLMA002](#)) for more information regarding the PowerPAD™ package.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	MAX	UNIT
Supply voltage	VDD, SPVDD	4.5	5.5	V
Supply voltage	HPVDD, CPVDD	3	5.5	V
V <sub>IH</sub> High-level input voltage	SPKR_EN, HP_EN, GAIN0, GAIN1, REG_EN	2		V
V <sub>IL</sub> Low-level input voltage	SPKR_EN, HP_EN, GAIN0, GAIN1, REG_EN		0.8	V

## RECOMMENDED OPERATING CONDITIONS (continued)

	MIN	MAX	UNIT
T <sub>A</sub> Operating free-air temperature	–40	85	°C

## GENERAL DC ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25°C, VDD = SPVDD = HPVDD = CPVDD = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>IH</sub> High-level input current	SPKR_EN, HP_EN, GAIN0, GAIN1, REG_EN = VDD		0.02	1	μA
I <sub>IL</sub> Low-level input current	SPKR_EN, HP_EN, GAIN0, GAIN1, REG_EN = 0 V		0.02	1	μA
I <sub>DD(Speaker)</sub> Supply current, speaker amplifier ONLY enabled	SPKR_EN = 0 V, HP_EN = REG_EN = 0 V		5	12	mA
I <sub>DD(HP)</sub> Supply current, headphone amplifier ONLY enabled	SPKR_EN = HP_EN = 2 V, REG_EN = 0 V		7.5	14	mA
I <sub>DD(REG)</sub> Supply current, regulator ONLY enabled	SPKR_EN = REG_EN = 2 V, HP_EN = 0 V		0.65	1	mA
I <sub>DD(SD)</sub> Supply current, shutdown mode	SPKR_EN = 2 V, HP_EN = REG_EN = 0 V		2.5	5	μA

## SPEAKER AMPLIFIER DC CHARACTERISTICS

T<sub>A</sub> = 25°C, VDD = SPVDD = 5 V, R<sub>L</sub> = 4 Ω, Gain = 6 dB (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OO</sub>   Output offset voltage (measured differentially)	Inputs AC-coupled to GND, Gain = 6 dB		0.5	10	mV
PSRR Power supply rejection ratio	VDD = SPVDD = 4.5 V to 5.5 V	–60	–74		dB

## SPEAKER AMPLIFIER AC CHARACTERISTICS

T<sub>A</sub> = 25°C, VDD = SPVDD = 5 V, R<sub>L</sub> = 4 Ω, Gain = 6 dB (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>O</sub> Output power	THD+N = 1%, f = 1 kHz, R <sub>L</sub> = 8 Ω		1.25		W
	THD+N = 10%, f = 1 kHz, R <sub>L</sub> = 8 Ω		1.5		
	THD+N = 1%, f = 1 kHz, R <sub>L</sub> = 4 Ω		2		
	THD+N = 10%, f = 1 kHz, R <sub>L</sub> = 4 Ω		2.3		
THD+N Total harmonic distortion plus noise	P <sub>O</sub> = 1 W, R <sub>L</sub> = 8 Ω, f = 20 Hz to 20 kHz		0.1%		
	P <sub>O</sub> = 0.5 W, R <sub>L</sub> = 8 Ω, f = 20 Hz to 20 kHz		0.08%		
kSVR Supply ripple rejection ratio	f = 1 kHz, CBYPASS = 0.47 μF, V <sub>RIPPLE</sub> = 200 mV <sub>PP</sub>		–60		dB
SNR Signal-to-noise rejection ratio	Maximum output at THD+N <1%, f = 1 kHz, Gain = 6 dB		90		dB
Crosstalk (Left-Right; Right-Left)	f = 1 kHz, P <sub>O</sub> = 1 W, Gain = 6 dB		–80		dB
	f = 10 kHz, P <sub>O</sub> = 1 W, Gain = 6 dB		–75		dB
V <sub>n</sub> Noise output voltage	CBYPASS = 0.47 μF, f = 20 Hz to 20 kHz, Gain = 6 dB, No weighting		30		μV <sub>rms</sub>
Z <sub>I</sub> Input Impedance	Gain = 21.6 dB	15	20		kΩ
G Gain	GAIN0, GAIN1 = 0.8 V	5.4	6	6.6	dB
	GAIN0 = 0.8 V; GAIN1 = 2 V	9.4	10	10.6	
	GAIN0 = 2 V, GAIN1 = 0.8 V	15	15.6	16.2	
	GAIN0, GAIN1 = 2 V	21	21.6	22.2	
Gain Matching	Channel-to Channel		0.01		dB
Start-up time from shutdown	CBYPASS = 0.47 μF		30		ms

## HEADPHONE AMPLIFIER DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $HPVDD = CPVDD = VDD = 5\text{ V}$ ,  $R_L = 16\ \Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OS} $	Output offset voltage	Inputs grounded		1	3	mV
PSRR	Power supply rejection ratio	$HPVDD = 4.5\text{ V to }5.5\text{ V}$	-75	-100		dB

## HEADPHONE AMPLIFIER AC CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $HPVDD = 5\text{ V}$ ,  $R_L = 16\ \Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (outputs in phase)	THD+N = 10%, $R_L = 16\ \Omega$ , $f = 1\text{ kHz}$		200		mW
		THD+N = 10%, $R_L = 32\ \Omega$ , $f = 1\text{ kHz}$		100		
THD+N	Total harmonic distortion plus noise	$P_O = 85\text{ mW}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $R_L = 16\ \Omega$		0.03%		
		$P_O = 50\text{ mW}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $R_L = 32\ \Omega$		0.04%		
	Dynamic Range with Signal Present	A-Weighted, $f = 20\text{ Hz to }20\text{ kHz}$		-100		dB FS
kSVR	Supply ripple rejection	$f = 1\text{ kHz}$ , 200-mV <sub>PP</sub> ripple		-60		dB
	Crosstalk	$P_O = 35\text{ mW}$ , $f = 20\text{ Hz to }20\text{ kHz}$		-80		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N 1%, $f = 1\text{ kHz}$		95		dB
$V_n$	Noise output voltage	$f = 20\text{ Hz to }20\text{ kHz}$ , No weighting		20		$\mu\text{V}_{rms}$
$Z_I$	Input Impedance		15	20		k $\Omega$
Gain	Closed-loop voltage gain	$R_L = 16\ \Omega$	-1.45	-1.5	-1.55	V/V
	Start-up time from shutdown			5		ms

## LDO CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $VDD = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_I$	Input voltage	$V_{DD}$	4.5		5.5	V
$I_O$	Continuous output current		120			mA
$V_O$	Output voltage	$0 < I_O < 120\text{ mA}$ ; $4.9\text{ V} < V_I < 5.5\text{ V}$	3.2	3.3	3.4	V
	Line regulation	$I_L = 5\text{ mA}$ ; $4.9\text{ V} < V_I < 5.5\text{ V}$		1.8	10	mV
	Load regulation	$I_L = 0 - 120\text{ mA}$ , $V_I = 5\text{ V}$		0.13	0.23	mV/ mA
	Power supply ripple rejection	$V_{DD} = 4.9\text{ V}$ , $I_L = 10\text{ mA}$		46		dB
		$f = 100\text{ Hz}$				

TYPICAL CHARACTERISTICS

Default graph conditions:  $V_{CC} = 5\text{ V}$ ,  $\text{Freq} = 1\text{ kHz}$ , AES17 Filter.

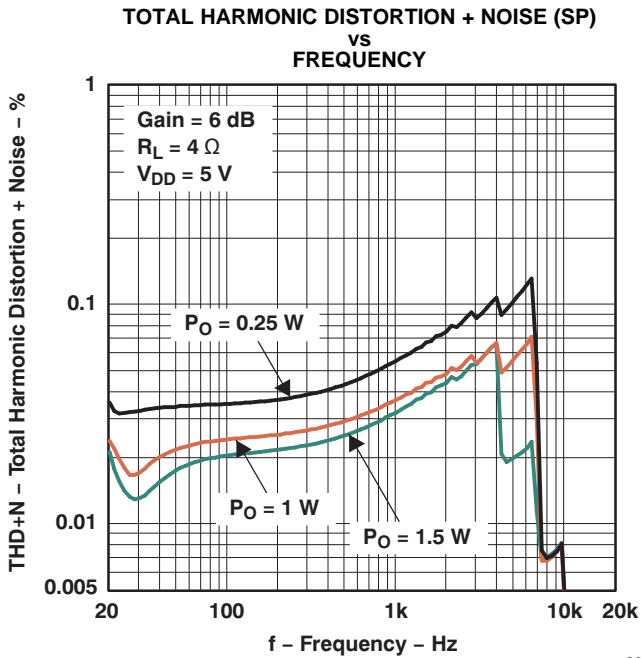


Figure 1.

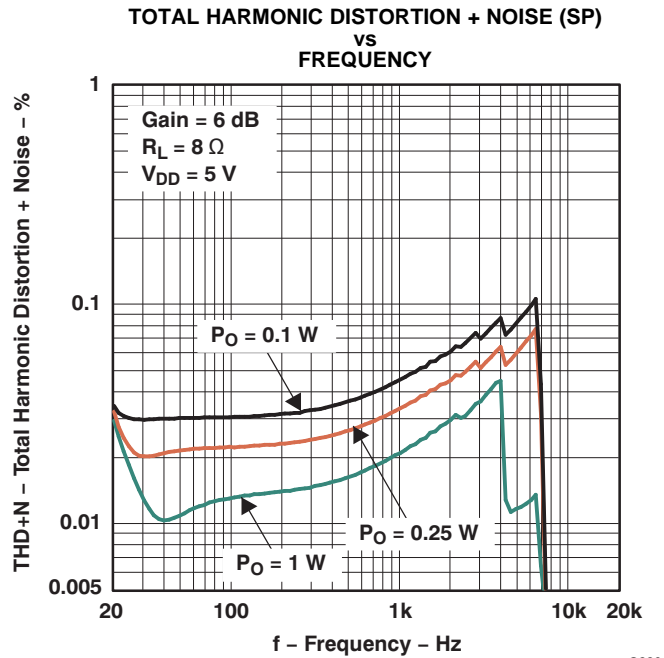


Figure 2.

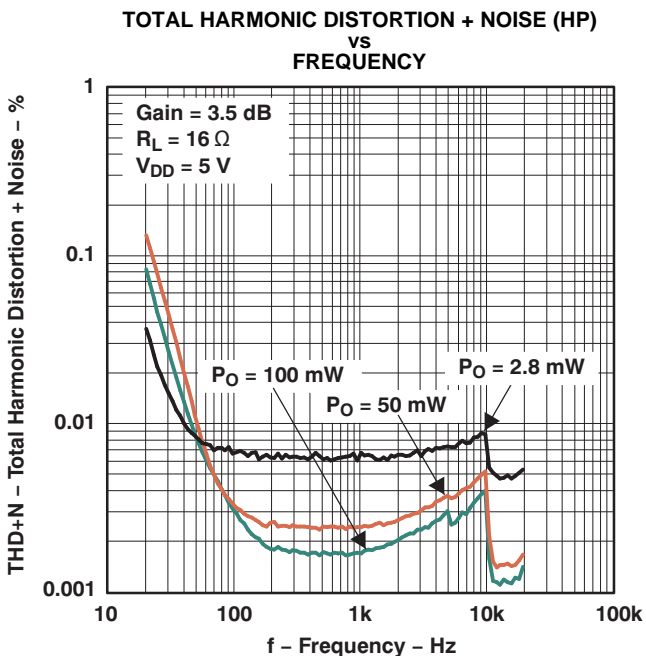


Figure 3.

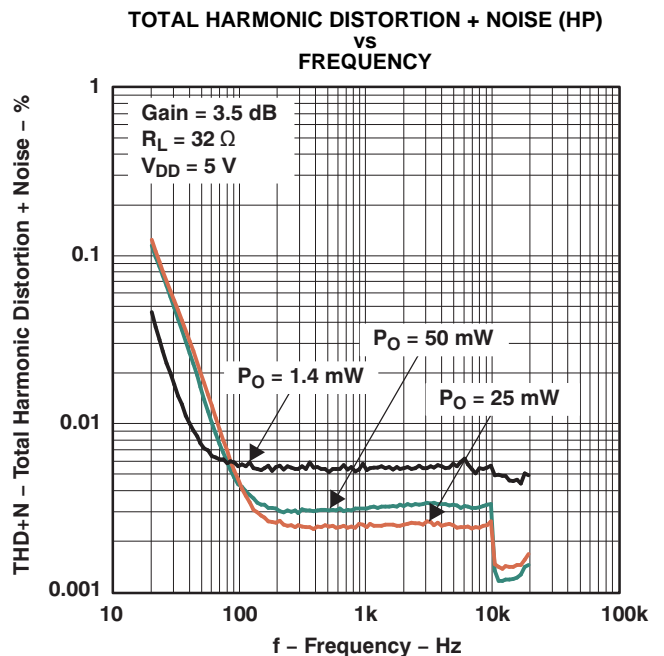


Figure 4.

TYPICAL CHARACTERISTICS (continued)

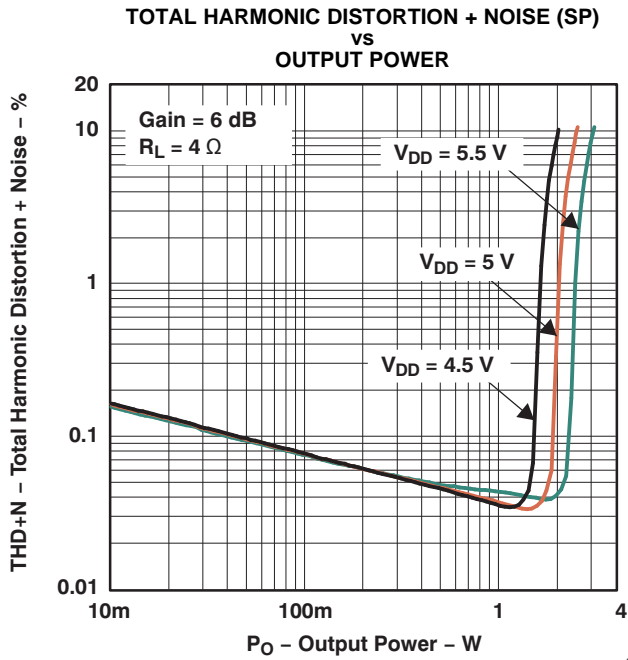


Figure 5.

G005

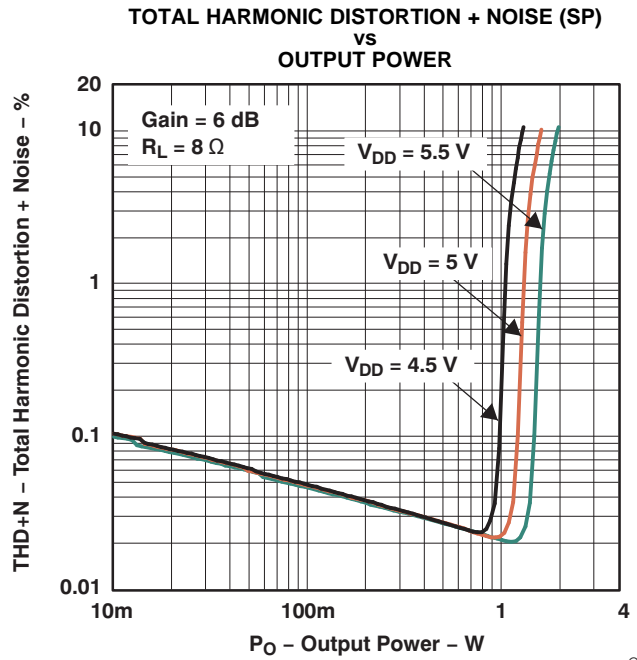


Figure 6.

G006

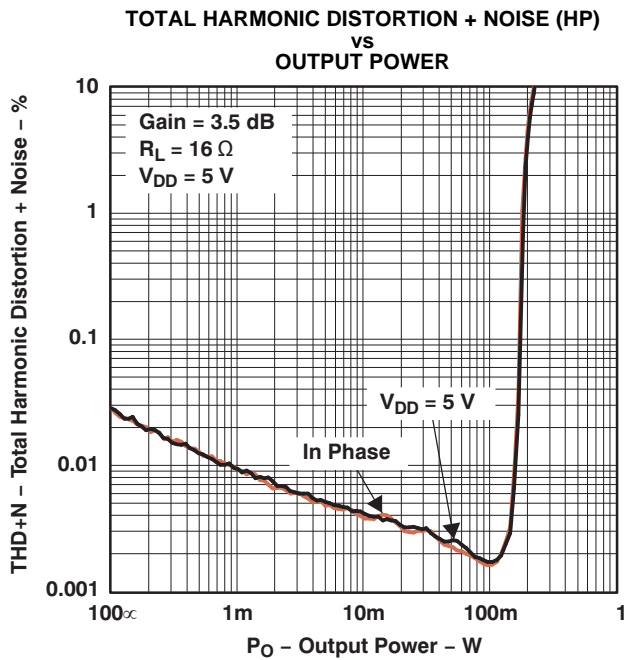


Figure 7.

G007

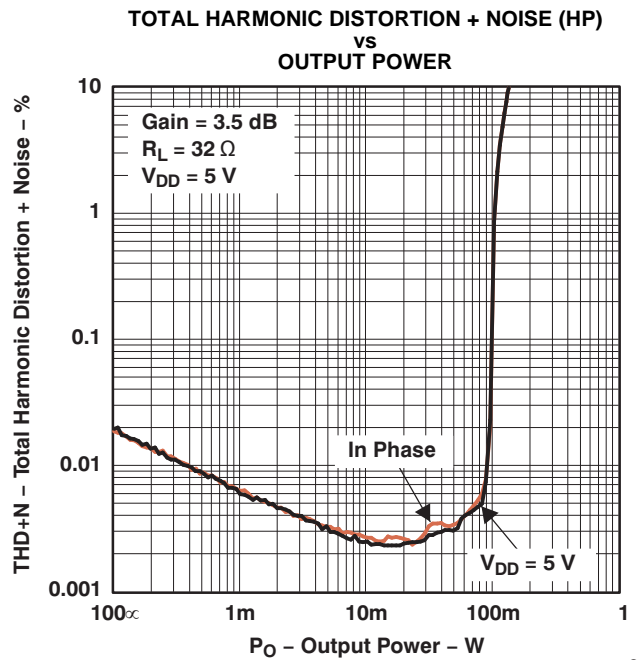


Figure 8.

G008



TYPICAL CHARACTERISTICS (continued)

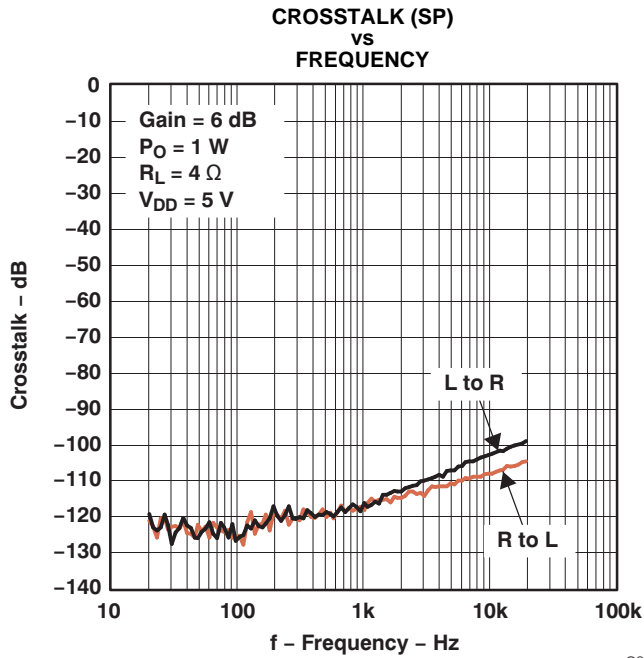


Figure 9.

G009

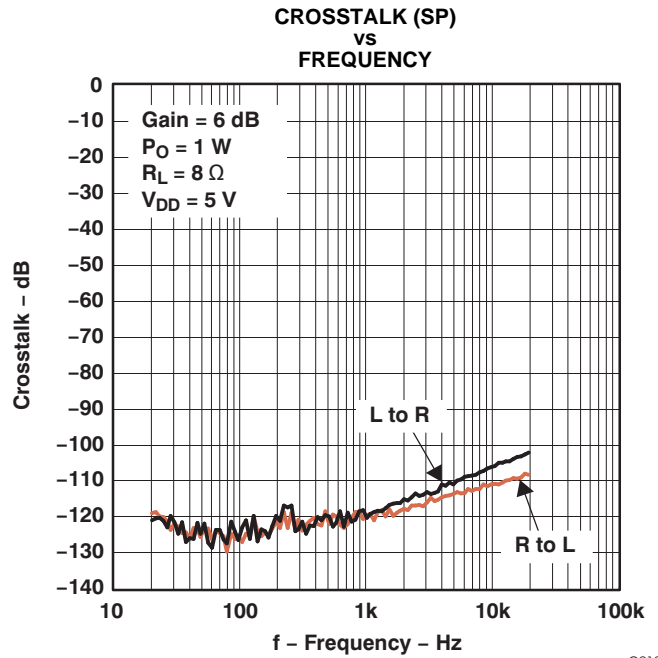


Figure 10.

G010

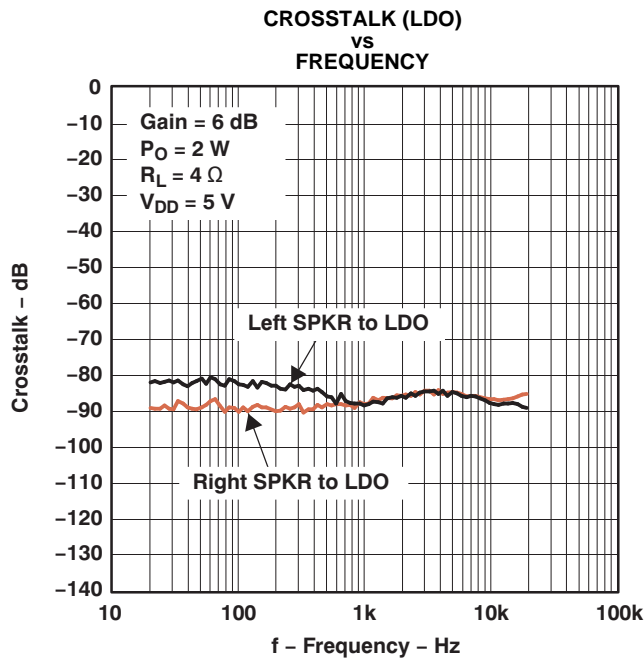


Figure 11.

G011

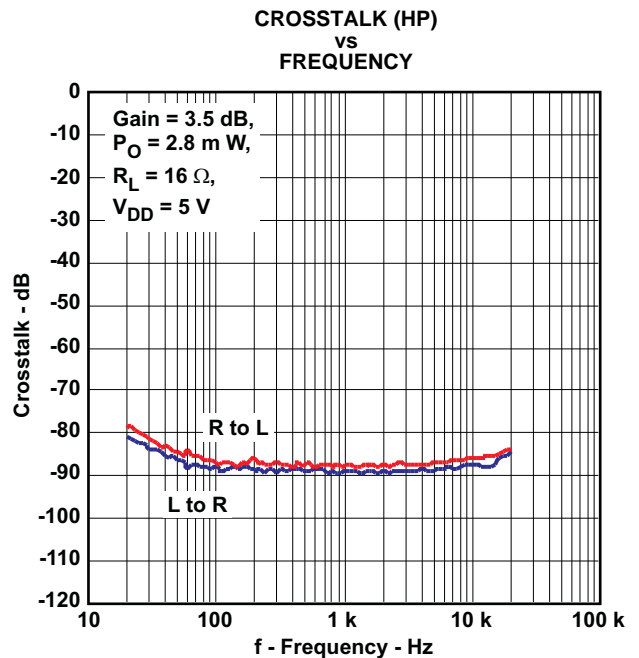


Figure 12.

TYPICAL CHARACTERISTICS (continued)

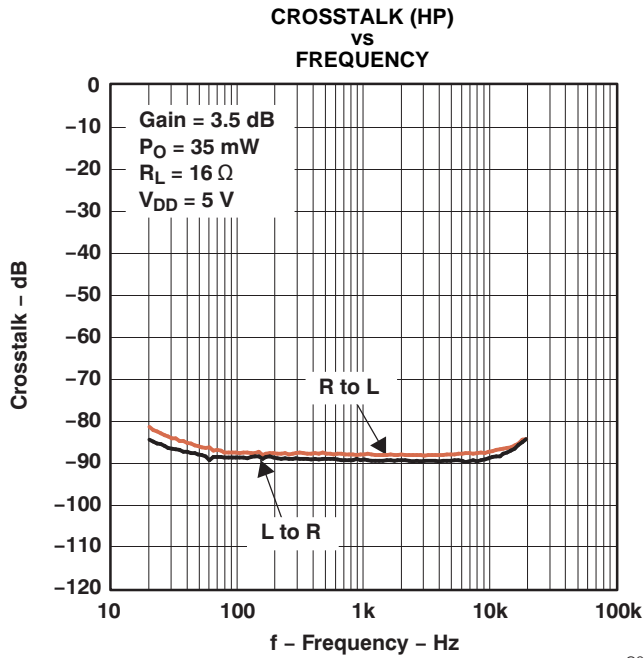


Figure 13.

G012

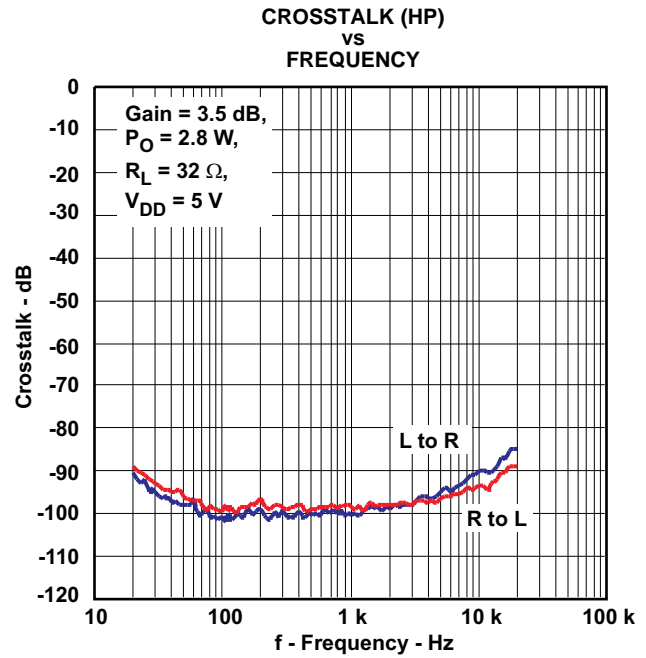


Figure 14.

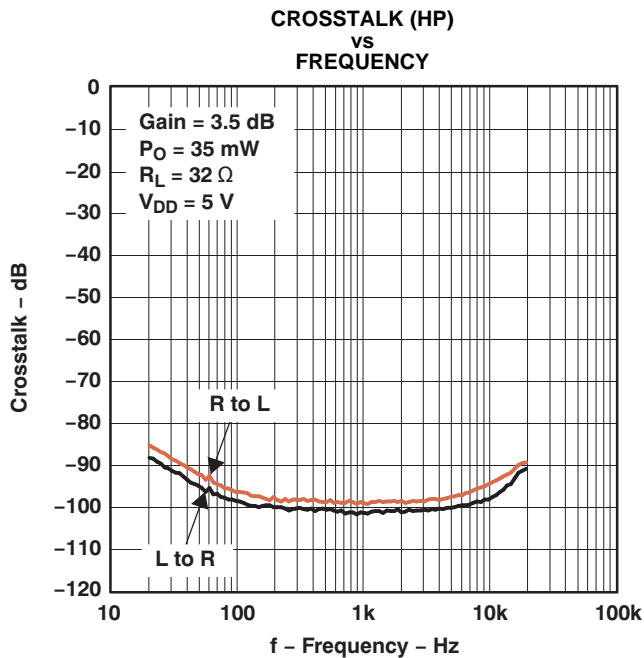


Figure 15.

G013

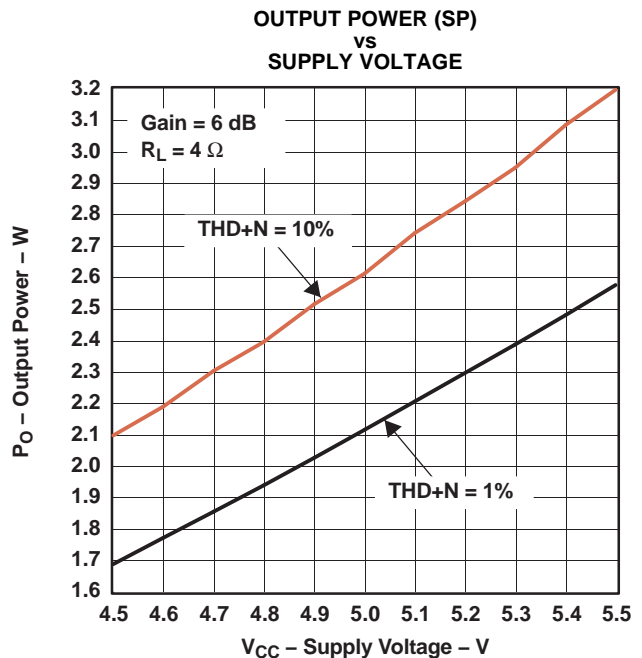


Figure 16.

G014

TYPICAL CHARACTERISTICS (continued)

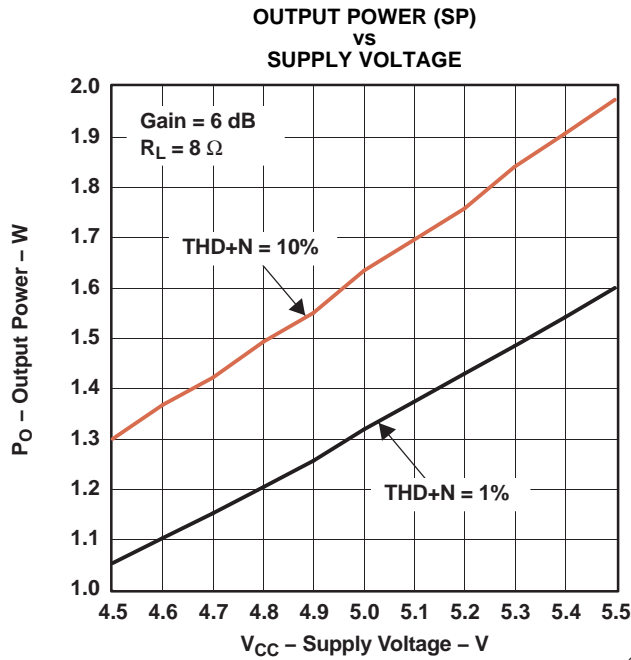


Figure 17.

G015

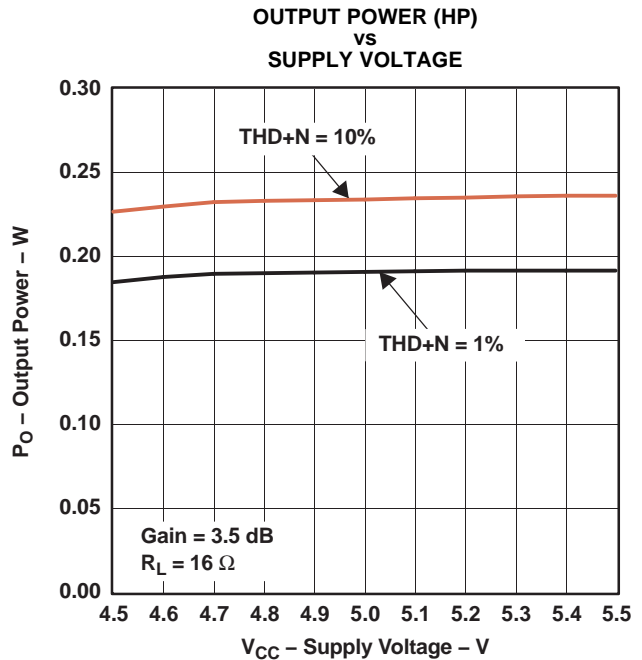


Figure 18.

G016

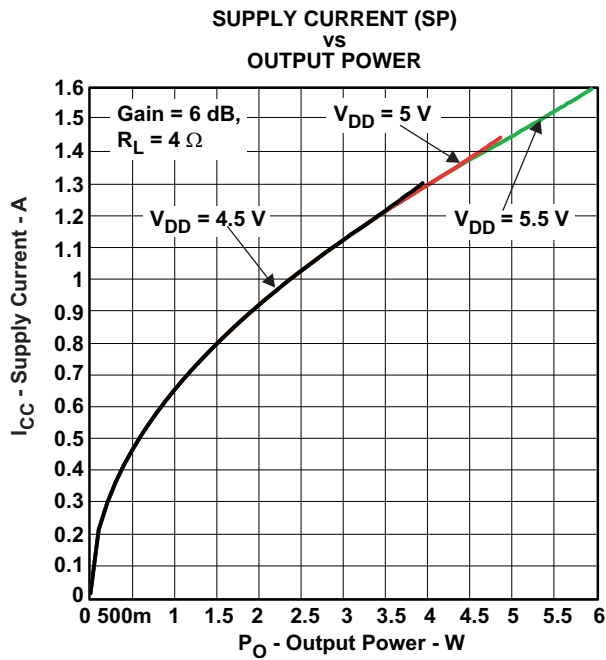


Figure 19.

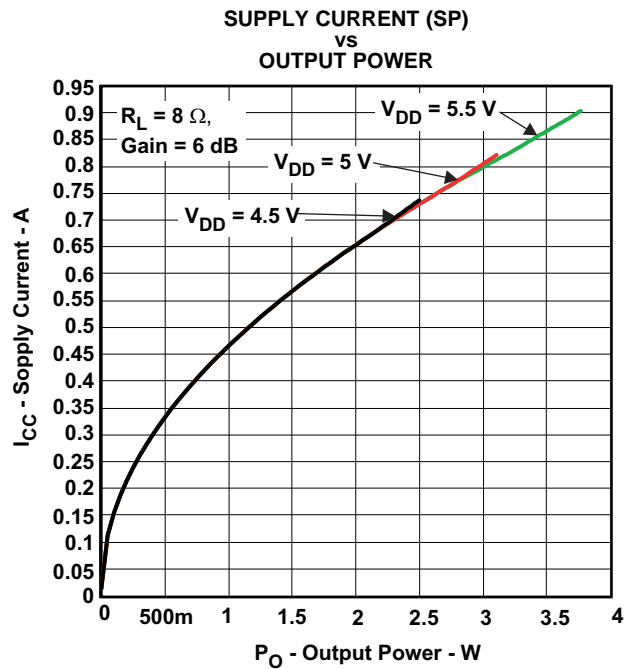


Figure 20.

TYPICAL CHARACTERISTICS (continued)

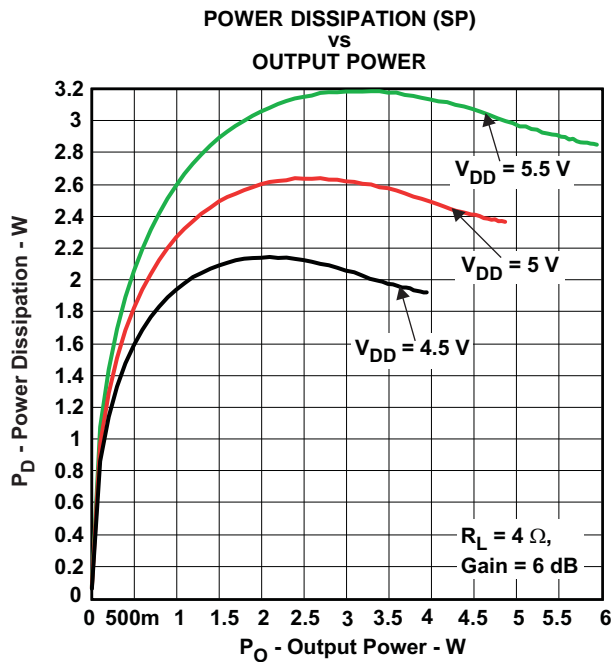


Figure 21.

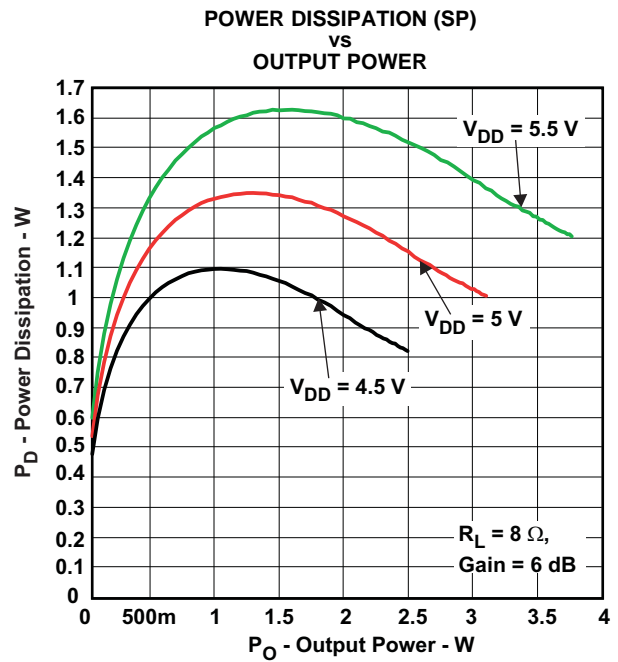


Figure 22.

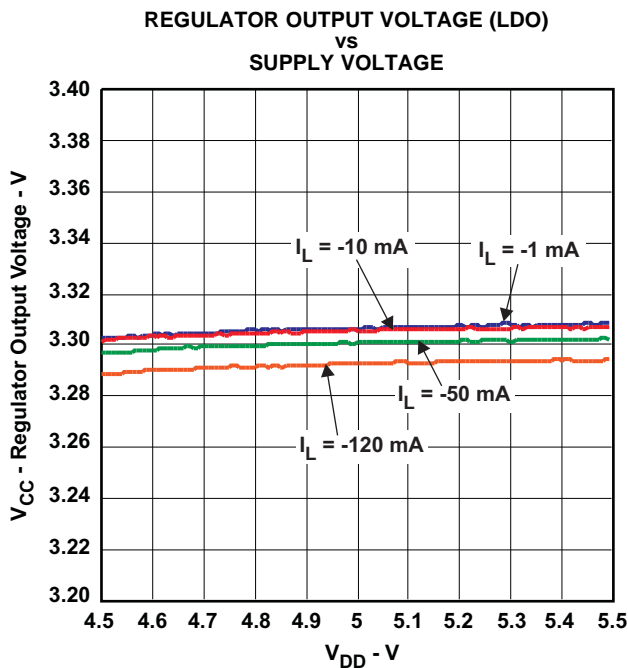


Figure 23.

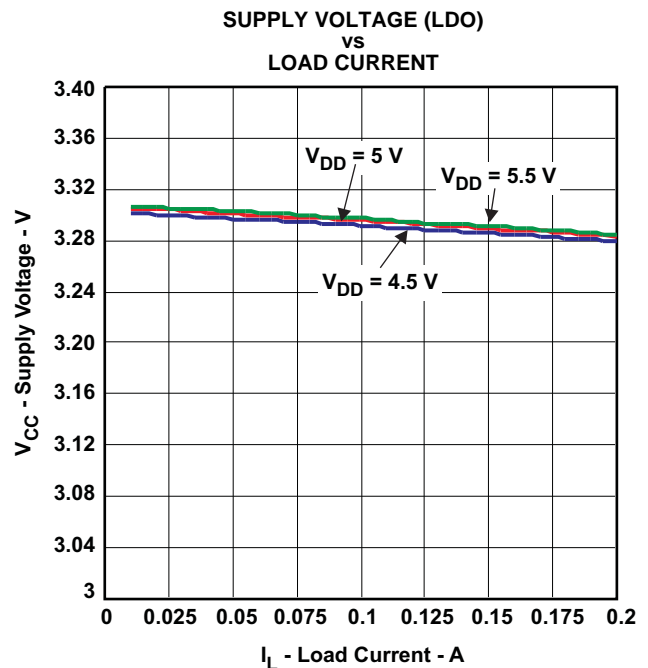


Figure 24.

TYPICAL CHARACTERISTICS (continued)

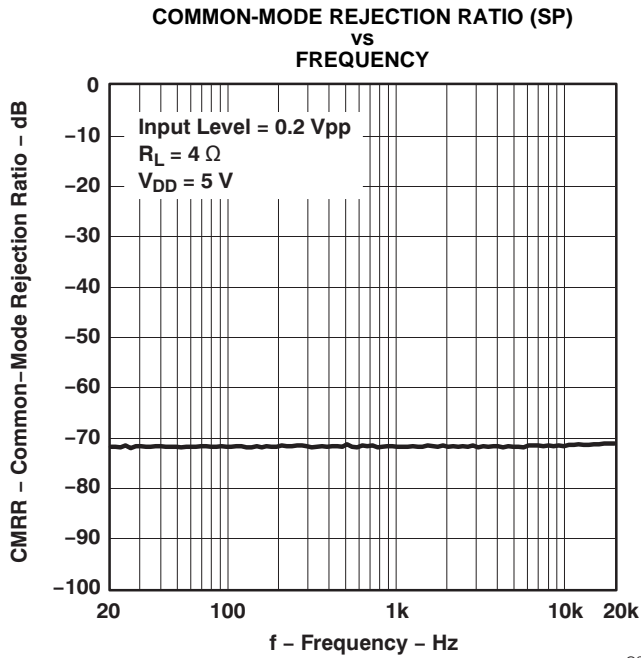


Figure 25.

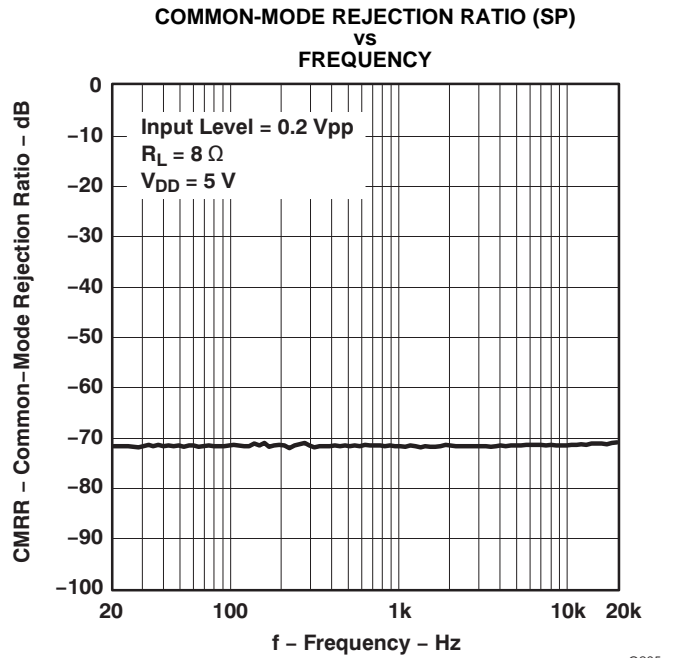


Figure 26.

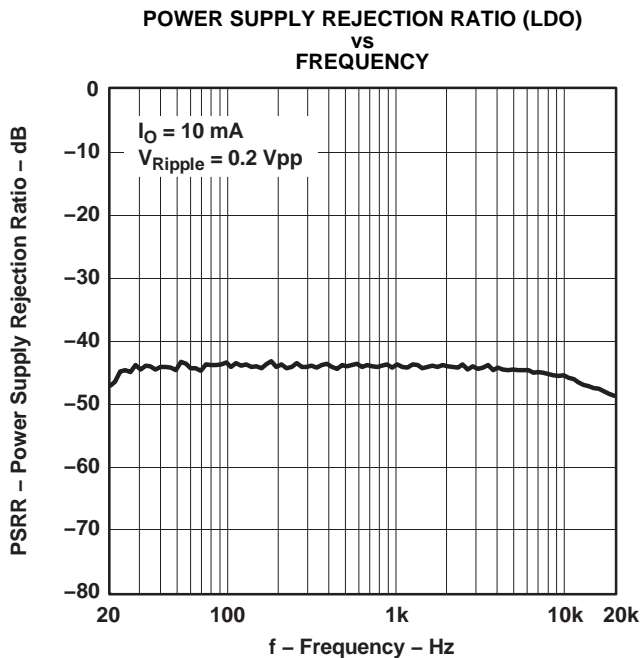


Figure 27.

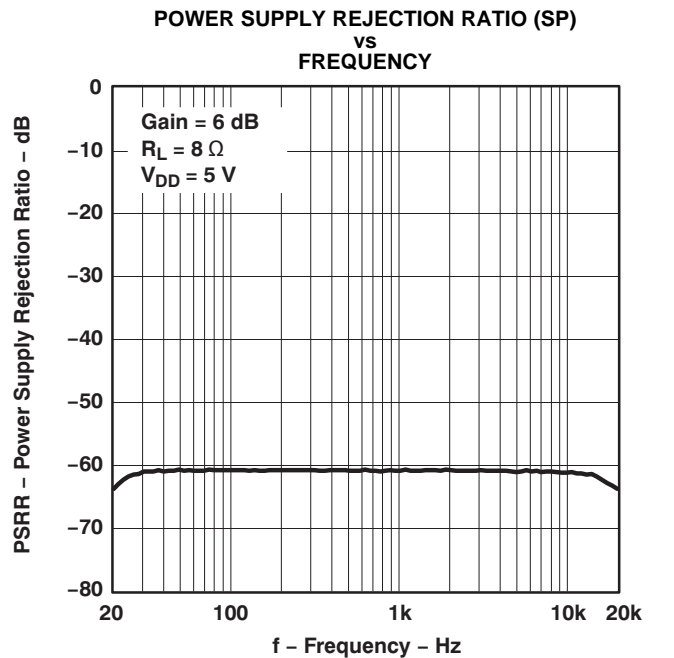


Figure 28.

TYPICAL CHARACTERISTICS (continued)

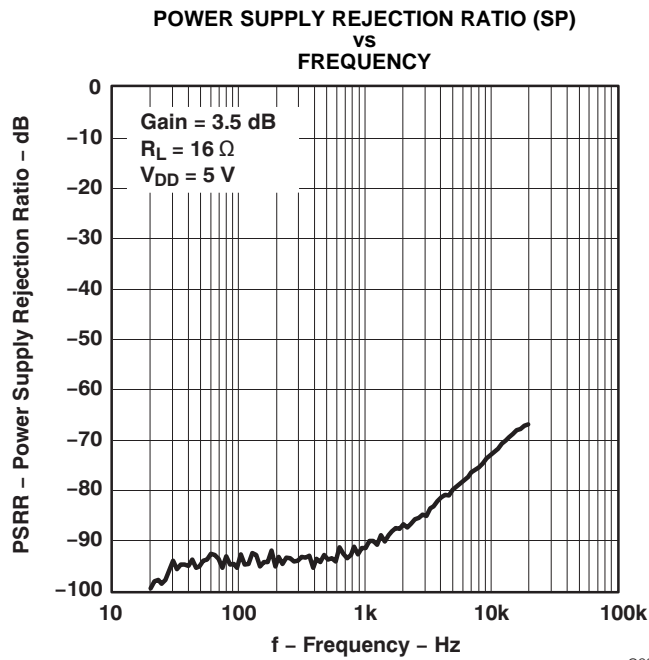


Figure 29.

G028

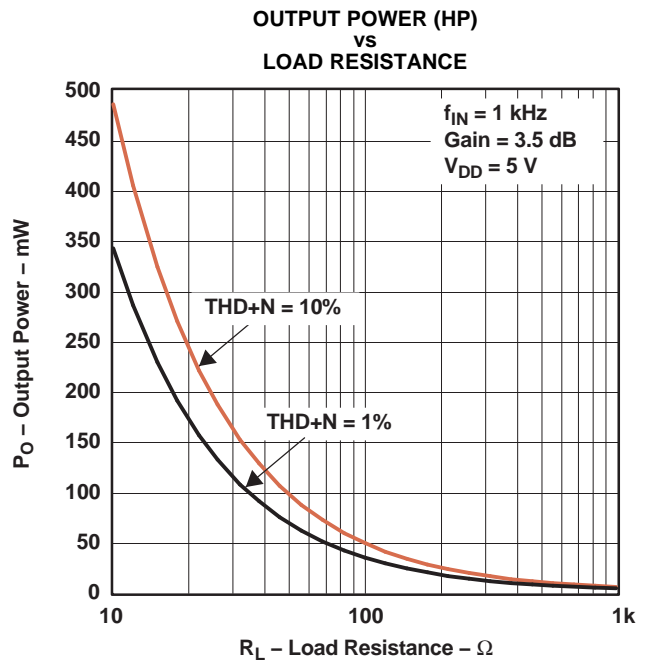


Figure 30.

G029

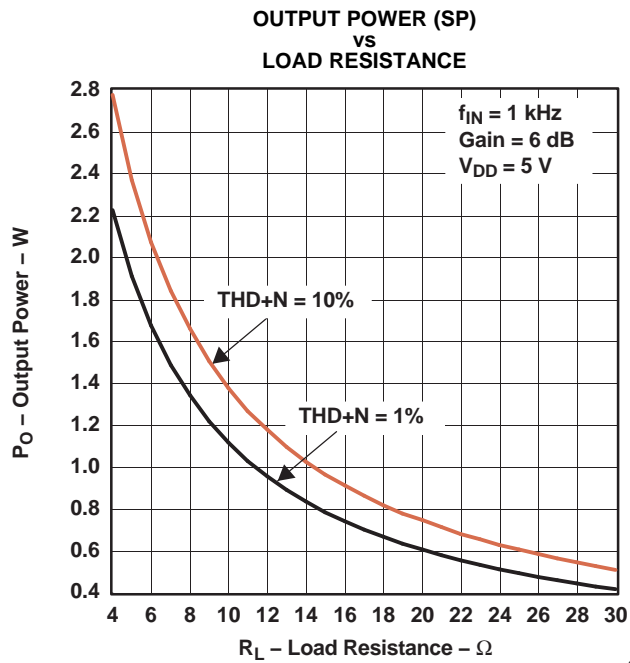


Figure 31.

G030

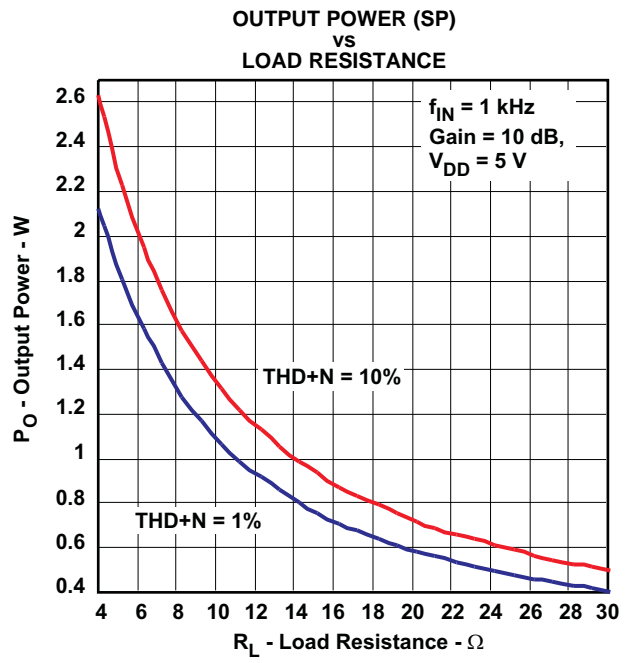
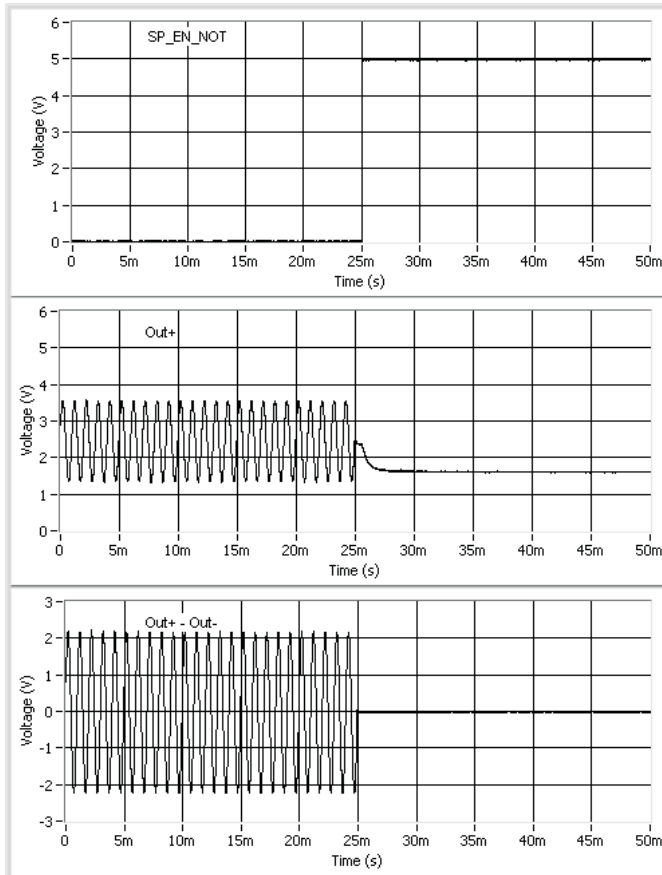


Figure 32.

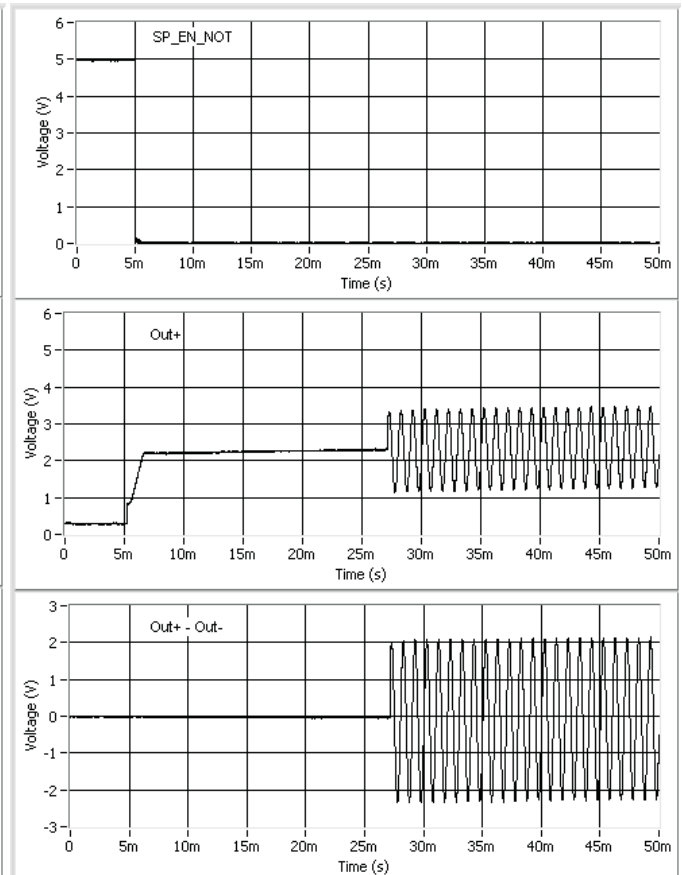
**TYPICAL CHARACTERISTICS (continued)**

**SPEAKER SHUTDOWN - 8 Ω - 10 dB**



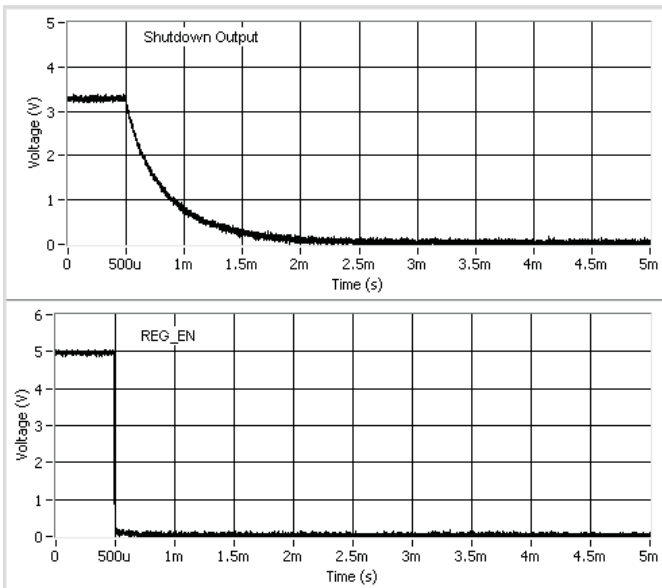
**Figure 33.**

**SPEAKER STARTUP - 8 Ω - 10 dB**



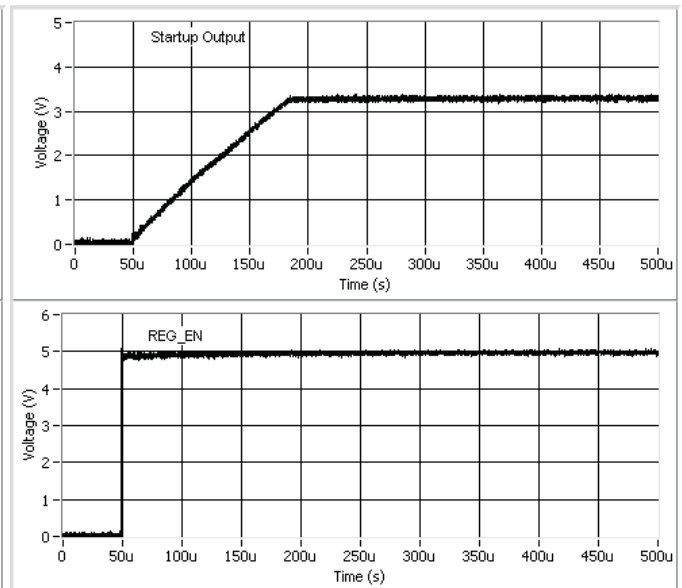
**Figure 34.**

**LDO SHUTDOWN - 120 mA**



**Figure 35.**

**LDO STARTUP - 120 mA**



**Figure 36.**

TYPICAL CHARACTERISTICS (continued)

HP SHUTDOWN - 32 Ω

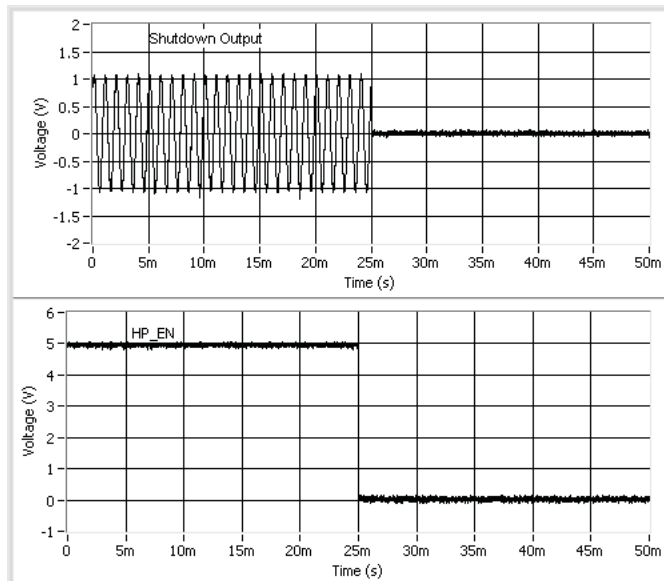


Figure 37.

HP STARTUP - 32 Ω

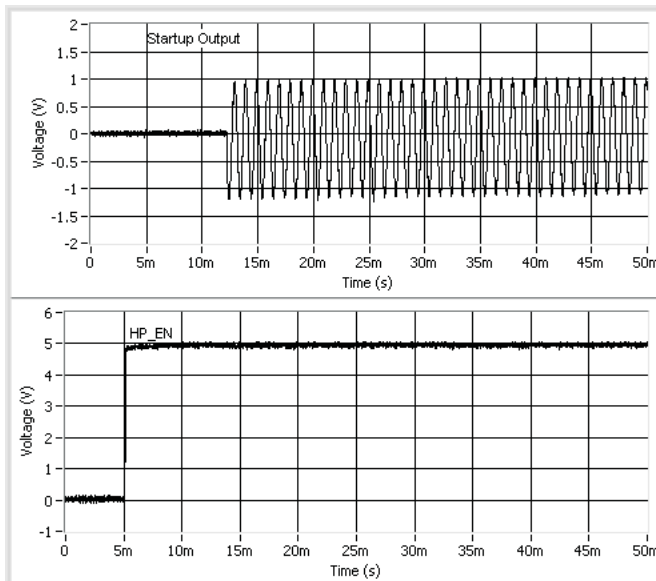
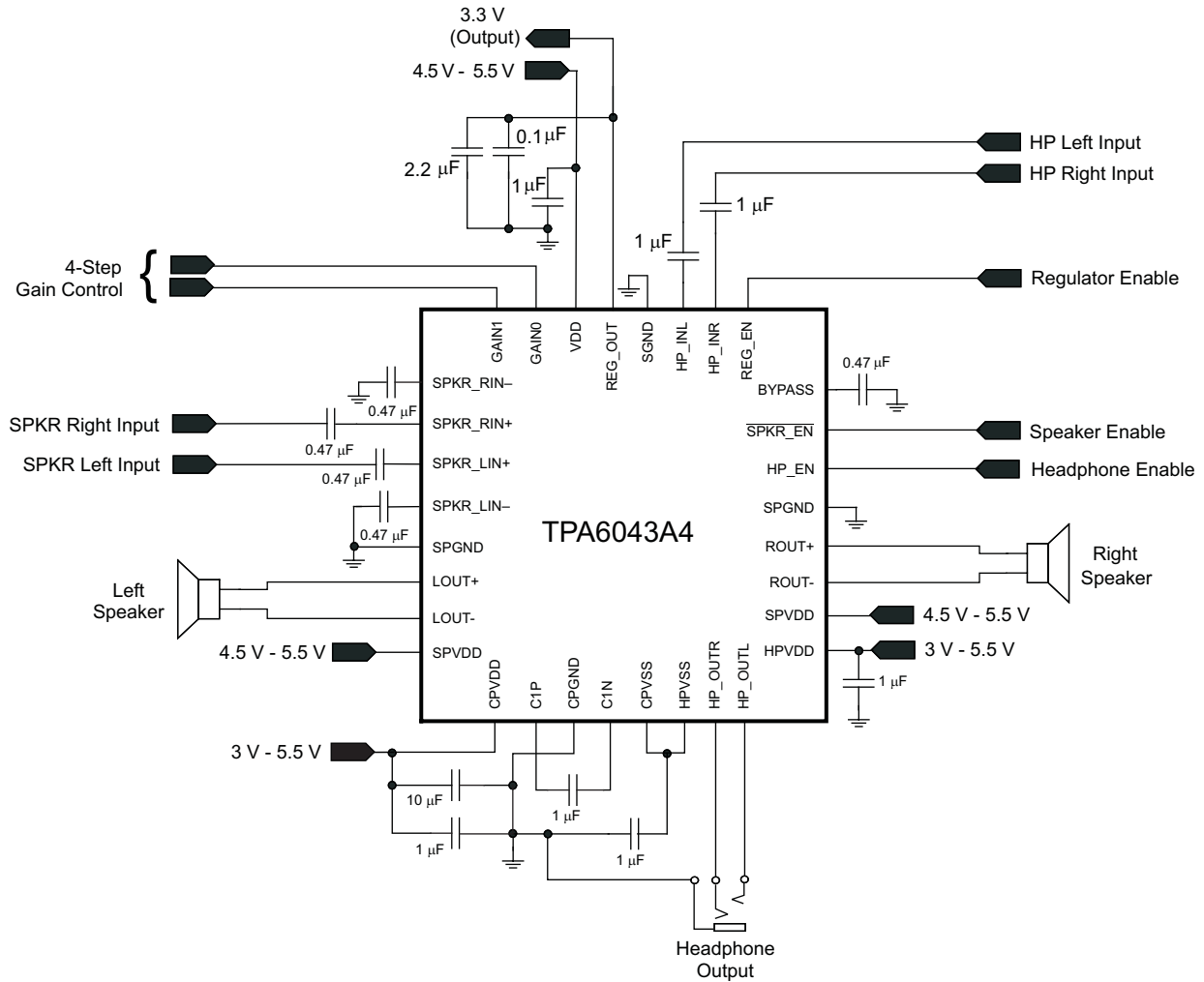


Figure 38.



**APPLICATION INFORMATION**



**Figure 39. Single-Ended Input Application Circuit**

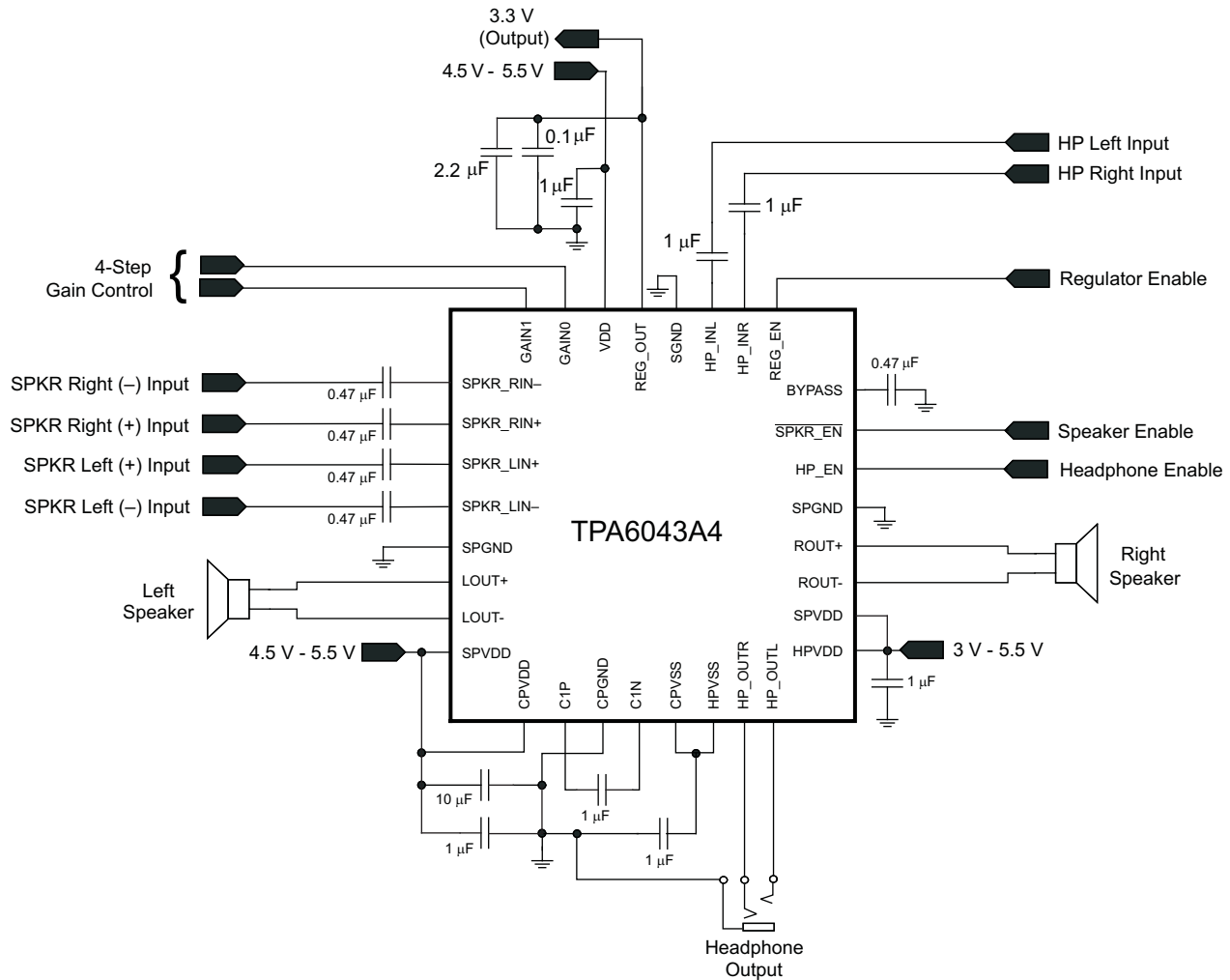


Figure 40. Differential Input Application Circuit

### Power Enable Modes

The TPA6043A4 allows disable of any or all of the main circuit blocks when not in use in order to reduce operating power to an absolute minimum. The  $\overline{\text{SPKR\_EN}}$  control can be used to disable the speaker amplifier while the  $\text{HP\_EN}$  can be used separately to turn off the headphone amplifier. The LDO also has an independent power control,  $\text{REG\_EN}$ . With all circuit blocks disabled, the supply current in shutdown mode is only 5  $\mu\text{A}$ . See the General DC Electrical Characteristics for operating currents with each circuit block operating independently.

### Speaker Amplifier Description

The speaker amplifier is capable of driving 2 W/ch of continuous RMS power into a 4- $\Omega$  load at 5 V. An internal 4-step control allows variation of the gain from 6 dB to 21.6 dB.

### Fully Differential Amplifier

The TPA6043A4 speaker amplifier is a fully differential amplifier with differential inputs and outputs. The fully differential architecture consist of a differential amplifier and a common mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode voltage at the output is biased around  $V_{\text{DD}}/2$  regardless of the common-mode voltage at the input.

One of the primary advantages of the fully differential amplifier is improved RF immunity. GSM handsets save power by turning on and off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked up on input and output traces. The fully differential amplifier cancels the signal and others of this type much better than typical audio amplifiers.

### Gain Setting via GAIN0 and GAIN1 Inputs

The gain of the TPA6043A4 is set by two terminals, GAIN0 and GAIN1. The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance ( $Z_i$ ) to vary as a function of the gain setting.

Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (k $\Omega$ )
		TYPICAL	TYPICAL
0	0	6	108
0	1	10	78
1	0	15.6	46
1	1	21.6	25

### Input Capacitor, $C_i$

The input capacitor allows the amplifier to bias the input signal to the proper dc level for proper operation. In this case, the input capacitor,  $C_i$ , and the input impedance of the amplifier,  $R_i$ , form a high-pass filter with the corner frequency determined in Equation 1. Figure 41 shows how the input capacitor and the input resistor within the amplifier interact.

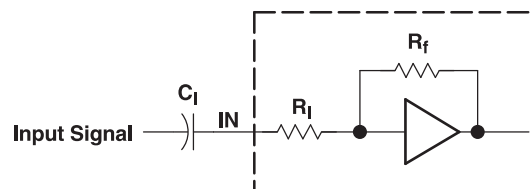
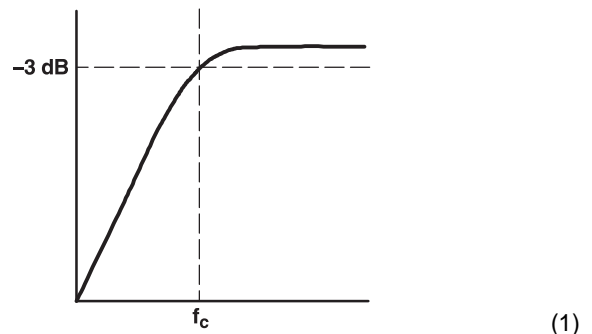


Figure 41. Input Resistor and Input Capacitor

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_i C_i} \quad (1)$$



The value of  $C_i$  is important to consider as it directly affects the low-frequency, or bass, performance of the circuit. Furthermore, the input impedance changes with a change in volume. The higher the volume, the lower the input impedance is. To determine the appropriate capacitor value, reconfigure Equation 1 into Equation 2. The value of the input resistor,  $R_i$ , can be determined from Equation 2.

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

Low-leakage tantalum or ceramic capacitors are recommended. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at  $V_{CC}/2$ , which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in each specific application. Recommended capacitor values are between 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$ .

**Windows Vista™ Premium Mode Specifications**

Device Type	Requirement	Windows Premium Mobile Vista Specifications	TPA6043A4 Typical Performance
Analog Speaker Output Jack ( $R_L = 8\Omega$ , FS = 0.707 Vrms)	THD+N	$\leq -65$ dB FS [20 Hz, 20 kHz]	-74 dB FS[20 Hz, 20 kHz]
	Dynamic Range with Signal Present	$\leq -80$ dB FS A-Weight	-89 dB FS A-Weight
	Line Output Crosstalk	$\leq -60$ dB [20 Hz, 20 kHz]	-100 dB [20 Hz, 20 kHz]
Analog Headphone Out Jack ( $R_L = 32\Omega$ , FS = 0.300 Vrms)	THD+N	$\leq -45$ dB FS [20 Hz, 20 kHz]	-81 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	$\leq -80$ dB FS A-Weight	-100 dB FS A-Weight
	Headphone Output Crosstalk	$\leq -60$ dB [20 Hz, 20 kHz]	-82 dB [20 Hz, 20 kHz]

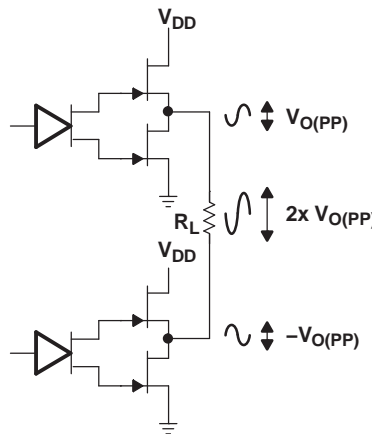
**Bridge-Tied Load Versus Single-Ended Mode**

Figure 42 shows a Class-AB audio power amplifier (APA) in a bridge-tied-load (BTL) configuration. The TPA6043A4 speaker amplifier consists of two Class-AB differential amplifiers per channel driving the positive and negative terminals of the load. Specifically, differential drive means that as one side of the amplifier (the positive terminal, for example) is slewing up, the other side is slewing down, and vice versa. This doubles the voltage swing across the load as opposed to a ground-referenced load, or a single-ended load. Power is proportional to the square of the voltage. Plugging 2x VO(PP) into the power equation yields 4X the output power from the same supply rail and load impedance as would have been obtained with a ground-referenced load (see Equation 3).

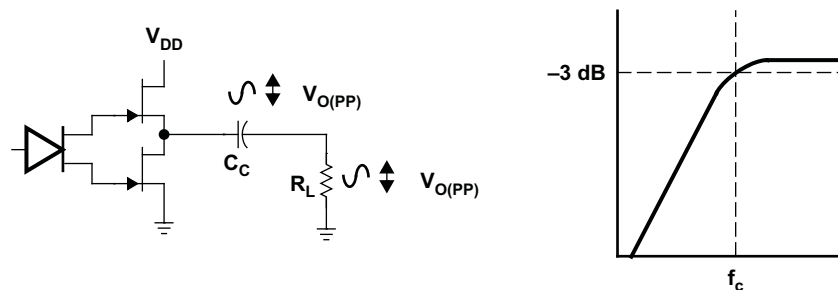
$$V_{(RMS)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$Power = \frac{V_{(RMS)}^2}{R_L}$$

(3)



**Figure 42. Differential Output Configuration**



**Figure 43. Single-Ended Configuration and Frequency Response**

Bridge-tying the outputs in a typical computer audio, LCD TV, or multimedia LCD monitor application drastically increases output power. For example, if an amplifier in a single-ended configuration was capable of outputting a maximum of 250 mW for a given load with a supply voltage of 12 V, then that same amplifier would be able to output 1 W of power in a BTL configuration with the same supply voltage and load. In addition to the increase in output power, the BTL configuration does not suffer from the same low-frequency issues that plague the single-ended configuration. In a BTL configuration, there is no need for an output capacitor to block dc, so no unwanted filtering occurs. In addition, the BTL configuration saves money and space, as the dc-blocking capacitors needed for single-ended operation are large and expensive. For example, with an 8-Ω load in SE operation, the user needs a 1000-μF capacitor to obtain a cutoff frequency below 20 Hz. This capacitor is expensive and large.

## Headphone Amplifier Description

The headphone amplifier has a fixed gain of  $-1.5$  V/V. It uses single-ended (SE) inputs. The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath™ amplifier requires no output dc blocking capacitors and does not place any voltage on the sleeve. The block diagram and waveform of [Figure 44](#) illustrate the ground-referenced headphone architecture. This is the architecture of the TPA6043A4.

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely clipped, and large amounts of dc current rush through the headphones, potentially damaging them. The left-side drawing in [Figure 44](#) illustrates the conventional headphone amplifier connection to the headphone jack and output signal.

DC blocking capacitors are often large in value. The headphone speakers (typical resistive values of 16 Ω or 32 Ω) combine with the dc blocking capacitors to form a high-pass filter. [Equation 4](#) shows the relationship between the load impedance ( $R_L$ ), the capacitor ( $C_O$ ), and the cutoff frequency ( $f_c$ ).

$$f_c = \frac{1}{2\pi R_L C_O} \quad (4)$$

$C_O$  can be determined using [Equation 5](#), where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \quad (5)$$

If  $f_c$  is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

Two different headphone amplifier applications are available that allow for the removal of the output dc blocking capacitors. The capacitor-less amplifier architecture is implemented in the same manner as the conventional amplifier with the exception of the headphone jack shield pin. This amplifier provides a reference voltage, which is connected to the headphone jack shield pin. This is the voltage on which the audio output signals are centered. This voltage reference is half of the amplifier power supply to allow symmetrical swing of the output voltages. Do not connect the shield to any GND reference, or large currents will result. The scenario can happen if, for example, an accessory other than a floating GND headphone is plugged into the headphone connector. See the second block diagram and waveform in [Figure 44](#).

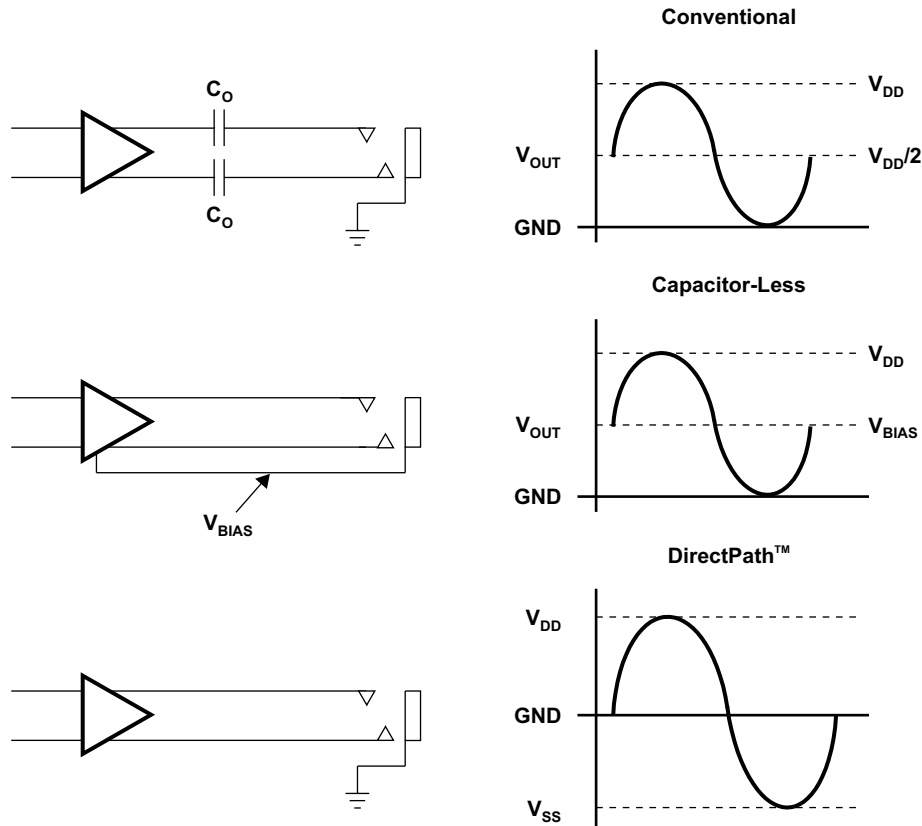


Figure 44. Amplifier Applications

### Input-Blocking Capacitors

DC input-blocking capacitors block the dc portion of the audio source and allow the inputs to properly bias. Maximum performance is achieved when the inputs of the TPA6043A4 are properly biased. Performance issues such as pop are optimized with proper input capacitors.

The dc input-blocking capacitors can be removed, provided the inputs are connected differentially and within the input common-mode range of the amplifier, the audio signal does not exceed  $\pm 3$  V, and pop performance is sufficient.

$C_{IN}$  is a theoretical capacitor used for mathematical calculations only. Its value is the series combination of the dc input-blocking capacitors,  $C_{(DCINPUT-BLOCKING)}$ . Use Equation 6 to determine the value of  $C_{(DCINPUT-BLOCKING)}$ . For example, if  $C_{IN}$  is equal to 0.22  $\mu$ F, then  $C_{(DCINPUT-BLOCKING)}$  is equal to about 0.47  $\mu$ F.

$$C_{IN} = \frac{1}{2} C_{(DCINPUT-BLOCKING)} \tag{6}$$

The two  $C_{(DCINPUT-BLOCKING)}$  capacitors form a high-pass filter with the input impedance of the TPA6043A4. Use Equation 6 to calculate  $C_{IN}$ , then calculate the cutoff frequency using  $C_{IN}$  and the differential input impedance of the TPA6043A4,  $R_{IN}$ , using Equation 7. Note that the differential input impedance changes with gain. See Figure 40 for input impedance values. The frequency and/or capacitance can be determined when one of the two values are given.

$$f_{C_{IN}} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi f_{C_{IN}} R_{IN}} \quad (7)$$

If a high-pass filter with a -3-dB point of no more than 20 Hz is desired over all gain settings, the minimum impedance would be used in the Equation 7. The minimum input impedance for TPA6043A4 is 20 kΩ. The capacitor value by Equation 7 would be 0.399 μF. However, this is  $C_{IN}$ , and the desired value is for  $C_{(DCINPUT-BLOCKING)}$ . Multiplying  $C_{IN}$  by 2 yields 0.80 μF, which is close to the standard capacitor value of 1 μF. Place 1-μF capacitors at each input terminal of the TPA6043A4 to complete the filter.

### Charge Pump Flying Capacitor and CPVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The CPVSS capacitor must be at least equal to the flying capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1 μF is typical.

### Decoupling Capacitors

The TPA6043A4 is a DirectPath™ headphone amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are as low as possible. To filter high-frequency transients, spikes, and digital hash on the power line, use good low equivalent-series-resistance (ESR) ceramic capacitors, typically 1 μF. Find the smallest package possible, and place as close as possible to the device  $V_{DD}$  lead. Placing the decoupling capacitors close to the TPA6043A4 is important for the performance of the amplifier. Use a 10 μF or greater capacitor near the TPA6043A4 to filter lower frequency noise signals; however, the high PSRR of the TPA6043A4 makes the 10-μF capacitor unnecessary in most applications.

### Midrail Bypass Capacitor, $C_{BYPASS}$

The midrail bypass capacitor,  $C_{(BYPASS)}$ , has several important functions. During start-up or recovery from shutdown mode,  $C_{BYPASS}$  determines the rate at which the amplifier starts up. A 1-μF capacitor yields a start-up time of approximately 30 ms.  $C_{BYPASS}$  also reduces the noise coupled into the output signal by the power supply. This improves the power supply ripple rejection (PSRR) of the amplifier. Ceramic or polyester capacitors with low ESR and values in the range of 0.47 μF to 1 μF are recommended.

### LOW DROPOUT REGULATOR (LDO) DESCRIPTION

The TPA6043A4 contains a 3.3-V output low dropout regulator (LDO) capable of providing a maximum of 120 mA with a drop of less than 150 mV from the 5-V supply. This can be used to power an external CODEC. A 10-μF decoupling capacitor is recommended at the output of the LDO, as well as 0.1-μF capacitor to filter high-frequency noise from the supply line.

### LAYOUT RECOMMENDATIONS

Solder the exposed thermal pad (metal pad on the bottom of the part) on the TPA6043A4 QFN package to a pad on the PCB.

It is important to keep the TPA6043A4 external components close to the body of the amplifier to limit noise pickup. One should lay out the differential input leads symmetrical and close together to take advantage of the inherent common mode rejection of the TPA6043A4. The layout of the TPA6043A4 evaluation module (EVM) is a good example of component placement, and the layout files are available at [www.ti.com](http://www.ti.com).

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6043A4RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA 6043A4	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6043A4RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6043A4RHBR	VQFN	RHB	32	3000	356.0	356.0	35.0

## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

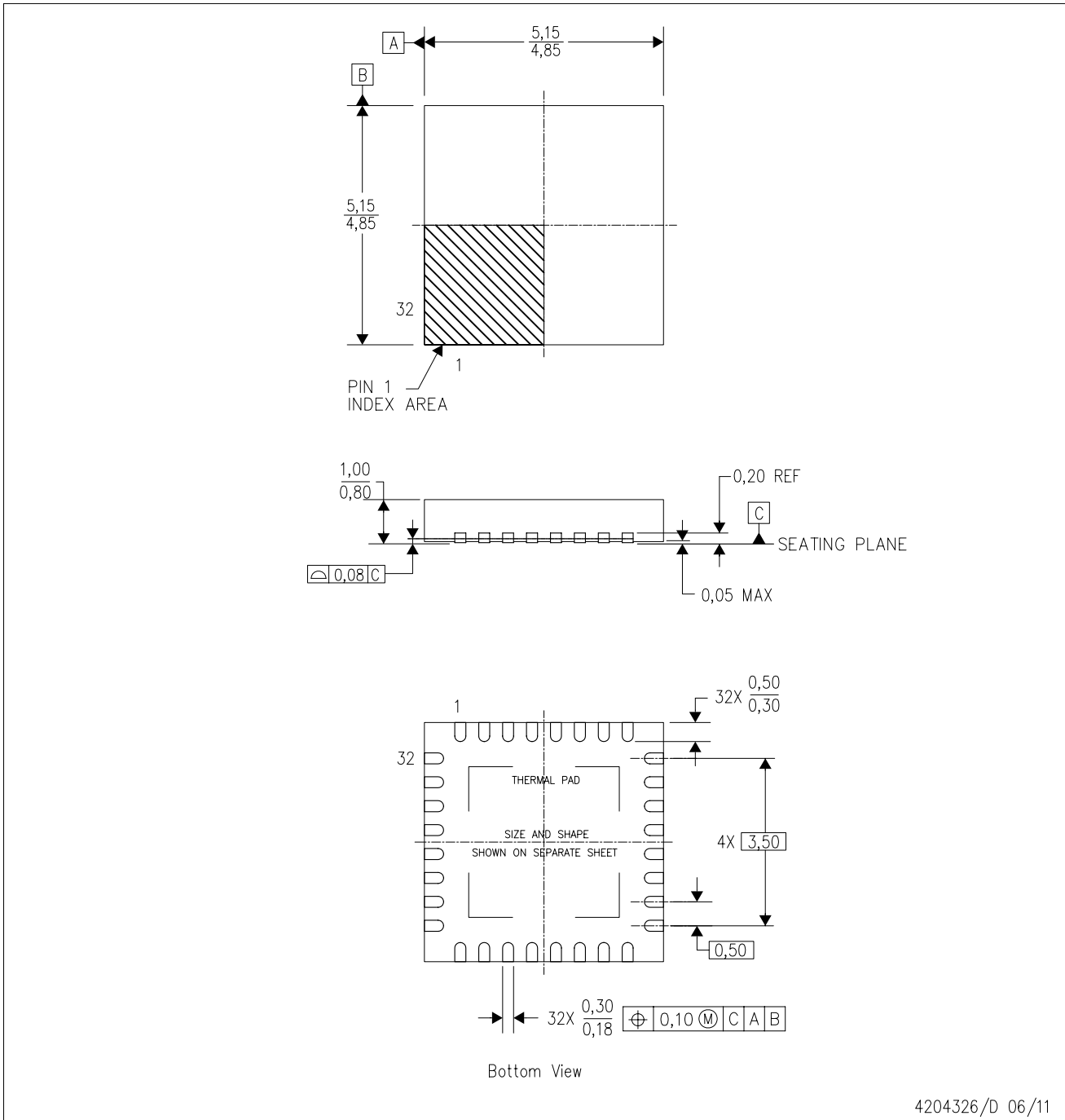


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

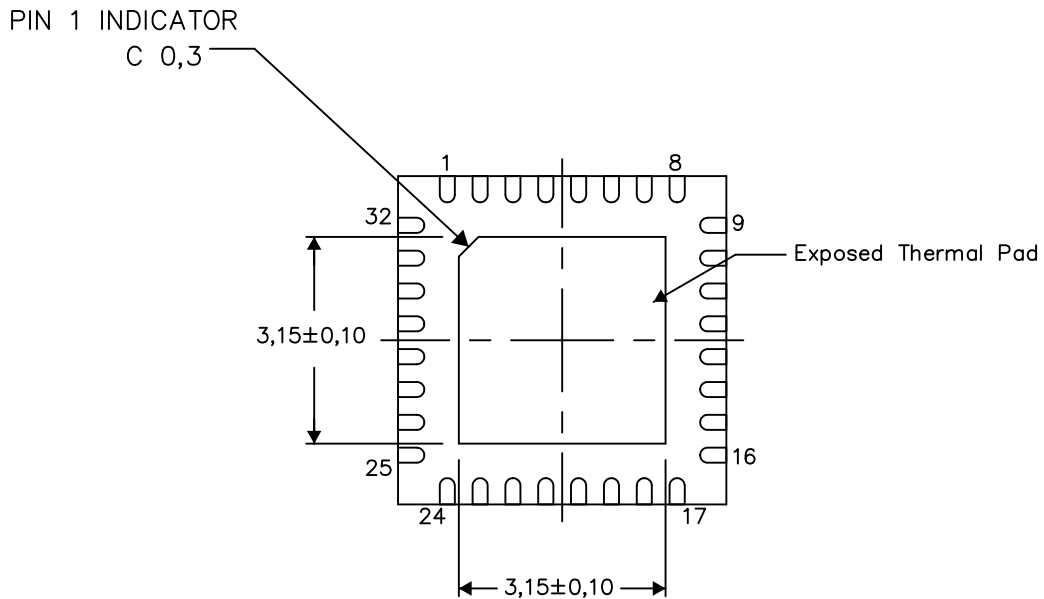
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



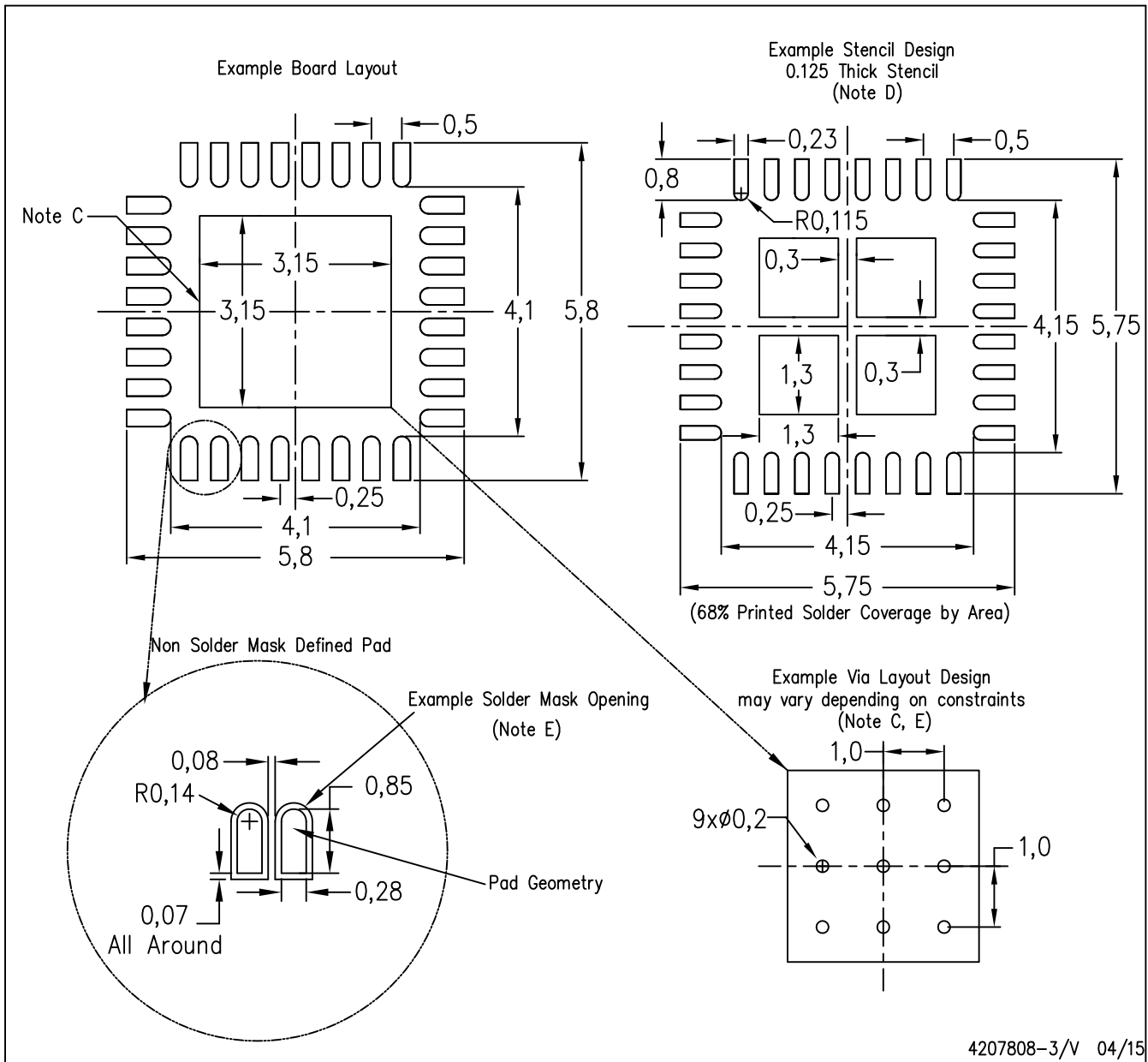
Exposed Thermal Pad Dimensions

4206356-3/AC 05/15

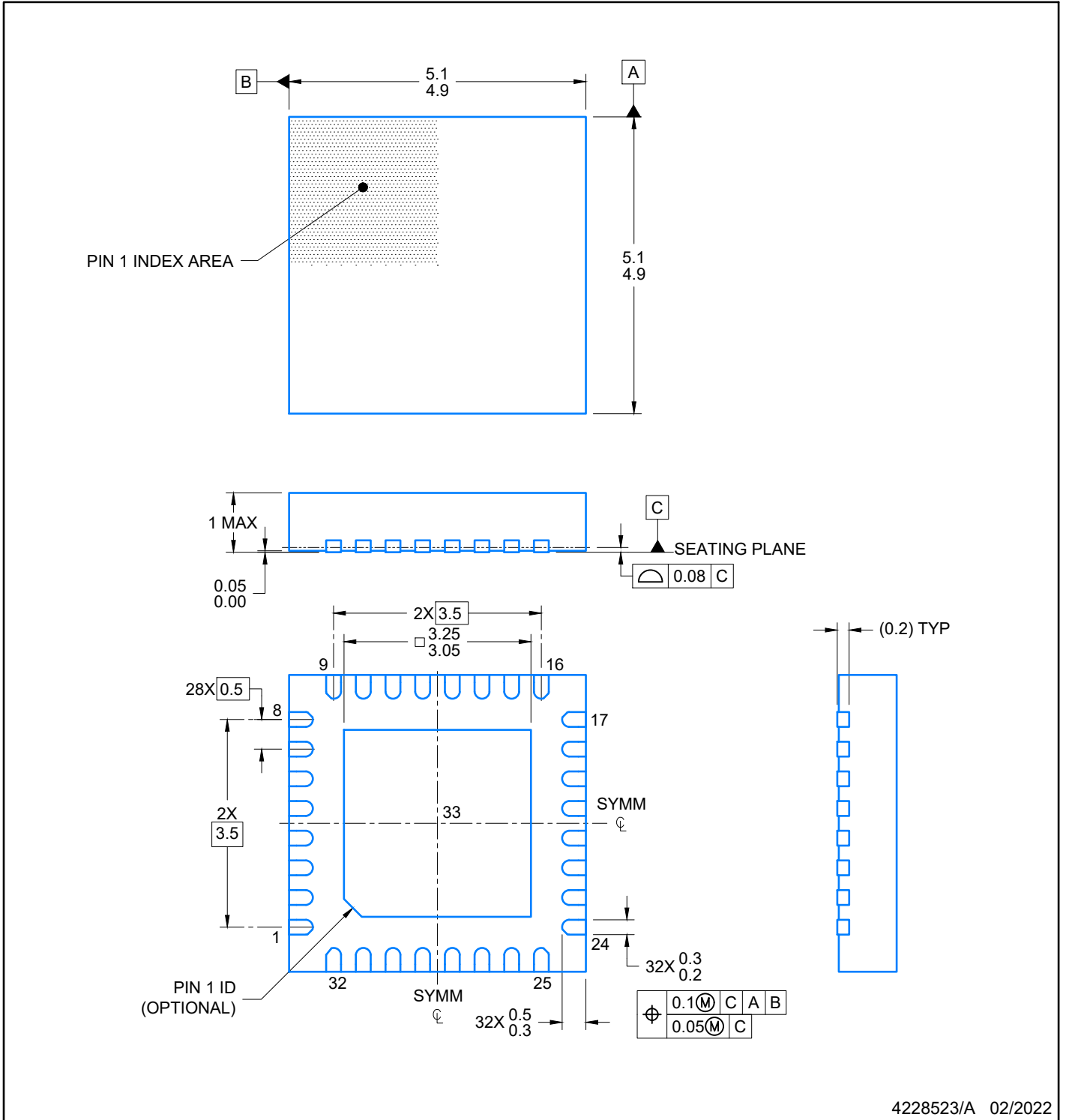
NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



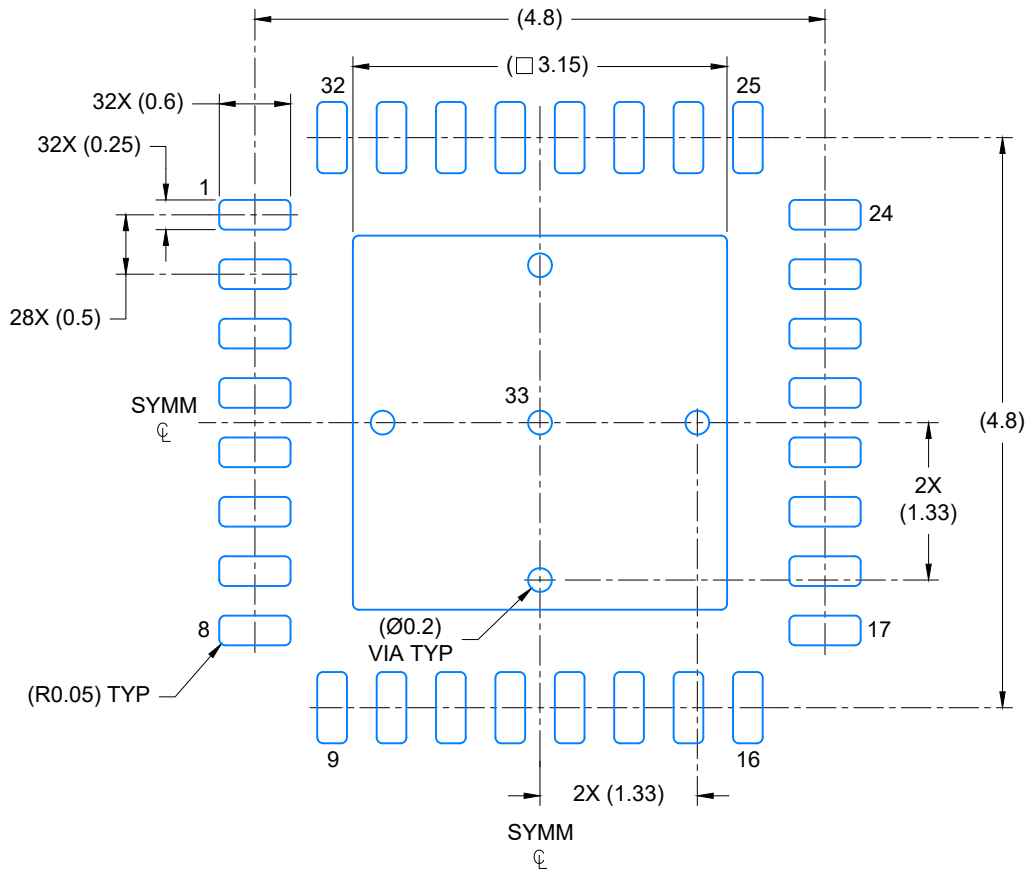
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.



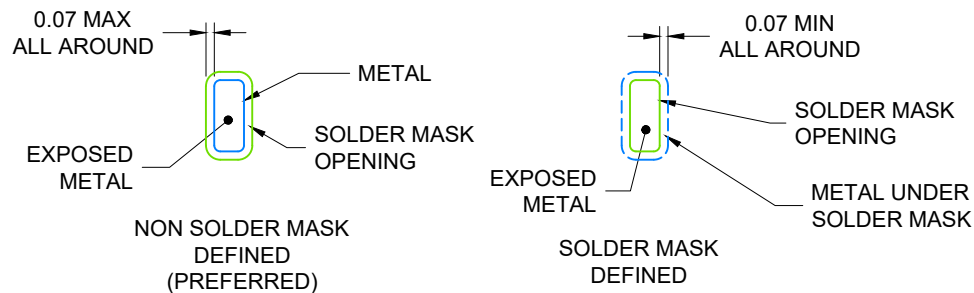
4228523/A 02/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



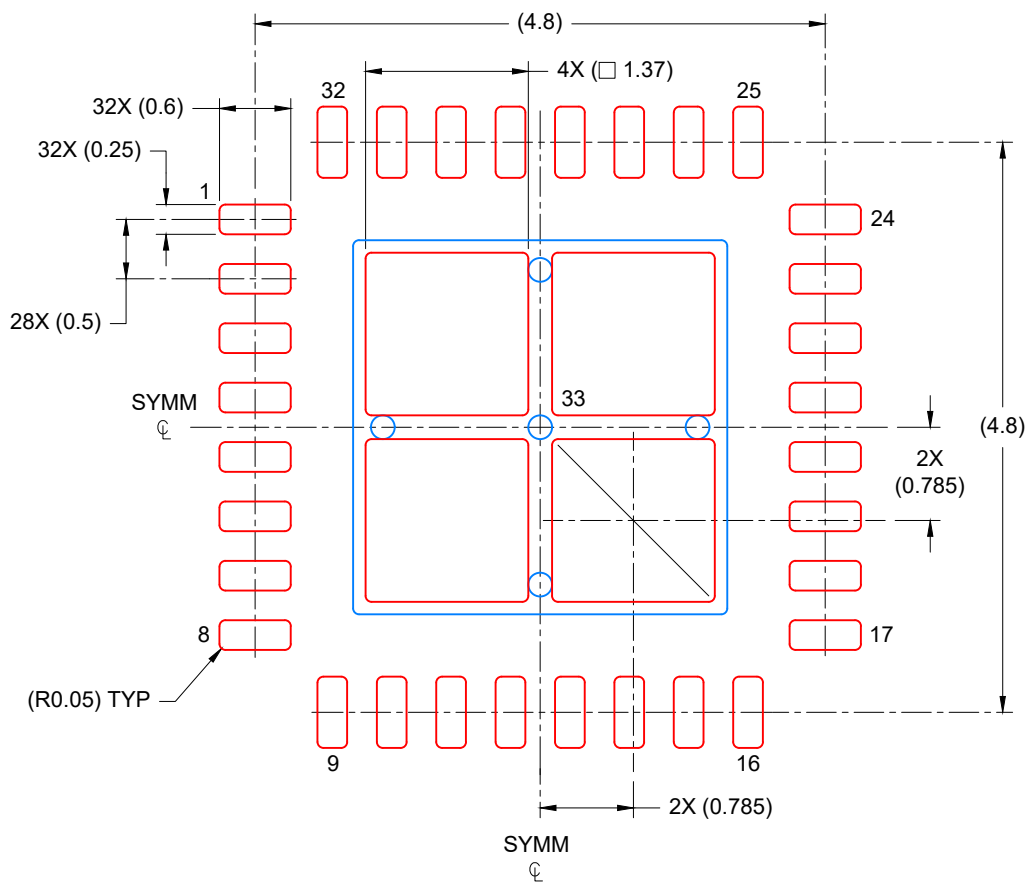
SOLDER MASK DETAILS

4228523/A 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 75% PRINTED COVERAGE BY AREA  
 SCALE: 15X

4228523/A 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated