

TPS650861 Programmable Multirail PMU for Multicore Processors, FPGAs, and Systems

1 Device Overview

1.1 Features

- Two Banks of One-Time Programmable Memory for Programming Default Voltages and Sequence
- Wide V_{IN} Range From 5.6 V to 21 V
- Three Variable-Output Voltage Synchronous Step-Down Controllers With D-CAP2™ Topology
 - Scalable Output Current Using External FETs With Selectable Current Limit
 - I²C DVS Control From 0.41 V to 1.67 V in 10-mV Steps or 1 V to 3.575 V in 25-mV Steps or Fixed 5 V Output
- Three Variable-Output Voltage Synchronous Step-Down Converters With DCS-Control Topology
 - V_{IN} Range From 3 V to 5.5 V
 - Up to 3 A of Output Current
 - I²C DVS Control From 0.425 V to 3.575 V in 25-mV Steps
- Three LDO Regulators With Adjustable Output Voltage
 - LDOA1: I²C-Selectable Voltage From 1.35 V to 3.3 V for up to 200 mA of Output Current
 - LDOA2 and LDOA3: I²C-Selectable Voltage From 0.7 V to 1.5 V for up to 600 mA of Output Current Each
- VTT LDO for DDR Memory Termination
- Three Load Switches With Slew Rate Control
 - Up to 300 mA of Output Current With Voltage Drop Less Than 1.5% of Nominal Input Voltage
 - $R_{DS(ON)} < 96 \text{ m}\Omega$ at Input Voltage of 1.8 V
- 5-V Fixed-Output Voltage LDO (LDO5)
 - Power Supply for Gate Drivers of SMPS and for LDOA1
 - Automatic Switch to External 5-V Buck for Higher Efficiency
- Built-in Flexibility and Configurability by OTP Programming
 - Six GPI Pins Configurable to Enable (CTL1 to CTL6) or Sleep Mode Entry (CTL3 and CTL6) of Any Selected Rails
 - Four GPO Pins Configurable to Power Good of Any Selected Rails
 - Open-Drain Interrupt Output Pin
- I²C Interface Supports Standard Mode (100 kHz), Fast Mode (400 kHz), and Fast Mode Plus (1 MHz)

1.2 Applications

- Programmable Logic Controller
- Machine Vision Camera
- Video Surveillance
- Test and Measurement
- Embedded PCs
- Motion Control

1.3 Description

The TPS650861 device family is a single-chip power-management IC (PMIC) designed to be programmed for optimal output voltages and sequencing. The TPS650861 has three controllers to provide flexible power capable of up to 30A with large external FETs for high power designs but which can scale down in both size and cost for smaller designs. Combined with three 3 A converters, three general purpose LDOs, a termination LDO for DDR, and three load switches, the TPS650861 can provide system power for a wide variety of applications. The D-CAP2™ and DCS-Control high-frequency voltage regulators use small passives to achieve a small solution size. The D-CAP2 and DCS-Control topologies have excellent transient response performance, ideal for processor core and system memory rails that have fast load switching. The device has two banks of one-time programmable (OTP) memory. For large volume opportunities, please contact a local TI sales representative to determine if use of TI's manufacturing for a custom OTP is available. Third party distributors may also support programming of the TPS650861.

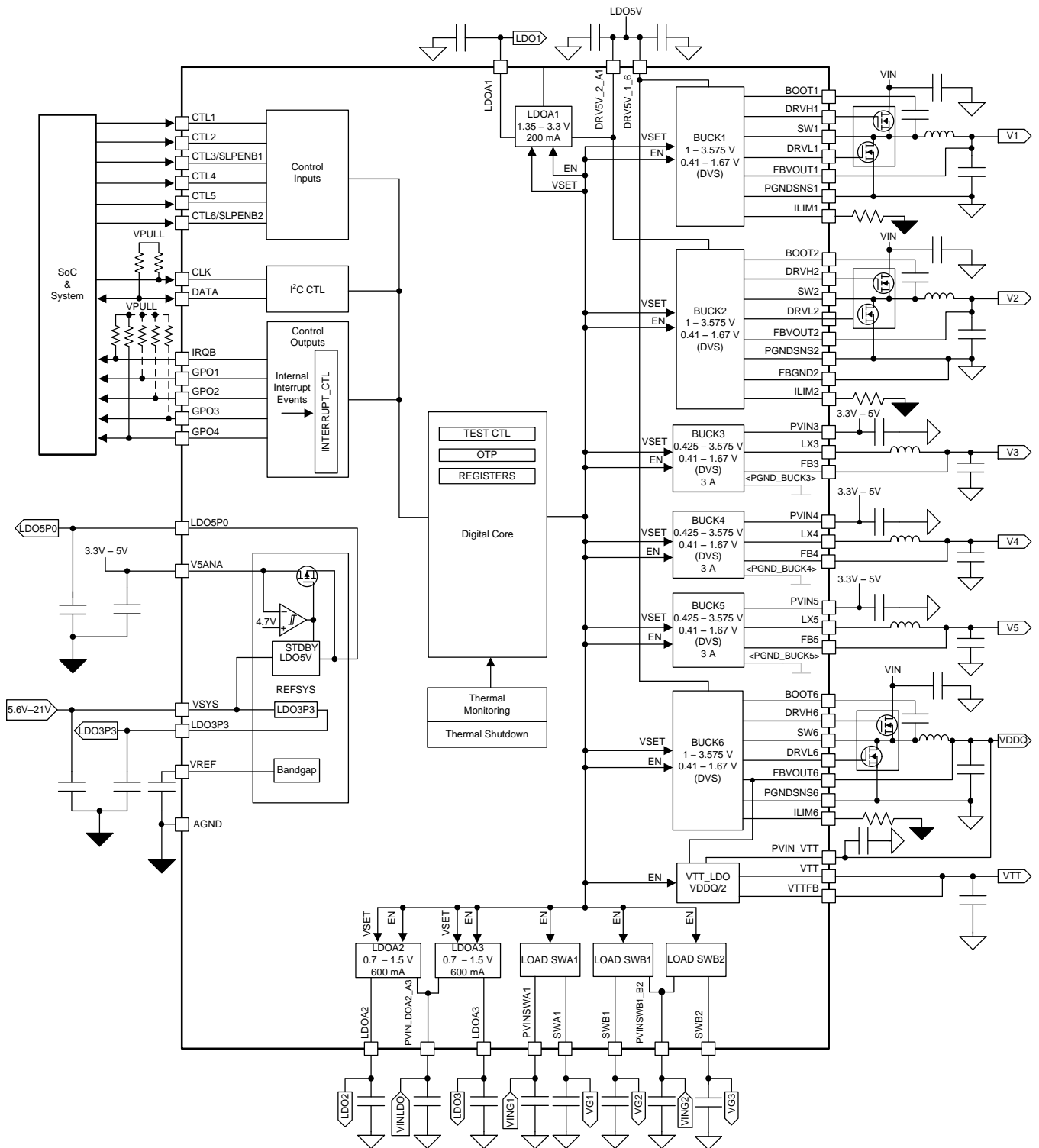
Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| TPS650861 | VQFN (64) | 8.00 mm × 8.00 mm |

(1) For more information, see the [Mechanical, Packaging, and Orderable Information](#) section.



1.4 PMIC Functional Block Diagram



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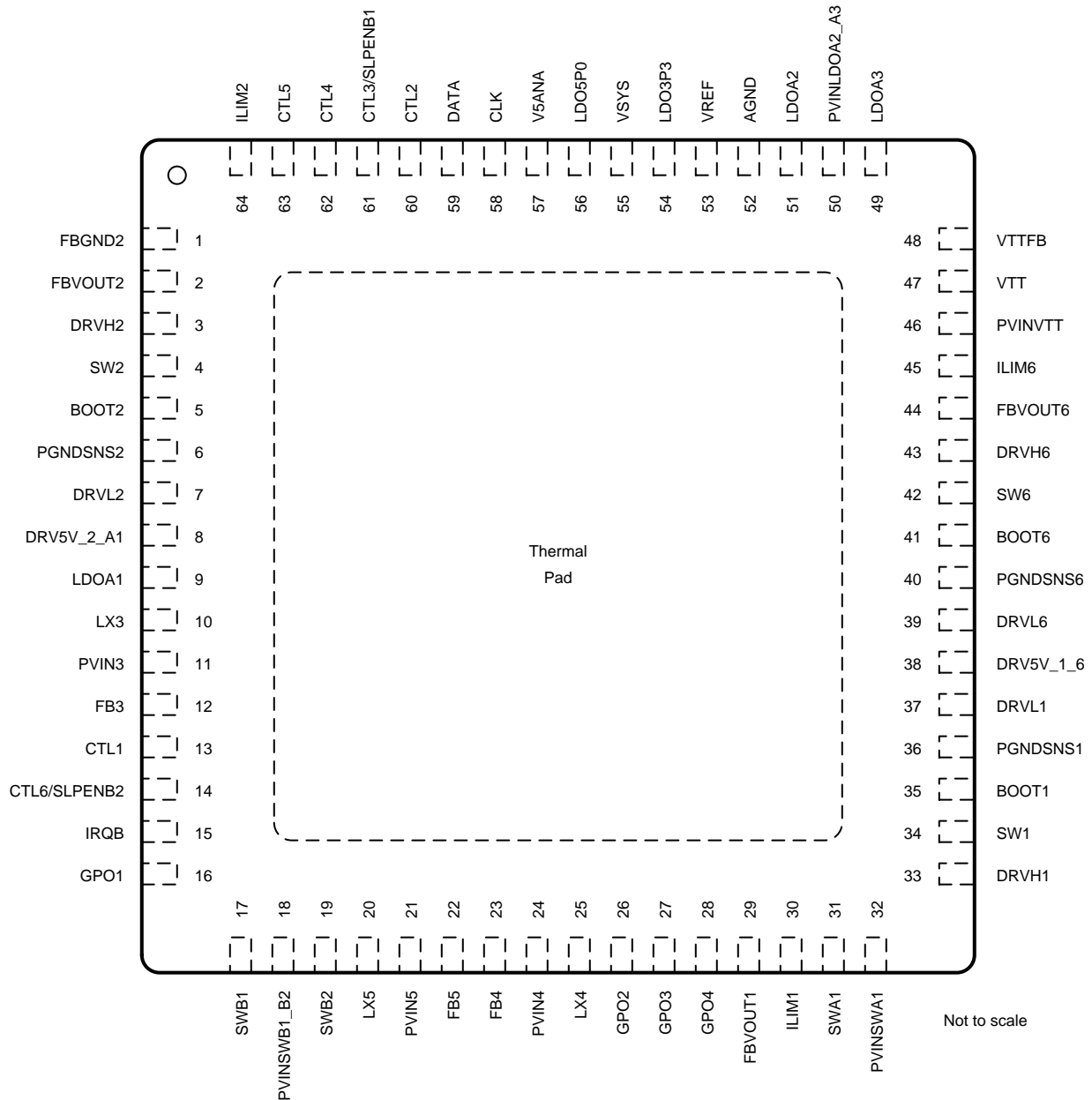
2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | COMMENT |
|-----------|----------|-----------------|
| July 2018 | * | Initial release |

3 Pin Configuration and Functions

Figure 3-1 shows the 64-pin RSK Plastic Quad Flatpack No-Lead package.



NOTE: The thermal pad must be connected to the system power ground plane.

Figure 3-1. 64-Pin RSK VQFN With Exposed Thermal Pad (Top View)

3.1 Pin Functions

Pin Functions

| PIN | | I/O | DESCRIPTION |
|------------------------|--------|-----|---|
| NO. | NAME | | |
| SMPS REGULATORS | | | |
| 1 | FBGND2 | I | Remote negative feedback sense for BUCK2 controller. Connect to negative terminal of output capacitor. Connect to ground when not in use. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|------------------------------|-------------|-----|--|
| NO. | NAME | | |
| 2 | FBVOUT2 | I | Remote positive feedback sense for BUCK2 controller. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 3 | DRVH2 | O | High-side gate driver output for BUCK2 controller. Leave floating when not in use. |
| 4 | SW2 | I | Switch node connection for BUCK2 controller. Connect to ground when not in use. |
| 5 | BOOT2 | I | Bootstrap pin for BUCK2 controller. Connect a 100-nF ceramic capacitor between this pin and SW2 pin. Leave floating when not in use. |
| 6 | PGNDSNS2 | I | Power GND connection for BUCK2. Connect to ground terminal of external low-side FET. Connect to ground when not in use. |
| 7 | DRVL2 | O | Low-side gate driver output for BUCK2 controller. Leave floating when not in use. |
| 8 | DRV5V_2_A1 | I | 5-V supply to BUCK2 gate driver and LDOA1. Bypass to ground with a 2.2- μ F (typical) ceramic capacitor. Shorted on board to LDO5P0 pin typically. Bypass not required if BUCK2 and LDOA1 are not in use. |
| 10 | LX3 | O | Switch node connection for BUCK3 converter. Connect to ground when not in use. |
| 11 | PVIN3 | I | Power input to BUCK3 converter. Bypass to ground with a 10- μ F (typical) ceramic capacitor. Bypass not required if BUCK3 is not in use. |
| 12 | FB3 | I | Remote feedback sense for BUCK3 converter. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 20 | LX5 | O | Switch node connection for BUCK5 converter. Leave floating when not in use. |
| 21 | PVIN5 | I | Power input to BUCK5 converter. Bypass to ground with a 10- μ F (typical) ceramic capacitor. Bypass not required if BUCK5 is not in use. |
| 22 | FB5 | I | Remote feedback sense for BUCK5 converter. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 23 | FB4 | I | Remote feedback sense for BUCK4 converter. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 24 | PVIN4 | I | Power input to BUCK4 converter. Bypass to ground with a 10- μ F (typical) ceramic capacitor. Bypass not required if BUCK4 is not in use. |
| 25 | LX4 | O | Switch node connection for BUCK4 converter. Leave floating when not in use. |
| 29 | FBVOUT1 | I | Remote feedback sense for BUCK1 controller. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 30 | ILIM1 | I | Current limit set pin for BUCK1 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET. Connect to ground when BUCK1 not in use. |
| 33 | DRVH1 | O | High-side gate driver output for BUCK1 controller. Leave floating when not in use. |
| 34 | SW1 | I | Switch node connection for BUCK1 controller. Connect to ground when not in use. |
| 35 | BOOT1 | I | Bootstrap pin for BUCK1 controller. Connect a 100-nF ceramic capacitor between this pin and SW1 pin. Leave floating when not in use. |
| 36 | PGNDSNS1 | I | Power GND connection for BUCK1. Connect to ground terminal of external low-side FET. Connect to ground when not in use. |
| 37 | DRVL1 | O | Low-side gate driver output for BUCK1 controller. Leave floating when not in use. |
| 38 | DRV5V_1_6 | I | 5-V supply to BUCK1 and BUCK6 gate drivers. Bypass to ground with a 2.2- μ F (typical) ceramic capacitor. Shorted on board to LDO5P0 pin typically. Bypass not required if BUCK1 and BUCK6 are not in use. |
| 39 | DRVL6 | O | Low-side gate driver output for BUCK6 controller. Leave floating when not in use. |
| 40 | PGNDSNS6 | I | Power GND connection for BUCK6. Connect to ground terminal of external low-side FET. Connect to ground when not in use. |
| 41 | BOOT6 | I | Bootstrap pin for BUCK6 controller. Connect a 100-nF ceramic capacitor between this pin and SW6 pin. Leave floating when not in use. |
| 42 | SW6 | I | Switch node connection for BUCK6 controller. Connect to ground when not in use. |
| 43 | DRVH6 | O | High-side gate driver output for BUCK6 controller. Leave floating when not in use. |
| 44 | FBVOUT6 | I | Remote feedback sense for BUCK6 controller and reference voltage for VTT LDO regulation. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 45 | ILIM6 | I | Current limit set pin for BUCK6 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET. Connect to ground when BUCK6 not in use. |
| 64 | ILIM2 | I | Current limit set pin for BUCK2 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET. Connect to ground when BUCK2 not in use. |
| LDO AND LOAD SWITCHES | | | |
| 9 | LDOA1 | O | LDOA1 output. Bypass to ground with a 4.7- μ F (typical) ceramic capacitor. Leave floating when not in use. |
| 17 | SWB1 | O | Output of load switch B1. Bypass to ground with a 0.1- μ F (typical) ceramic capacitor. Leave floating when not in use. |
| 18 | PVINSWB1_B2 | I | Power supply to load switch B1 and B2. Bypass to ground with a 1- μ F (typical) ceramic capacitor to improve transient performance. Connect to ground when not in use. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|------------------|--------------|-----|---|
| NO. | NAME | | |
| 19 | SWB2 | O | Output of load switch B2. Bypass to ground with a 0.1- μ F (typical) ceramic capacitor. Leave floating when not in use. |
| 31 | SWA1 | O | Output of load switch A1. Bypass to ground with a 0.1- μ F (typical) ceramic capacitor. Leave floating when not in use. |
| 32 | PVINSWA1 | I | Power supply to load switch A1. Bypass to ground with a 1- μ F (typical) ceramic capacitor to improve transient performance. Connect to ground when not in use. |
| 46 | PVINVTT | I | Power supply to VTT LDO. Bypass to ground with a 10- μ F (minimum) ceramic capacitor. Bypass not required if VTT LDO is not in use. |
| 47 | VTT | O | Output of load VTT LDO. Bypass to ground with 2 \times 22- μ F (minimum) ceramic capacitors. Leave floating when not in use. |
| 48 | VTTFB | I | Remote feedback sense for VTT LDO. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 49 | LDOA3 | O | Output of LDOA3. Bypass to ground with a 4.7- μ F (typical) ceramic capacitor. Leave floating when not in use. |
| 50 | PVINLDOA2_A3 | I | Power supply to LDOA2 and LDOA3. Bypass to ground with a 4.7- μ F (typical) ceramic capacitor. Connect to ground when not in use. |
| 51 | LDOA2 | O | Output of LDOA2. Bypass to ground with a 4.7- μ F (typical) ceramic capacitor. Leave floating when not in use. |
| 54 | LDO3P3 | O | Output of 3.3-V internal LDO. Bypass to ground with a 4.7- μ F (typical) ceramic capacitor. |
| 56 | LDO5P0 | O | Output of 5-V internal LDO or an internal switch that connects this pin to V5ANA. Bypass to ground with a 4.7- μ F (typical) ceramic capacitor. |
| 57 | V5ANA | I | Bias used by converters (BUCK3, BUCK4, and BUCK5) for regulation. Must be same supply as PVINx. Also has an internal load switch that connects this pin to LDO5P0 pin if 5-V is used. Bypass this pin with an optional ceramic capacitor to improve transient performance. |
| INTERFACE | | | |
| 13 | CTL1 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. |
| 14 | CTL6/SLPENB2 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. Alternatively, when configured to active-low sleep enable, a group of VRs chosen can be entered into (L) or out of (H) sleep state where their output voltages may be different from those in normal state. |
| 15 | IRQB | O | Open-drain output interrupt pin. Refer to Section 5.11.4, IRQ: PMIC Interrupt Register , for definitions. For programming, this pin must be supplied with a stable 7-V supply to burn the OTP memory. Recommend bypassing to ground with a 1- μ F (typical) ceramic capacitor. Do not back-drive any pull-up on this output if programming. ⁽¹⁾ |
| 16 | GPO1 | O | General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect Power Good status of VRs of any choice or to be controlled by an I ² C register bit by the user, which then can be used as an enable signal to an external VR. |
| 26 | GPO2 | O | General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect Power Good status of VRs of any choice or to be controlled by an I ² C register bit by the user, which then can be used as an enable signal to an external VR. |
| 27 | GPO3 | O | General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect Power Good status of VRs of any choice or to be controlled by an I ² C register bit by the user, which then can be used as an enable signal to an external VR. |
| 28 | GPO4 | O | Open-drain output that can be configured to reflect Power Good status of VRs of any choice or to be controlled by an I ² C register bit by the user, which then can be used as an enable signal to an external VR. |
| 58 | CLK | I | I ² C clock |
| 59 | DATA | I/O | I ² C data |
| 60 | CTL2 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. |
| 61 | CTL3/SLPENB1 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. Alternatively, when configured to active-low sleep enable, a group of VRs chosen can be entered into (L) or out of (H) sleep state where their output voltages may be different from those in normal state. |
| 62 | CTL4 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. For programming, this pin must be supplied with a stable 7-V supply to enter the programming state. Because of this requirement, CTL4 is generally not used to enable or disable regulators for the TPS650861 to avoid enabling rails during programming or damaging devices connected to CTL4. No bypass capacitor is needed for this pin. ⁽¹⁾ |
| 63 | CTL5 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. |
| REFERENCE | | | |
| 52 | AGND | — | Analog ground. Do not connect to the thermal pad ground on top layer. Connect to ground of VREF capacitor. |
| 53 | VREF | O | Band-gap reference output. Stabilize it by connecting a 100-nF (typical) ceramic capacitor between this pin and quiet ground. |
| 55 | VSYS | I | System voltage detection and input to internal LDOs (3.3 V and 5 V). Bypass to ground with a 1- μ F (typical) ceramic capacitor. |

(1) Ambient temperature must remain below 50 °C during programming, total time must be less than one minute.

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|--------------------|--------------------|-----|--|
| NO. | NAME | | |
| THERMAL PAD | | | |
| — | Thermal pad (PGND) | — | Connect to PCB ground plane using multiple vias for good thermal and electrical performance. |

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|---|-------------------|-----|------|
| ANALOG | | | |
| Input voltage from battery, V _{SYS} | −0.3 | 28 | V |
| PVIN3, PVIN4, PVIN5, LDO5P0, DRV5V_1_6, DRV5V_2_A1, DRVL1, DRVL2, DRVL6 | −0.3 | 7 | V |
| V5ANA | −0.3 | 6 | V |
| PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2 | −0.3 | 0.3 | V |
| DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6 | −0.3 | 34 | V |
| SW1, SW2, SW6 | −5 ⁽²⁾ | 28 | V |
| LX3, LX4, LX5 | −2 ⁽³⁾ | 8 | V |
| Differential voltage, BOOTx to SWx | −0.3 | 5.5 | V |
| VREF, LDO3P3, FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5, ILIM1, ILIM2, ILIM6, PVINVT, VTT, VTTFB, PVINSWA1, SWA1, PVINSWB1_B2, SWB1, SWB2, LDOA1 | −0.3 | 3.6 | V |
| PVINLDOA2_A3, LDOA2, LDOA3 | −0.3 | 3.3 | V |
| DIGITAL IO | | | |
| DATA, CLK, GPO1-GPO3 | −0.3 | 3.6 | V |
| CTL1-CTL6, GPO4, IRQB (normal use) | −0.3 | 7 | V |
| CTL4, IRQB (programming) ⁽⁴⁾ | −0.3 | 8.4 | V |
| Storage temperature, T _{stg} | −40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Transient for less than 5 ns

(3) Transient for less than 20 ns

(4) Ambient temperature must remain below 50 °C during programming, total time must be less than one minute.

4.2 ESD Ratings

| | VALUE | UNIT |
|--|--|-------|
| V _{ESD} Electrostatic discharge | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾ | ±1000 |
| | Charged Device Model (CDM), per JESD22-C101 ⁽²⁾ | ±250 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|------|-------|------------------|------|
| ANALOG | | | | |
| V _{SYS} | 5.6 | 13 | 21 | V |
| V _{REF} | –0.3 | | 1.3 | V |
| PVIN3, PVIN4, PVIN5, LDO5P0, V5ANA, DRV5V_1_6, DRV5V_2_A1 | –0.3 | | 5.5 | V |
| PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2 | –0.3 | | 0.3 | V |
| DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6 | –0.3 | | 26.5 | v |
| DRVL1, DRVL2, DRVL6 | –0.3 | | 5.5 | V |
| SW1, SW2, SW6 | –1 | | 21 | V |
| LX3, LX4, LX5 | –1 | | 5.5 | V |
| FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5 | –0.3 | | 3.6 | V |
| LDO3P3, ILIM1, ILIM2, ILIM6, LDOA1 | –0.3 | | 3.3 | V |
| PVINVTT | –0.3 | BUCK6 | FBVOUT6 | V |
| V _{TT} , V _{TTFB} | –0.3 | | 0.5 × FBVOUT6 | V |
| PVINSWA1, SWA1, PVINSWB1_B2, SWB1, SWB2 | –0.3 | | 3.6 | V |
| PVINLDOA2_A3 | –0.3 | | 1.8 | V |
| LDOA2, LDOA3 | –0.3 | | 1.5 | V |
| DIGITAL IO | | | | |
| DATA, CLK, CTL1–CTL6, GPO1–GPO4, IRQB (normal use) | –0.3 | | 3.3 | V |
| CTL4, IRQB (during programming) ⁽¹⁾ | 6.7 | 7 | 7.3 | V |
| CHIP | | | | |
| Operating ambient temperature, T _A | –40 | 27 | 85 | °C |
| Operating junction temperature, T _J | –40 | 27 | 125 | °C |

(1) Ambient temperature must remain below 50 °C during programming, total time must be less than one minute.

4.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS650861 | UNIT |
|-------------------------------|--|------------|------|
| | | RSK (VQFN) | |
| | | 64 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 25.8 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 11.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 4.4 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 4.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 0.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics application report](#).

4.5 Electrical Characteristics: Total Current Consumption

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|-----|-----|-----|------|
| I _{SD} | PMIC shutdown current that includes I _Q for references, LDO5, LDO3P3, and digital core | | 65 | | μA |

4.6 Electrical Characteristics: Reference and Monitoring System

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A = 25^\circ\text{C}$) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--|--|-------|------|------|------------------|
| REFERENCE | | | | | | |
| V_{REF} | Band-gap reference voltage | | | 1.25 | | V |
| | Accuracy | | -0.5% | | 0.5% | |
| C_{VREF} | Band-gap output capacitor | | 0.047 | 0.1 | 0.22 | μF |
| $V_{SYS_UVLO_5V}$ | VSYS UVLO threshold for LDO5 | V_{SYS} falling | 5.24 | 5.4 | 5.56 | V |
| $V_{SYS_UVLO_5V_HYS}$ | VSYS UVLO threshold hysteresis for LDO5 | V_{SYS} rising above $V_{SYS_UVLO_5V}$ | | 200 | | mV |
| $V_{SYS_UVLO_3V}$ | VSYS UVLO threshold for LDO3P3 | V_{SYS} falling | 3.45 | 3.6 | 3.75 | V |
| $V_{SYS_UVLO_3V_HYS}$ | VSYS UVLO threshold hysteresis for LDO3P3 | V_{SYS} rising above $V_{SYS_UVLO_3V}$ | | 150 | | mV |
| T_{CRIT} | Critical threshold of die temperature | T_J rising | 130 | 145 | 160 | $^\circ\text{C}$ |
| T_{CRIT_HYS} | Hysteresis of T_{CRIT} | T_J falling | | 10 | | $^\circ\text{C}$ |
| T_{HOT} | Hot threshold of die temperature | T_J rising | 110 | 115 | 120 | $^\circ\text{C}$ |
| T_{HOT_HYS} | Hysteresis of T_{HOT} | T_J falling | | 10 | | $^\circ\text{C}$ |
| LDO5 | | | | | | |
| V_{IN} | Input voltage at V_{SYS} pin | | 5.6 | 13 | 21 | V |
| V_{OUT} | DC output voltage | $I_{OUT} = 10\text{ mA}$ | 4.9 | 5 | 5.1 | V |
| I_{OUT} | DC output current | | | 100 | 180 | mA |
| I_{OCP} | Overcurrent protection | Measured with output shorted to ground | 200 | | | mA |
| V_{TH_PG} | Power Good assertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 94% | | |
| $V_{TH_PG_HYS}$ | Power Good deassertion hysteresis | V_{OUT} rising or falling | | 4% | | |
| I_Q | Quiescent current | $V_{IN} = 13\text{ V}$, $I_{OUT} = 0\text{ A}$ | | 20 | | μA |
| C_{OUT} | External output capacitance | | 2.7 | 4.7 | 10 | μF |
| V5ANA-to-LDO5P0 LOAD SWITCH | | | | | | |
| $R_{DS(on)}$ | On resistance | $V_{IN} = 5\text{ V}$, measured from V5ANA pin to LDO5P0 pin at $I_{OUT} = 200\text{ mA}$ | | | 1 | Ω |
| V_{TH_PG} | Power Good threshold for external 5-V supply | V_{V5ANA} rising | | 4.7 | | V |
| $V_{TH_HYS_PG}$ | Power Good threshold hysteresis for external 5-V supply | V_{V5ANA} falling | | 100 | | mV |
| I_{LKG} | Leakage current | Switch disabled, $V_{V5ANA} = 5\text{ V}$, $V_{LDO5} = 0\text{ V}$ | | | 10 | μA |
| LDO3P3 | | | | | | |
| V_{IN} | Input voltage at V_{SYS} pin | | 5.6 | 13 | 21 | V |
| V_{OUT} | DC output voltage | $I_{OUT} = 10\text{ mA}$ | | 3.3 | | V |
| | Accuracy | $V_{IN} = 13\text{ V}$, $I_{OUT} = 10\text{ mA}$ | -3% | | 3% | |
| I_{OUT} | DC output current | | | | 40 | mA |
| I_{OCP} | Overcurrent protection | Measured with output shorted to ground | 70 | | | mA |
| V_{TH_PG} | Power Good assertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 92% | | |
| $V_{TH_PG_HYS}$ | Power Good deassertion hysteresis | V_{OUT} falling | | 3% | | |
| I_Q | Quiescent current | $V_{IN} = 13\text{ V}$, $I_{OUT} = 0\text{ A}$ | | 20 | | μA |
| C_{OUT} | External output capacitance | | 2.2 | 4.7 | 10 | μF |

4.7 Electrical Characteristics: Buck Controllers

over recommended input voltage range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $T_A = 25^\circ\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|---|------------------|-------|--------|-------------------|
| BUCK1, BUCK2, BUCK6 | | | | | | |
| V_{IN} | Power input voltage for external HSD FET | | 5.6 | 13 | 21 | V |
| V_{OUT} | DC output voltage VID range and options | VID step size = 10 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111 | 0.41 | | 1.67 | V |
| | | VID step size = 25 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111 | 1 ⁽¹⁾ | | 3.575 | V |
| | DC output voltage accuracy | $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3\text{ V}$, $I_{OUT} = 100\text{ mA to }7\text{ A}$ | -2% | | 2% | |
| | Total output voltage accuracy (DC + ripple) in DCM | $I_{OUT} = 10\text{ mA}$, $V_{OUT} \leq 1\text{ V}$ | -30 | | 40 | mV |
| $V_{FB_EXT_BUCK1}$ | Feedback regulation voltage | Applies only to the Buck1 Controller if programmed for external feedback voltage adjustability | 384 | 400 | 416 | mV |
| $I_{FB_LKG_BUCK1}$ | Feedback pin leakage current | Applies only to the Buck1 Controller if programmed for external feedback voltage adjustability | | | 65 | nA |
| $SR(V_{OUT})$ | Output DVS slew rate | VID step size = 10 mV | 2.5 | 3.125 | | mV/ μs |
| | | VID step size = 25 mV | 3.125 | 4 | | |
| I_{LIM_LSD} | Low-side output valley current limit accuracy (programmed by external resistor R_{LIM}) | | -15% | | 15% | |
| I_{LIMREF} | Source current out of ILIM1 pin | $T = 25^\circ\text{C}$ | 45 | 50 | 55 | μA |
| V_{LIM} | Voltage at ILIM1 pin | $V_{LIM} = R_{LIM} \times I_{LIMREF}$ | 0.2 | | 2.25 | V |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3\text{ V}$, $I_{OUT} = 7\text{ A}$ | -0.5% | | 0.5% | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $V_{IN} = 13\text{ V}$, $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3\text{ V}$, $I_{OUT} = 0\text{ A to }7\text{ A}$, referenced to V_{OUT} at $I_{OUT} = I_{OUT_MAX}$ | 0% | | 1% | |
| V_{TH_PG} | Power Good deassertion threshold in percentage of target V_{OUT} | V_{OUT} rising | 105.5% | 108% | 110.5% | |
| | | V_{OUT} falling | 89.5% | 92% | 94.5% | |
| R_{DSON_DRVH} | Driver DRVH resistance | Source, $I_{DRVH} = -50\text{ mA}$ | | 3 | | Ω |
| | | Sink, $I_{DRVH} = 50\text{ mA}$ | | 2 | | Ω |
| R_{DSON_DRVL} | Driver DRVL resistance | Source, $I_{DRVL} = -50\text{ mA}$ | | 3 | | Ω |
| | | Sink, $I_{DRVL} = 50\text{ mA}$ | | 0.4 | | Ω |
| R_{DIS} | Output auto-discharge resistance | BUCKx_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | BUCKx_DISCHG[1:0] = 10 | | 200 | | Ω |
| | | BUCKx_DISCHG[1:0] = 11 | | 500 | | Ω |
| C_{BOOT} | Bootstrap capacitance | | | 100 | | nF |
| R_{ON_BOOT} | Bootstrap switch ON resistance | | | | 20 | Ω |

(1) BUCKx_VID[6:0] = 0000001 – 0011000

4.8 Electrical Characteristics: Synchronous Buck Converters

over recommended input voltage range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and $T_A = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|--|-------|------|-------|-------------------|
| BUCK3, BUCK4, BUCK5 | | | | | | |
| V_{IN} | Power input voltage | | 3.0 | | 5.5 | V |
| V_{OUT} | DC output voltage VID range and options | VID step size = 25 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111 | 0.425 | | 3.575 | V |
| | | $V_{IN} = 5.0\text{ V}$, $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3\text{ V}$, $I_{OUT} = 1.5\text{ A}$ | -2% | | 2% | |
| | DC output voltage accuracy | $V_{IN} = 3.3\text{ V}$, $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8\text{ V}$, $I_{OUT} = 1.5\text{ A}$ | -2% | | 2% | |
| | | $V_{IN} = 5.0\text{ V}$, $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8\text{ V}, 2.5, 3.3\text{ V}$, $I_{OUT} = 100\text{ mA}$ | -2.5% | | 2.5% | |
| | | $V_{IN} = 3.3\text{ V}$, $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$ | -2.5% | | 2.5% | |
| SR(V_{OUT}) | Output DVS slew rate | | 3.125 | 4 | | mV/ μs |
| I_{OUT} | Continuous DC output current | | | | 3 | A |
| I_{IND_LIM} | HSD FET current limit | | 4.3 | | 7 | A |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3\text{ V}$, $I_{OUT} = 1.5\text{ A}$ | -0.5% | | 0.5% | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $V_{IN} = 5\text{ V}$, $V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3\text{ V}$, $I_{OUT} = 0\text{ A}$ to 3 A , referenced to V_{OUT} at $I_{OUT} = 1.5\text{ A}$ | -0.2% | | 2% | |
| V_{TH_PG} | Power Good deassertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 108% | | |
| | | V_{OUT} falling | | 92% | | |
| $V_{TH_HYS_PG}$ | Power Good reassertion hysteresis entering back into V_{TH_PG} | V_{OUT} rising or falling | | 3% | | |
| C_{OUT} | Output filtering capacitance | | | | 400 | μF |
| R_{DIS} | Output auto-discharge resistance | BUCKx_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | BUCKx_DISCHG[1:0] = 10 | | 200 | | |
| | | BUCKx_DISCHG[1:0] = 11 | | 500 | | |

4.9 Electrical Characteristics: LDOs

over recommended input voltage range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $T_A = 25^\circ\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|--|----------------------------|------|------|---------------|
| LDOA1 | | | | | | |
| V_{IN} | Input voltage | | 4.5 | 5 | 5.5 | V |
| V_{OUT} | DC output voltage | Set by LDOA1_VID[3:0] | 1.35 | | 3.3 | V |
| | Accuracy | $I_{OUT} = 0$ to 200 mA | -2% | | 2% | V |
| I_{OUT} | DC output current | | | | 200 | mA |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $I_{OUT} = 40$ mA | -0.5% | | 0.5% | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $I_{OUT} = 10$ mA to 200 mA | -2% | | 2% | |
| I_{OCP} | Overcurrent protection | $V_{IN} = 5$ V, Measured with output shorted to ground | 500 | | | mA |
| V_{TH_PG} | Power Good deassertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 108% | | |
| | | V_{OUT} falling | | 92% | | |
| $t_{STARTUP}$ | Start-up time | Measured from EN = H to reach 95% of final value, $C_{OUT} = 4.7$ μF | | | 500 | μs |
| I_Q | Quiescent current | $I_{OUT} = 0$ A | | 23 | | μA |
| C_{OUT} | External output capacitance | | 2.7 | 4.7 | 10 | μF |
| | ESR | | | | 100 | m Ω |
| R_{DIS} | Output auto-discharge resistance | LDOA1_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | LDOA1_DISCHG[1:0] = 10 | | 190 | | Ω |
| | | LDOA1_DISCHG[1:0] = 11 | | 450 | | Ω |
| LDOA2 and LDOA3 | | | | | | |
| V_{IN} | Power input voltage | | $V_{OUT} + V_{DROP}^{(1)}$ | 1.8 | 1.98 | V |
| V_{OUT} | LDOA2 DC output voltage | Set by LDOA2_VID[3:0] | 0.7 | | 1.5 | V |
| | LDOA3 DC output voltage | Set by LDOA3_VID[3:0] | 0.7 | See | 1.5 | V |
| | DC output voltage accuracy | $I_{OUT} = 0$ to 600 mA | -2% | | 3% | |
| I_{OUT} | DC output current | | | | 600 | mA |
| V_{DROP} | Dropout voltage | $V_{OUT} = 0.99 \times V_{OUT_NOM}$, $I_{OUT} = 600$ mA | | | 350 | mV |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $I_{OUT} = 300$ mA | -0.5% | | 0.5% | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $I_{OUT} = 10$ mA to 600 mA | -2% | | 2% | |
| I_{OCP} | Overcurrent protection | Measured with output shorted to ground | 0.65 | 1.25 | | A |
| V_{TH_PG} | Power Good assertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 108% | | |
| | | V_{OUT} falling | | 92% | | |
| $t_{STARTUP}$ | Start-up time | Measured from EN = H to reach 95% of final value, $C_{OUT} = 4.7$ μF | | | 500 | μs |
| I_Q | Quiescent current | $I_{OUT} = 0$ A | | 20 | | μA |
| PSRR | Power supply rejection ratio | $f = 1$ kHz, $V_{IN} = 1.8$ V, $V_{OUT} = 1.2$ V, $I_{OUT} = 300$ mA, $C_{OUT} = 2.2$ μF – 4.7 μF | | 48 | | dB |
| | | $f = 10$ kHz, $V_{IN} = 1.8$ V, $V_{OUT} = 1.2$ V, $I_{OUT} = 300$ mA, $C_{OUT} = 2.2$ μF – 4.7 μF | | 30 | | dB |
| C_{OUT} | External output capacitance | | 2.2 | 4.7 | 10 | μF |
| | ESR | | | | 100 | m Ω |
| R_{DIS} | Output auto-discharge resistance | LDOA[2,3]_DISCHG[1:0] = 01 | | 80 | | Ω |
| | | LDOA[2,3]_DISCHG[1:0] = 10 | | 180 | | Ω |
| | | LDOA[2,3]_DISCHG[1:0] = 11 | | 475 | | Ω |

(1) The minimum value must be equal to or greater than 1.62 V.

Electrical Characteristics: LDOs (continued)

over recommended input voltage range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $T_A = 25^\circ\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|------|--------------|-----|---------------|
| VTT LDO | | | | | | |
| V_{IN} | Power input voltage | | | 1.2 | 3.3 | V |
| V_{OUT} | DC output voltage | $V_{IN} = 1.2\text{ V}$, Measured at VTTFB pin | | $V_{IN} / 2$ | | V |
| | DC output voltage accuracy | Relative to $V_{IN} / 2$, $I_{OUT} \leq 10\text{ mA}$, $1.1\text{ V} \leq V_{IN} \leq 1.35\text{ V}$ | -10 | | 10 | mV |
| Relative to $V_{IN} / 2$, $I_{OUT} \leq 500\text{ mA}$, $1.1\text{ V} \leq V_{IN} \leq 1.35\text{ V}$ | | -25 | | 25 | | |
| I_{OUT} | DC Output Current (Rms Value Over Operation) | $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$ | -500 | 0 | 500 | mA |
| | Pulsed Current (Duty Cycle Limited to Remain Below DC Rms Specification) | source(+) and sink(-): $I_{OCP} = 0.95\text{ A}$, $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$ | -500 | | 500 | mA |
| source(+) and sink(-): $I_{OCP} = 1.8\text{ A}$, $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$ | | -1800 | | 1800 | | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | Relative to $V_{IN} / 2$, $I_{OUT} \leq 10\text{ mA}$, $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$ | -10 | | 10 | mV |
| | | Relative to $V_{IN} / 2$, $I_{OUT} \leq 500\text{ mA}$, $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$ | -20 | | 20 | |
| | | Relative to $V_{IN} / 2$, $I_{OUT} \leq 1200\text{ mA}$, $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$ | -30 | | 30 | |
| | | Relative to $V_{IN} / 2$, $I_{OUT} \leq 1800\text{ mA}$, $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$ | -40 | | 40 | |
| ΔV_{OUT_TR} | Load transient regulation | DC + AC at sense point, $1.1\text{ V} \leq V_{IN} \leq 1.5\text{ V}$, ($I_{OUT} = 0$ to 350 mA and 350 mA to 0) AND (0 to -350 mA and -350 mA to 0) with $1\text{ }\mu\text{s}$ of rise and fall time $C_{OUT} = 40\text{ }\mu\text{F}$ | -5% | | 5% | |
| I_{OCP} | Overcurrent protection | Measured with output shorted to ground: OTPs with VTT $I_{LIM} = 0.95\text{ A}$ | 0.95 | | | A |
| | | Measured with output shorted to ground: OTPs with VTT $I_{LIM} = 1.8\text{ A}$ | 1.8 | | | |
| V_{TH_PG} | Power Good deassertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 110% | | |
| | | V_{OUT} falling | | 95% | | |
| $V_{TH_HYS_PG}$ | Power Good reassertion hysteresis entering back into V_{TH_PG} | | | 5% | | |
| I_Q | Total ground current | $V_{IN} = 1.2\text{ V}$, $I_{OUT} = 0\text{ A}$ | | | 240 | μA |
| I_{LKG} | OFF leakage current | $V_{IN} = 1.2\text{ V}$, disabled | | | 1 | μA |
| C_{IN} | External input capacitance | | 10 | | | μF |
| C_{OUT} | External output capacitance | | 35 | | | μF |
| R_{DIS} | Output auto-discharge resistance | VTT_DISCHG = 0 | 1000 | | | k Ω |
| | | VTT_DISCHG = 1 | 60 | 80 | 100 | Ω |

4.10 Electrical Characteristics: Load Switches

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--|---|-----|------|------|---------------|
| SWA1 | | | | | | |
| V_{IN} | Input voltage range | | 0.5 | | 3.3 | V |
| I_{OUT} | DC output current | | | | 300 | mA |
| $R_{DS(on)}$ | ON resistance | $V_{IN} = 1.8\text{ V}$, measured from PVINSWA1 pin to SWA1 pin at $I_{OUT} = I_{OUT(MAX)}$ | | 60 | 93 | m Ω |
| | | $V_{IN} = 3.3\text{ V}$, measured from PVINSWA1 pin to SWA1 pin at $I_{OUT} = I_{OUT(MAX)}$ | | 100 | 165 | |
| V_{TH_PG} | Power Good deassertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 108% | | |
| | | V_{OUT} falling | | 92% | | |
| $V_{TH_HYS_PG}$ | Power Good reassertion hysteresis entering back into V_{TH_PG} | V_{OUT} rising or falling | | 2% | | |
| I_{INRUSH} | Inrush current upon turnon | $V_{IN} = 3.3\text{ V}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ | | | 10 | mA |
| I_Q | Quiescent current | $V_{IN} = 3.3\text{ V}$, $I_{OUT} = 0\text{ A}$ | | 10.5 | | μA |
| | | $V_{IN} = 1.8\text{ V}$, $I_{OUT} = 0\text{ A}$ | | 9 | | |
| I_{LKG} | Leakage current | Switch disabled, $V_{IN} = 1.8\text{ V}$ | | 7 | 370 | nA |
| | | Switch disabled, $V_{IN} = 3.3\text{ V}$ | | 10 | 900 | |
| C_{OUT} | External output capacitance | | | 0.1 | | μF |
| R_{DIS} | Output auto-discharge resistance | SWA1_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | SWA1_DISCHG[1:0] = 10 | | 200 | | |
| | | SWA1_DISCHG[1:0] = 11 | | 500 | | |
| SWB1, SWB2, SWB1_2 | | | | | | |
| V_{IN} | Input voltage range | | 0.5 | | 3.3 | V |
| I_{OUT} | DC current per output | | | | 400 | mA |
| $R_{DS(on)}$ | ON resistance per output | $V_{IN} = 1.8\text{ V}$, measured from PVINSWB1_B2 pin to SWBx pin at $I_{OUT} = I_{OUT(MAX)}$, per output switch | | 68 | 92 | m Ω |
| | | $V_{IN} = 3.3\text{ V}$, measured from PVINSWB1_B2 pin to SWBx pin at $I_{OUT} = I_{OUT(MAX)}$, per output switch | | 75 | 125 | m Ω |
| V_{TH_PG} | Power Good deassertion threshold in percentage of target V_{OUT} | V_{OUT} rising | | 108% | | |
| | | V_{OUT} falling | | 92% | | |
| $V_{TH_HYS_PG}$ | Power Good reassertion hysteresis entering back into V_{TH_PG} | V_{OUT} rising or falling | | 2% | | |
| I_{INRUSH} | Inrush current upon turning on | $V_{IN} = 3.3\text{ V}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ | | | 10 | mA |
| I_Q | Quiescent current | $V_{IN} = 3.3\text{ V}$, $I_{OUT} = 0\text{ A}$ | | 10.5 | | μA |
| | | $V_{IN} = 1.8\text{ V}$, $I_{OUT} = 0\text{ A}$ | | 9 | | |
| I_{LKG} | Leakage current | Switch disabled, $V_{IN} = 1.8\text{ V}$ | | 7 | 460 | nA |
| | | Switch disabled, $V_{IN} = 3.3\text{ V}$ | | 10 | 1150 | |
| C_{OUT} | External output capacitance | | | 0.1 | | μF |
| R_{DIS} | Output auto-discharge resistance | SWBx_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | SWBx_DISCHG[1:0] = 10 | | 200 | | |
| | | SWBx_DISCHG[1:0] = 11 | | 500 | | |

4.11 Digital Signals: I²C Interface

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--------------------------------|------------------------------|-----|------|-----|------|
| V _{OL} | Low-level output voltage | V _{PULL_UP} = 1.8 V | | | 0.4 | V |
| V _{IH} | High-level input voltage | | 1.2 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.4 | V |
| I _{LKG} | Leakage current | V _{PULL_UP} = 1.8 V | | 0.01 | 0.3 | μA |
| R _{PULL-UP} | Pullup resistance | Standard mode | | | 8.5 | kΩ |
| | | Fast mode | | | 2.5 | |
| | | Fast mode plus | | | 1 | |
| C _{OUT} | Total load capacitance per pin | | | | 50 | pF |

4.12 Digital Input Signals (CTLx)

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|-----------------|------|-----|-----|------|
| V _{IH} | High-level input voltage | | 0.85 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.4 | V |

4.13 Digital Output Signals (IRQB, GPOx)

Over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------------------|------------------------------|-----|-----|------|------|
| V _{OL} | Low-level output voltage | I _{OL} < 2 mA | | | 0.4 | V |
| I _{LKG} | Leakage current | V _{PULL_UP} = 1.8 V | | | 0.35 | μA |

4.14 Timing Requirements

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---------------------------------|----------------------------------|-----|-----|------|------|
| I²C INTERFACE | | | | | |
| f _{CLK} | Clock frequency (standard mode) | | | 100 | kHz |
| | Clock frequency (fast mode) | | | 400 | kHz |
| | Clock frequency (fast mode plus) | | | 1000 | kHz |
| t _r | Rise time (standard mode) | | | 1000 | ns |
| | Rise time (fast mode) | | | 300 | ns |
| | Rise time (fast mode plus) | | | 120 | ns |
| t _f | Fall time (standard mode) | | | 300 | ns |
| | Fall time (fast mode) | | | 300 | ns |
| | Fall time (fast mode plus) | | | 120 | ns |

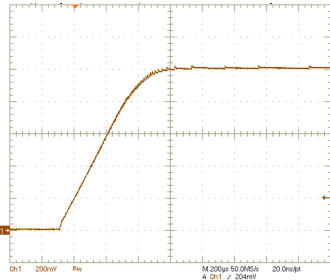
4.15 Switching Characteristics

over operating free-air temperature range and over recommended input voltage range (typical values are at $T_A = 25^\circ\text{C}$) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|--|-----|---------------------------------|------|---------------|
| BUCK CONTROLLERS | | | | | | |
| t_{PG} | Total turnon time | Measured from enable going high to when output reaches 90% of target value. | | 550 | 850 | μs |
| $T_{ON,MIN}$ | Minimum on-time of DRVH | | | 50 | | ns |
| T_{DEAD} | Driver dead-time | DRVH off to DRVL on | | 15 | | ns |
| | | DRVL off to DRVH on | | 30 | | ns |
| f_{SW} | Switching frequency | Continuous-conduction mode, $V_{IN} = 13\text{ V}$, $V_{OUT} \geq 1\text{ V}$ | | 1000 | | kHz |
| BUCK CONVERTERS | | | | | | |
| t_{PG} | Total turnon time | Measured from enable going high to when output reaches 90% of target value. | | 250 | 1000 | μs |
| f_{SW} | Switching frequency | Continuous-conduction mode | | See Figure 4-10 | | MHz |
| LDOax | | | | | | |
| $t_{STARTUP}$ | Start-up time | Measured from enable going high to when output reaches 95% of final value, $V_{OUT} = 1.2\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$ | | 180 | | μs |
| VTT LDO | | | | | | |
| $t_{STARTUP}$ | Start-up time | Measured from enable going high to PG assertion, $V_{OUT} = 0.675\text{ V}$, $C_{OUT} = 40\text{ }\mu\text{F}$ | | 22 | | μs |
| SWA1 | | | | | | |
| $t_{TURN-ON}$ | Turnon time | Measured from enable going high to reach 95% of final value, $V_{IN} = 3.3\text{ V}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ | | 0.85 | | ms |
| | | Measured from enable going high to reach 95% of final value, $V_{IN} = 1.8\text{ V}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ | | 0.63 | | ms |
| SWB1_2 | | | | | | |
| $t_{TURN-ON}$ | Turnon time | Measured from enable going high to reach 95% of final value, $V_{IN} = 3.3\text{ V}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ | | 1.1 | | ms |
| | | Measured from enable going high to reach 95% of final value, $V_{IN} = 1.8\text{ V}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ | | 0.82 | | ms |

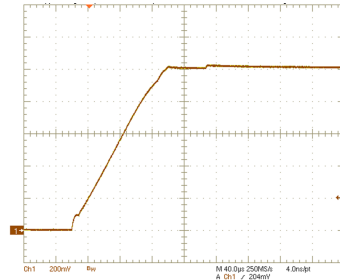
4.16 Typical Characteristics

Measurements are taken at 25°C.



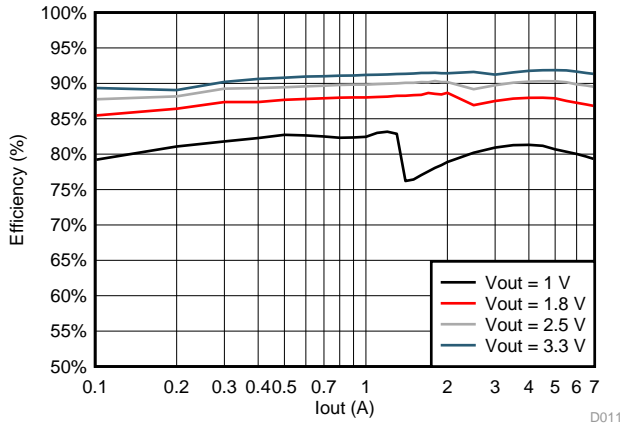
FET = CSD87588N L = PIMB061H-R22ms
 BUCK2_MODE = 0b C_{OUT} = 2 × 150 μF + 1 × 22 μF

Figure 4-1. Example BUCK2 Controller Start-Up



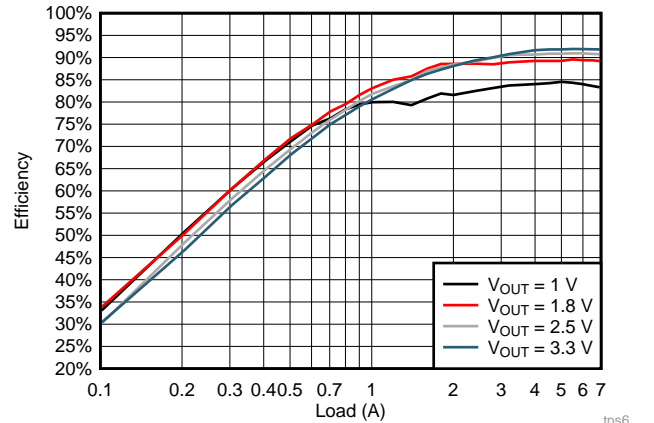
BUCK3_MODE = 0b L = PIFE32251B-R47ms
 C_{OUT} = 4 × 22 μF

Figure 4-2. Example BUCK3 Converter Start-Up



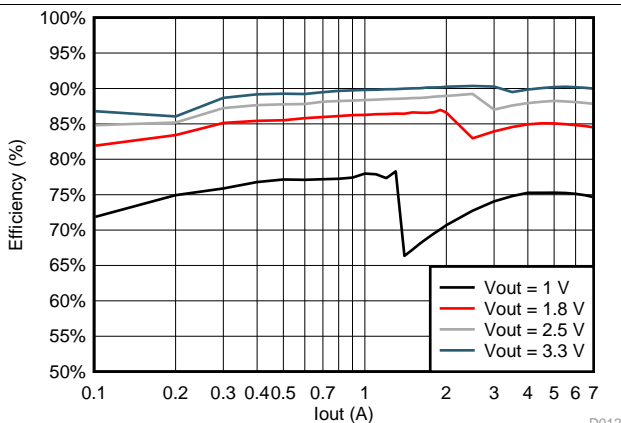
FET = CSD87381P L = PIMB061H-R47ms
 BUCK1_MODE = 0b

Figure 4-3. Example BUCK1 Efficiency at V_{IN} = 13 V In Auto Mode



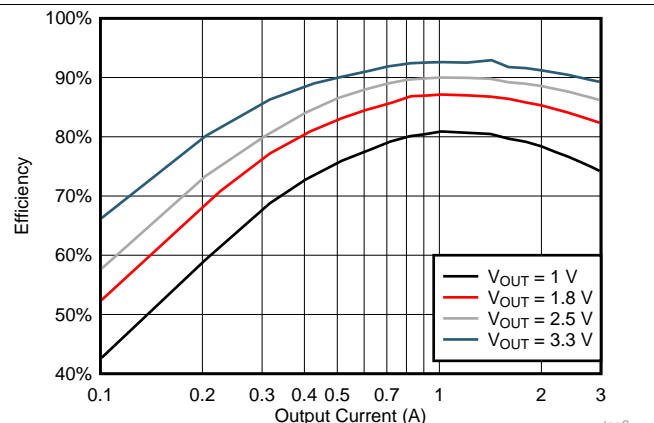
FET = CSD87381P L = PIMB061H-R47ms
 BUCK1_MODE = 1b

Figure 4-4. Example BUCK1 Efficiency at V_{IN} = 13 V in Forced PWM Mode



FET = CSD87381P L = PIMB061H-R47ms
 BUCK1_MODE = 0b

Figure 4-5. Example BUCK1 Efficiency at V_{IN} = 18 V In Auto Mode



L = PIFE32251B-R47ms

Figure 4-6. Example BUCK3 Efficiency at V_{IN} = 5 V

Typical Characteristics (continued)

Measurements are taken at 25°C.

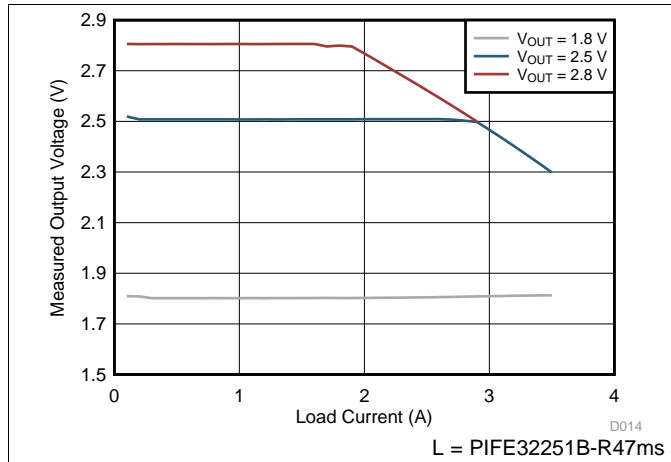


Figure 4-7. Converter Load Current Limitations with $V_{IN} = 3.3\text{ V}$

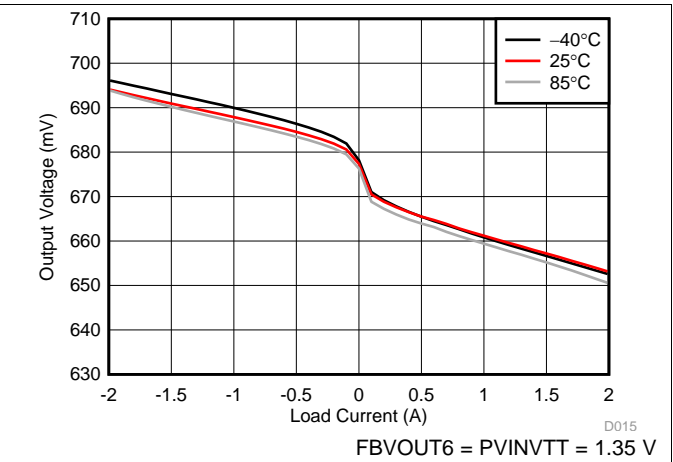


Figure 4-8. VTT LDO Regulation

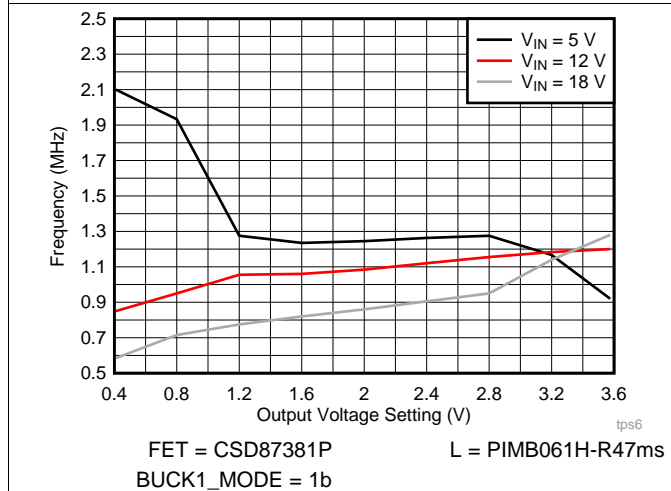


Figure 4-9. Controller Switching Frequency (Forced PWM Mode)

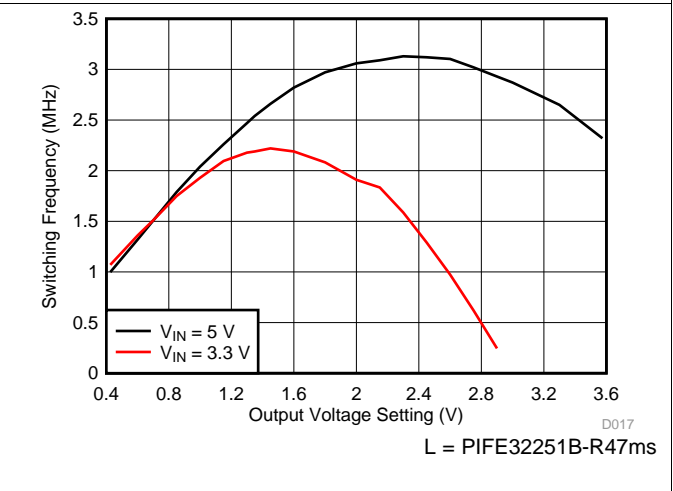


Figure 4-10. Converter Switching Frequency

5 Detailed Description

5.1 Overview

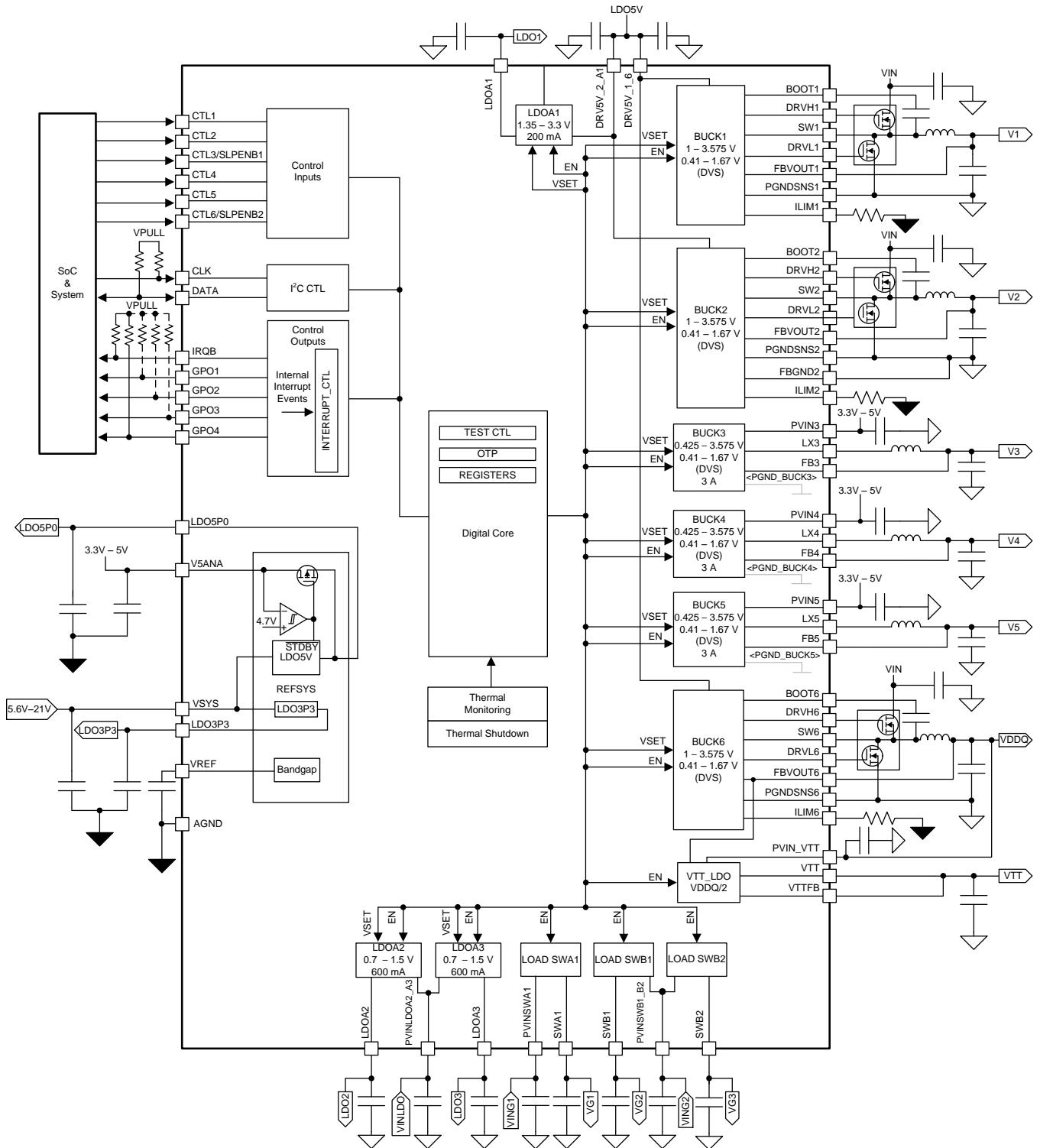
The TPS650861 power-management integrated circuit (PMIC) provides a highly flexible, programmable, and configurable power solution that can power a wide array of processors along with DDR3/DDR4 memory and other peripherals. Integrated in the PMIC are three step-down controllers (BUCK1, BUCK2, and BUCK6), three step-down converters (BUCK3, BUCK4, and BUCK5), a sink or source LDO (VTT LDO), three low-voltage V_{IN} LDOs (LDOA1–LDOA3), and three load switches (SWA1, SWB1, and SWB2). With on-chip one-time programmable (OTP) memory, configuration of each rail for default output value, power-up sequence, fault handling, and Power Good mapping into a GPO pin are all conveniently flexible. The TPS650861 has two OTP memory banks which are designed to be programmed to fit different designs. (See [Section 5.7](#)) All VRs have a built-in discharge resistor, and the value can be changed using the DISCHCNT1–DISCHCNT3 and LDOA1_SWB2_CTRL registers. When enabling a VR, the PMIC automatically disconnects the discharge resistor for that rail without any I²C command. lists the key characteristics of the voltage rails.

Table 5-1. Summary of Voltage Regulators

| RAIL | TYPE | INPUT VOLTAGE (V) | | OUTPUT VOLTAGE RANGE (V) | | | CURRENT (mA) |
|-----------|----------------------|-------------------|------|--------------------------|------------------|-------|--------------------|
| | | MIN | MAX | MIN | TYP | MAX | |
| BUCK1 | Step-down controller | 4.5 | 21 | 0.41 | OTP-programmable | 3.575 | scalable |
| BUCK2 | Step-down controller | 4.5 | 21 | 0.41 | OTP-programmable | 3.575 | scalable |
| BUCK3 | Step-down converter | 3 | 5.5 | 0.41 | OTP-programmable | 3.575 | 3000 |
| BUCK4 | Step-down Converter | 3 | 5.5 | 0.41 | OTP-programmable | 3.575 | 3000 |
| BUCK5 | Step-down converter | 3 | 5.5 | 0.41 | OTP-programmable | 3.575 | 3000 |
| BUCK6 | Step-down controller | 4.5 | 21 | 0.41 | OTP-programmable | 3.575 | scalable |
| LDOA1 | LDO | 4.5 | 5.5 | 1.35 | OTP-programmable | 3.3 | 200 ⁽¹⁾ |
| LDOA2 | LDO | 1.62 | 1.98 | 0.7 | OTP-programmable | 1.5 | 600 |
| LDOA3 | LDO | 1.62 | 1.98 | 0.7 | OTP-programmable | 1.5 | 600 |
| SWA1 | Load switch | 0.5 | 3.3 | | | | 300 |
| SWB1/SWB2 | Load switch | 0.5 | 3.3 | | | | 400 |
| VTT | Sink and source LDO | 1.1 | 1.8 | | FBVOUT6 / 2 | | OTP-programmable |

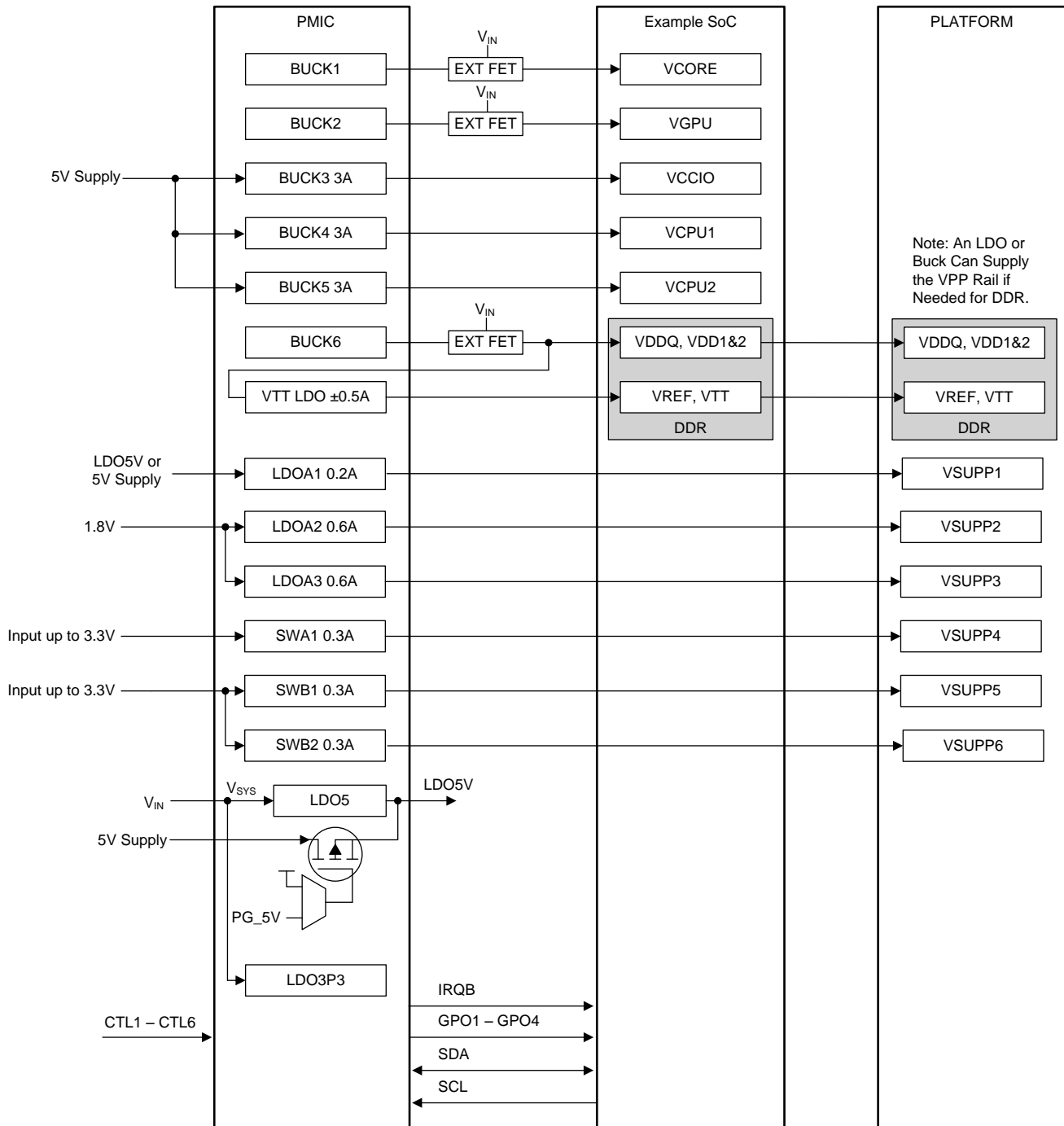
(1) When powered from a 5-V supply through the DRV5V_2_A1 pin. Otherwise, max current is limited by max I_{OUT} of LDO5.

5.2 Functional Block Diagram



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Figure 5-1. PMIC Functional Block Diagram



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Figure 5-2. Power Map Example

5.3 Programming the TPS650861

Detailed information regarding the programming of the non-volatile one-time programmable (OTP) memory is available in the [TPS65086100 OTP Memory Programming Guide](#).

5.4 SMPS Voltage Regulators

The buck controllers integrate gate drivers for external power stages with programmable current limit (set by an external resistor at ILIMx pin), which allows for optimal selection of external passive components based on the desired system load. The buck converters include integrated power stage and require a minimum number of pins for power input, inductor, and output voltage feedback input. Combined with high-frequency switching, all these features allow use of inductors in small form factor, thus reducing total-system cost and size.

The controllers, BUCK1, BUCK2, and BUCK6, have selectable auto- and forced-pulse width modulation (PWM) mode through the BUCKx_MODE bit in the BUCKxCTRL register. In auto mode, the VR automatically switches between PWM and pulsed frequency modulation (PFM) (discontinuous conduction mode) depending on the output load to maximize efficiency. In Force PWM mode, the VR remains in PWM (constant conduction mode) in order to keep the regulator switching even at low load to prevent switching noise in the audible range. The converters, BUCK3, BUCK4, and BUCK5, only support Forced PWM mode.

All controllers and converters can be used with the default V_{OUT} or can have their voltage dynamically changed at any time. This means that the rails can be default programmed for any available V_{OUT} by OTP programming locally or at the factory, so the device starts up with the default voltage, or during operation the rail can be configured by I²C to another operating V_{OUT} while the rail is enable or disabled. There are two step sizes or ranges available for V_{OUT} selection for controllers: 10-mV and 25-mV steps. The step-size range must be selected prior to use and must be programmed in the OTP locally or at the factory. It is not subject to change during operation.

For the 10-mV step-size range V_{OUT} options, see [Table 5-2](#). For the 25-mV step-size range V_{OUT} options, see [Table 5-3](#).

Table 5-2. 10-mV Step-Size V_{OUT} Range

| VID BITS | V _{OUT} | VID BITS | V _{OUT} | VID BITS | V _{OUT} |
|----------|------------------|----------|------------------|----------|------------------|
| 0000000 | 0 | 0101011 | 0.83 | 1010110 | 1.26 |
| 0000001 | 0.41 | 0101100 | 0.84 | 1010111 | 1.27 |
| 0000010 | 0.42 | 0101101 | 0.85 | 1011000 | 1.28 |
| 0000011 | 0.43 | 0101110 | 0.86 | 1011001 | 1.29 |
| 0000100 | 0.44 | 0101111 | 0.87 | 1011010 | 1.30 |
| 0000101 | 0.45 | 0110000 | 0.88 | 1011011 | 1.31 |
| 0000110 | 0.46 | 0110001 | 0.89 | 1011100 | 1.32 |
| 0000111 | 0.47 | 0110010 | 0.90 | 1011101 | 1.33 |
| 0001000 | 0.48 | 0110011 | 0.91 | 1011110 | 1.34 |
| 0001001 | 0.49 | 0110100 | 0.92 | 1011111 | 1.35 |
| 0001010 | 0.50 | 0110101 | 0.93 | 1100000 | 1.36 |
| 0001011 | 0.51 | 0110110 | 0.94 | 1100001 | 1.37 |
| 0001100 | 0.52 | 0110111 | 0.95 | 1100010 | 1.38 |
| 0001101 | 0.53 | 0111000 | 0.96 | 1100011 | 1.39 |
| 0001110 | 0.54 | 0111001 | 0.97 | 1100100 | 1.40 |
| 0001111 | 0.55 | 0111010 | 0.98 | 1100101 | 1.41 |
| 0010000 | 0.56 | 0111011 | 0.99 | 1100110 | 1.42 |
| 0010001 | 0.57 | 0111100 | 1.00 | 1100111 | 1.43 |
| 0010010 | 0.58 | 0111101 | 1.01 | 1101000 | 1.44 |
| 0010011 | 0.59 | 0111110 | 1.02 | 1101001 | 1.45 |
| 0010100 | 0.60 | 0111111 | 1.03 | 1101010 | 1.46 |
| 0010101 | 0.61 | 1000000 | 1.04 | 1101011 | 1.47 |
| 0010110 | 0.62 | 1000001 | 1.05 | 1101100 | 1.48 |
| 0010111 | 0.63 | 1000010 | 1.06 | 1101101 | 1.49 |
| 0011000 | 0.64 | 1000011 | 1.07 | 1101110 | 1.50 |
| 0011001 | 0.65 | 1000100 | 1.08 | 1101111 | 1.51 |
| 0011010 | 0.66 | 1000101 | 1.09 | 1110000 | 1.52 |
| 0011011 | 0.67 | 1000110 | 1.10 | 1110001 | 1.53 |
| 0011100 | 0.68 | 1000111 | 1.11 | 1110010 | 1.54 |
| 0011101 | 0.69 | 1001000 | 1.12 | 1110011 | 1.55 |
| 0011110 | 0.70 | 1001001 | 1.13 | 1110100 | 1.56 |
| 0011111 | 0.71 | 1001010 | 1.14 | 1110101 | 1.57 |
| 0100000 | 0.72 | 1001011 | 1.15 | 1110110 | 1.58 |
| 0100001 | 0.73 | 1001100 | 1.16 | 1110111 | 1.59 |
| 0100010 | 0.74 | 1001101 | 1.17 | 1111000 | 1.60 |
| 0100011 | 0.75 | 1001110 | 1.18 | 1111001 | 1.61 |
| 0100100 | 0.76 | 1001111 | 1.19 | 1111010 | 1.62 |
| 0100101 | 0.77 | 1010000 | 1.20 | 1111011 | 1.63 |
| 0100110 | 0.78 | 1010001 | 1.21 | 1111100 | 1.64 |
| 0100111 | 0.79 | 1010010 | 1.22 | 1111101 | 1.65 |
| 0101000 | 0.80 | 1010011 | 1.23 | 1111110 | 1.66 |
| 0101001 | 0.81 | 1010100 | 1.24 | 1111111 | 1.67 |
| 0101010 | 0.82 | 1010101 | 1.25 | | |

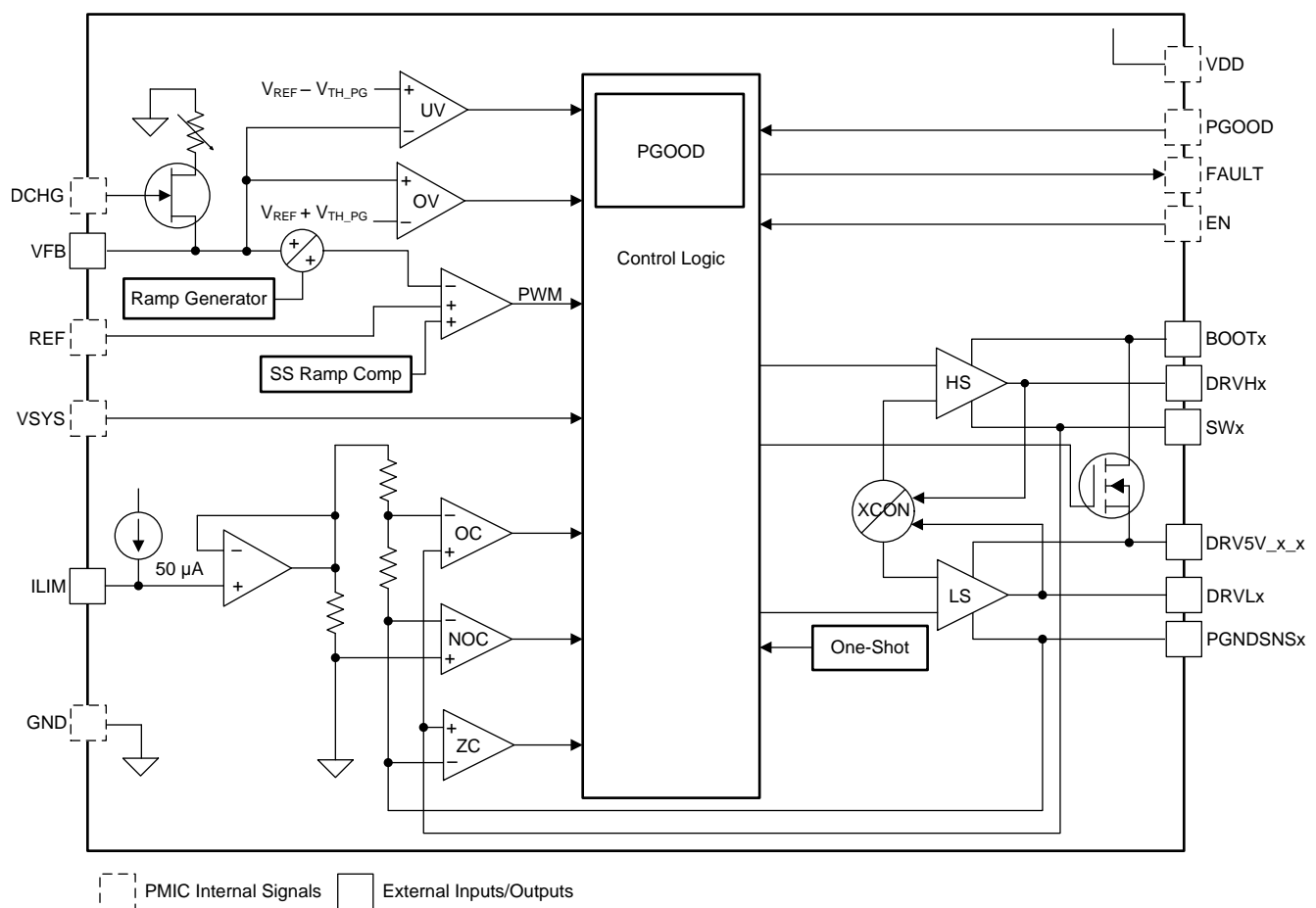
Table 5-3. 25-mV Step-Size V_{OUT} Range

| VID BITS | V _{OUT} (Converters) | V _{OUT} (Controllers) | VID BITS | V _{OUT} | VID BITS | V _{OUT} |
|----------|----------------------------------|-----------------------------------|----------|------------------|----------|------------------|
| 0000000 | 0 | 0 | 0101011 | 1.475 | 1010110 | 2.550 |
| 0000001 | 0.425 | 1.000 | 0101100 | 1.500 | 1010111 | 2.575 |
| 0000010 | 0.450 | 1.000 | 0101101 | 1.525 | 1011000 | 2.600 |
| 0000011 | 0.475 | 1.000 | 0101110 | 1.550 | 1011001 | 2.625 |
| 0000100 | 0.500 | 1.000 | 0101111 | 1.575 | 1011010 | 2.650 |
| 0000101 | 0.525 | 1.000 | 0110000 | 1.600 | 1011011 | 2.675 |
| 0000110 | 0.550 | 1.000 | 0110001 | 1.625 | 1011100 | 2.700 |
| 0000111 | 0.575 | 1.000 | 0110010 | 1.650 | 1011101 | 2.725 |
| 0001000 | 0.600 | 1.000 | 0110011 | 1.675 | 1011110 | 2.750 |
| 0001001 | 0.625 | 1.000 | 0110100 | 1.700 | 1011111 | 2.775 |
| 0001010 | 0.650 | 1.000 | 0110101 | 1.725 | 1100000 | 2.800 |
| 0001011 | 0.675 | 1.000 | 0110110 | 1.750 | 1100001 | 2.825 |
| 0001100 | 0.700 | 1.000 | 0110111 | 1.775 | 1100010 | 2.850 |
| 0001101 | 0.725 | 1.000 | 0111000 | 1.800 | 1100011 | 2.875 |
| 0001110 | 0.750 | 1.000 | 0111001 | 1.825 | 1100100 | 2.900 |
| 0001111 | 0.775 | 1.000 | 0111010 | 1.850 | 1100101 | 2.925 |
| 0010000 | 0.800 | 1.000 | 0111011 | 1.875 | 1100110 | 2.950 |
| 0010001 | 0.825 | 1.000 | 0111100 | 1.900 | 1100111 | 2.975 |
| 0010010 | 0.850 | 1.000 | 0111101 | 1.925 | 1101000 | 3.000 |
| 0010011 | 0.875 | 1.000 | 0111110 | 1.950 | 1101001 | 3.025 |
| 0010100 | 0.900 | 1.000 | 0111111 | 1.975 | 1101010 | 3.050 |
| 0010101 | 0.925 | 1.000 | 1000000 | 2.000 | 1101011 | 3.075 |
| 0010110 | 0.950 | 1.000 | 1000001 | 2.025 | 1101100 | 3.100 |
| 0010111 | 0.975 | 1.000 | 1000010 | 2.050 | 1101101 | 3.125 |
| 0011000 | 1.000 | 1.000 | 1000011 | 2.075 | 1101110 | 3.150 |
| 0011001 | 1.025 | 1.025 | 1000100 | 2.100 | 1101111 | 3.175 |
| 0011010 | 1.050 | 1.050 | 1000101 | 2.125 | 1110000 | 3.200 |
| 0011011 | 1.075 | 1.075 | 1000110 | 2.150 | 1110001 | 3.225 |
| 0011100 | 1.100 | 1.100 | 1000111 | 2.175 | 1110010 | 3.250 |
| 0011101 | 1.125 | 1.125 | 1001000 | 2.200 | 1110011 | 3.275 |
| 0011110 | 1.150 | 1.150 | 1001001 | 2.225 | 1110100 | 3.300 |
| 0011111 | 1.175 | 1.175 | 1001010 | 2.250 | 1110101 | 3.325 |
| 0100000 | 1.200 | 1.200 | 1001011 | 2.275 | 1110110 | 3.350 |
| 0100001 | 1.225 | 1.225 | 1001100 | 2.300 | 1110111 | 3.375 |
| 0100010 | 1.250 | 1.250 | 1001101 | 2.325 | 1111000 | 3.400 |
| 0100011 | 1.275 | 1.275 | 1001110 | 2.350 | 1111001 | 3.425 |
| 0100100 | 1.300 | 1.300 | 1001111 | 2.375 | 1111010 | 3.450 |
| 0100101 | 1.325 | 1.325 | 1010000 | 2.400 | 1111011 | 3.475 |
| 0100110 | 1.350 | 1.350 | 1010001 | 2.425 | 1111100 | 3.500 |
| 0100111 | 1.375 | 1.375 | 1010010 | 2.450 | 1111101 | 3.525 |
| 0101000 | 1.400 | 1.400 | 1010011 | 2.475 | 1111110 | 3.550 |
| 0101001 | 1.425 | 1.425 | 1010100 | 2.500 | 1111111 | 3.575 |
| 0101010 | 1.450 | 1.450 | 1010101 | 2.525 | | |

5.4.1 Controller Overview

The controllers are fast-reacting, high-frequency, scalable output power controllers capable of driving two external N-MOSFETs. They are D-CAP2 controller scheme that optimizes transient responses at high load currents for such applications as CORE and DDR supplies. The output voltage is compared with internal reference voltage after divider resistors. The PWM comparator determines the timing to turn on the high-side MOSFET. The PWM comparator response maintains a very small PWM output ripple voltage. Because the device does not have a dedicated oscillator for control loop on board, switching cycle is controlled by the adaptive on-time circuit. The on-time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the on-time one-shot timer.

The D-CAP2 control scheme has an injected ripple from the SW node that is added to the reference voltage to simulate output ripple, which eliminates the need for ESR-induced output ripple from D-CAP™ mode control. Thus, low-ESR output capacitors (such as low-cost ceramic MLCC capacitors) can be used with the controllers.



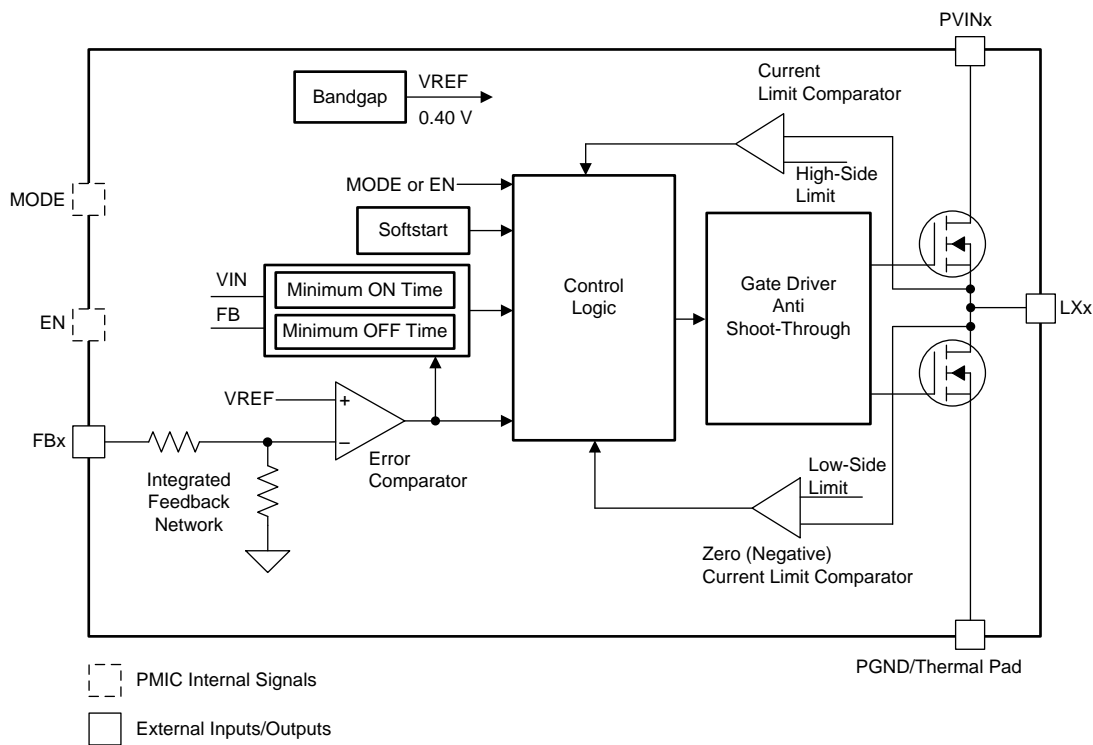
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Figure 5-3. Controller Block Diagram

5.4.2 Converter Overview

The PMIC synchronous step-down DCDC converters include a unique hysteretic PWM controller scheme which enables a high switching frequency converter, excellent transient and AC load regulation as well as operation with cost-competitive external components. The device operates on a quasi-fixed frequency and allows filtering of the switch noise by external filter components. The PMIC device offers fixed output voltage options featuring smallest solution size by using only three external components per converter.

A significant advantage of PMIC compared to other hysteretic PWM controller topologies is its excellent AC load transient regulation capability. When the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high-side switch is turned on. The high-side switch remains turned on until a minimum ON-time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high-side switch current limit. When the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high-side switch turns on again. In PWM mode operation, negative inductor current is allowed to enable continuous conduction mode even at no load condition.



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Figure 5-4. Converter Block Diagram

5.4.3 DVS

BUCK1–BUCK6 support dynamic voltage scaling (DVS) for maximum system efficiency. The VR outputs can slew up and down in either 10-mV or 25-mV steps using the 7-bit voltage ID (VID) defined in Section 4.7 and Section 4.8. DVS slew rate is minimum 2.5 mV/μs. In order to meet the minimum slew rate, VID progresses to the next code at 3-μs (nom) interval per 10-mV or at 6-μs interval per 25-mV steps. When DVS is active, the VR is forced into PWM mode, unless BUCKx_DECAY = 1, to ensure the output keeps track of VID code with minimal delay. Additionally, PGOOD is masked when DVS is in progress. Figure 5-5 shows an example of slew down and up from one VID to another (step size of 10 mV).

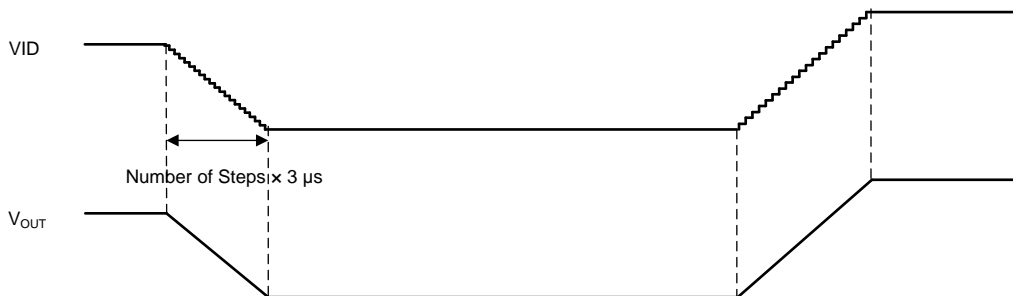


Figure 5-5. DVS Timing Diagram I (BUCKx_DECAY = 0)

As shown in Figure 5-6, if a BUCKx_VID[6:0] is set to 7b000 0000, its output voltage will slew down to the minimum VID value first, and then will drift down to 0 V as the SMPS stops switching. Subsequently, if a BUCKx_VID[6:0] is set to a value (neither 7b000 0000 nor 7b000 0001) when its output voltage is less than 0.5 V, the VR will ramp up to 0.5 V first with soft-start kicking in, then will slew up to target voltage in the slew rate aforementioned. It must be noted that a fixed 200 μs of soft-start time is reserved for V_{OUT} to reach 0.5 V.

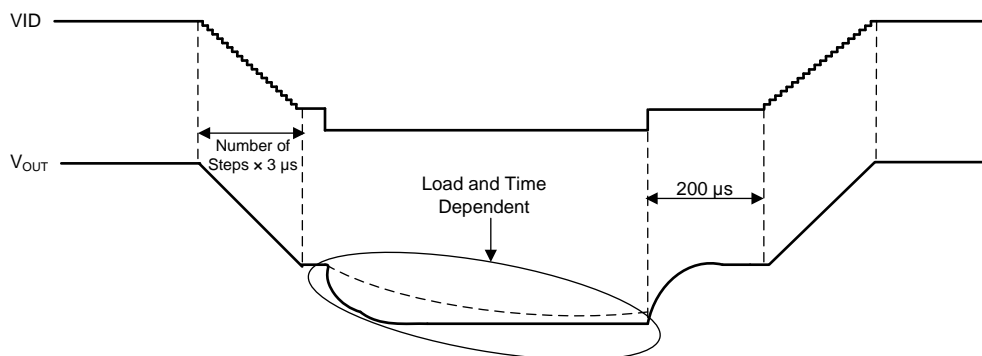


Figure 5-6. DVS Timing Diagram II (BUCKx_DECAY = 0)

5.4.4 Decay

In addition to DVS, BUCK1–BUCK6 can decay down to a lower voltage when BUCKx_DECAY bit in BUCKxCTRL register is set to 1. Decay mode is only used in a downward direction of VID. The VR does not control slew rate. As both high-side and low-side FETs stop switching, the output voltage ramps down naturally, dictated by current drawn from the load and output filtering capacitance. When the VR is in the middle of decay down its PGOOD is masked until V_{OUT} falls below the over-voltage (OV) threshold of the set VID value. Figure 5-7 shows two cases that differ from each other as to whether V_{OUT} has reached the target voltage corresponding to a new VID when the VR is commanded to slew back up to a higher voltage. In case that V_{OUT} has not decayed down below VID as denoted case 2, the VR will wait for VID to catch up, and then V_{OUT} will start ramping up to keep up with the VID ramp.

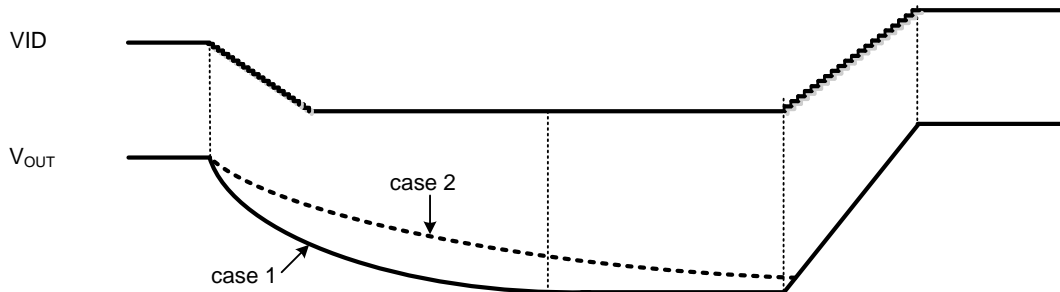


Figure 5-7. Decay Down to a Lower V_{OUT} and Slew Up

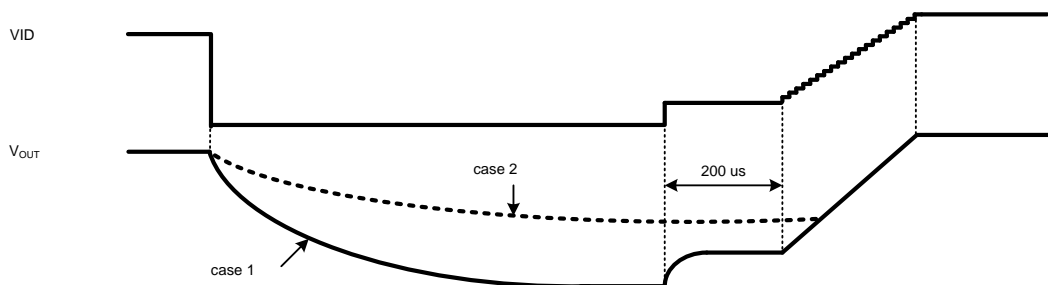


Figure 5-8. Decay Down to 0 V and Slew Up

5.4.5 Current Limit

The buck controllers (BUCK1, BUCK2, and BUCK6) have inductor-valley current-limit architecture and the current limit is programmable by an external resistor at the ILIMx pin. Equation 1 shows the calculation for a desired resistor value, depending on specific application conditions. I_{LIMREF} is the current source out of the ILIMx pin that is typically 50 μ A, and R_{DSON} is the maximum channel resistance of the low-side FET. The scaling factor is 1.3 to take into account all errors and temperature variations of R_{DSON} , I_{LIMREF} , and R_{ILIM} . Finally, 8 is another scaling factor associated with I_{LIMREF} .

$$R_{ILIM} = \frac{R_{DSON} \times 8 \times 1.3 \times \left(I_{LIM} - \frac{I_{ripple(min)}}{2} \right)}{I_{LIMREF}}$$

where

- I_{LIM} is the target current limit. An appropriate margin must be allowed when determining I_{LIM} from maximum output DC load current.
- $I_{ripple(min)}$ is the minimum peak-to-peak inductor ripple current for a given V_{OUT} . (1)

$$I_{ripple(min)} = \frac{V_{OUT} (V_{IN(MIN)} - V_{OUT})}{L_{max} \times V_{IN(MIN)} \times f_{sw(max)}}$$

where

- L_{max} is maximum inductance
- $f_{sw(max)}$ is maximum switching frequency
- $V_{IN(MIN)}$ minimum input voltage to the external power stage (2)

The buck converter limit inductor peak current cycle-by-cycle to I_{IND_LIM} is specified in Section 4.8.

The current limit circuit also protects against reverse current going back into the low side FET from the load. When operating in Force PWM mode, the inductor current is expected to go negative so it is important to ensure that the R_{ILIM} value is sufficient to account for this. If operating in PFM, this can be neglected. The equation for Force PWM minimum R_{ILIM} value is:

$$R_{ILIM} \geq \frac{R_{DSON} \times 8 \times 1.3 \times \left(\frac{I_{ripple(max)}}{2} \right)}{I_{LIMREF}}$$

where

- $I_{ripple(max)}$ is the maximum peak-to-peak inductor ripple current for a given V_{OUT} . (3)

$$I_{ripple(max)} = \frac{V_{OUT} (V_{IN(MAX)} - V_{OUT})}{L_{min} \times V_{IN(MAX)} \times f_{sw(min)}}$$

where

- L_{min} is minimum inductance
- $f_{sw(min)}$ is minimum switching frequency
- $V_{IN(MAX)}$ maximum input voltage to the external power stage (4)

If R_{ILIM} is too low for the chosen inductor and voltage conditions, then the ripple current at no load will trigger the negative current limit, forcing the low side FET to turn off. This will eventually result in the output voltage increasing above target regulation point due to irregular duty cycle created by current limit being triggered.

5.5 LDOs and Load Switches

5.5.1 VTT LDO

Typically powered from the BUCK6 output, the VTT LDO tracks FBVOUT6 and regulates its output to FBVOUT6 / 2. The LDO current limit is OTP dependent, and it is designed specifically to power DDR memory. The LDO core is a transconductance amplifier with large gain, and it drives a current output stage that either sources or sinks current depending on the deviation of the VTTFB pin voltage from the target regulation voltage.

5.5.2 LDOA1–LDOA3

The TPS650861 device integrates three general purpose LDOs. LDOA1 is powered from a 5-V supply through the DRV5V_2_A1 pin and it can be factory configured to be an Always-On rail (stay on even in case of emergency shutdown) as long as a valid power supply is available at VSYS. See [Table 5-4](#) for LDOA1 output voltage options. LDOA2 and LDOA3 share a power input pin (PVINLDOA2_A3). The output regulation voltages are set by writing to LDOAx_VID[3:0] bits (Reg 0x9A, 0x9B, and 0xAE). See [Table 5-5](#) for LDOA2 and LDOA3 output voltage options. LDOA1 is controlled by the LDOA1_SWB2_CTRL register.

Table 5-4. LDOA1 Output Voltage Options

| VID BITS | V _{OUT} | VID BITS | V _{OUT} | VID BITS | V _{OUT} | VID BITS | V _{OUT} |
|----------|------------------|----------|------------------|----------|------------------|----------|------------------|
| 0000 | 1.35 | 0100 | 1.8 | 1000 | 2.3 | 1100 | 2.85 |
| 0001 | 1.5 | 0101 | 1.9 | 1001 | 2.4 | 1101 | 3.0 |
| 0010 | 1.6 | 0110 | 2.0 | 1010 | 2.5 | 1110 | 3.3 |
| 0011 | 1.7 | 0111 | 2.1 | 1011 | 2.6 | 1111 | Not Used |

Table 5-5. LDOA2 and LDOA3 Output Voltage Options

| VID BITS | V _{OUT} | VID BITS | V _{OUT} | VID BITS | V _{OUT} | VID BITS | V _{OUT} |
|----------|------------------|----------|------------------|----------|------------------|----------|------------------|
| 0000 | 0.70 | 0100 | 0.90 | 1000 | 1.10 | 1100 | 1.30 |
| 0001 | 0.75 | 0101 | 0.95 | 1001 | 1.15 | 1101 | 1.35 |
| 0010 | 0.80 | 0110 | 1.00 | 1010 | 1.20 | 1110 | 1.40 |
| 0011 | 0.85 | 0111 | 1.05 | 1011 | 1.25 | 1111 | 1.50 |

5.5.3 Load Switches

The PMIC features three general-purpose load switches. SWA1 has its own power input pin (PVINSWA1), while SWB1 and SWB2 share one power input pin (PVINSWB1_B2). All switches have built-in slew rate control during start-up to limit the inrush current.

5.6 Power Goods (PGOOD or PG) and GPOs

The device provides information on status of VRs through four GPO pins along with Power Good Status registers defined in [Section 5.11.50](#) and [Section 5.11.51](#). Power Good information of any individual VR and load switch can be assigned to be part of the PGOOD tree as defined from [Section 5.11.40](#) to [Section 5.11.47](#). PGOOD assertion delays are programmable from 0 ms to 15 ms for GPO1, 5 ms to 100 ms for GPO3, and 0 ms to 100 ms for GPO2 and GPO4, respectively, as are defined in [Section 5.11.21](#) and [Section 5.11.34](#).

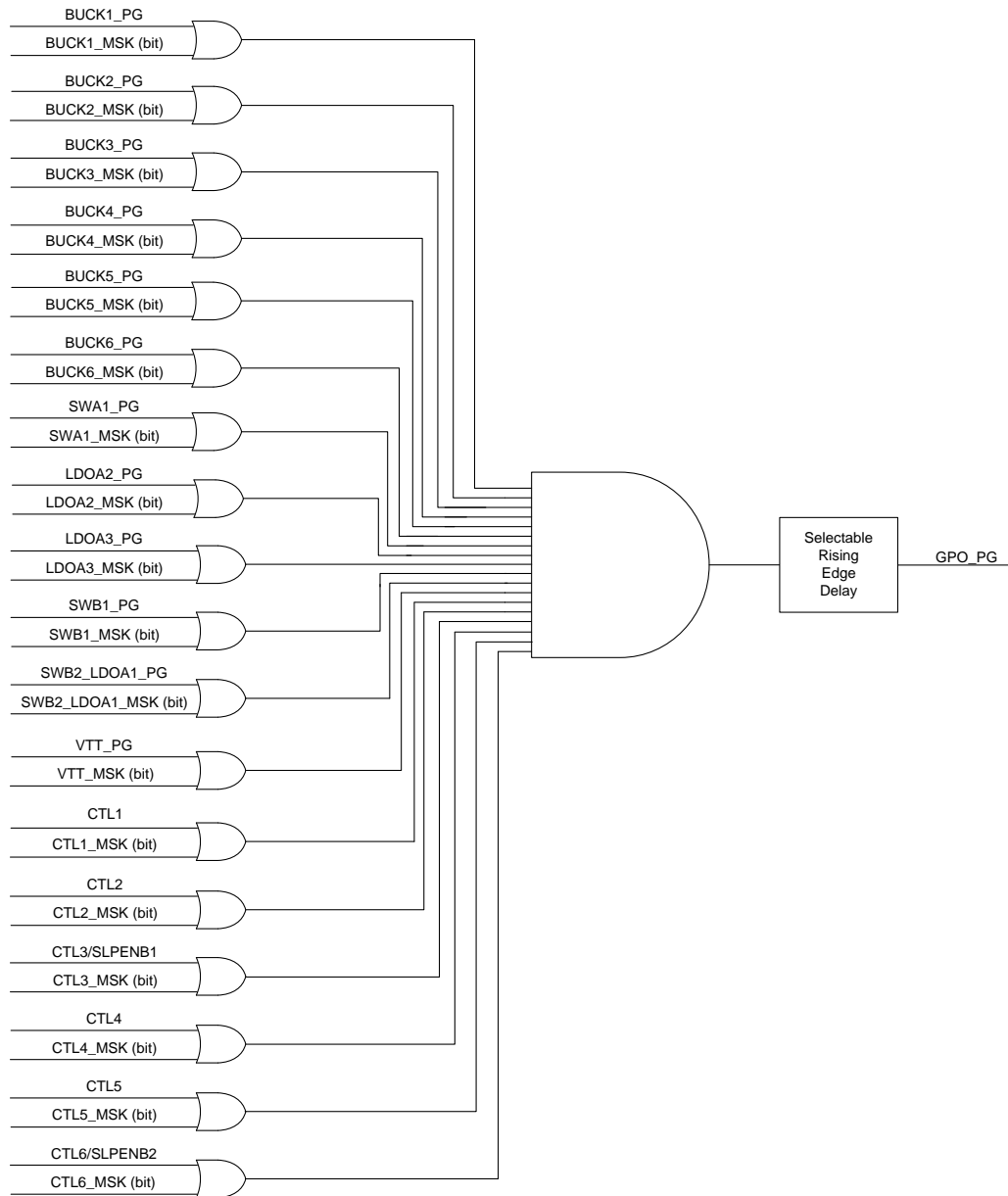


Figure 5-9. Power Good Tree

Alternatively, the GPOs can be used as general purpose outputs controlled by the user through I²C. Refer to the [Section 5.11.37](#) for details on controlling the GPOs in I²C control mode.

5.7 One-Time Programmable Memory

The PMIC has two banks of non-volatile one-time programmable (OTP) memory which stores the default settings for the device. The OTP memory is mapped to corresponding volatile registers which are cleared when VSYS goes below UVLO. When VSYS goes above UVLO, the contents of the OTP memory is loaded into the corresponding volatile registers which are then used to control the PMIC. The OTP is also reloaded in case of any emergency shutdown condition. When programming the PMIC, the values in the volatile registers which have OTP memory equivalents are burned into the OTP.

Some registers do not have OTP equivalent memory. For example, the IRQ register, which indicates which interrupts have been triggered, does not need OTP memory equivalent because its values are always determined after power up. Similarly, the IRQ_MASK register does not have OTP backing because in order to be useful, the processor needs to communicate with the PMIC to set the masks correctly. There is no need to have a default value other than 1b for these bits. OTP programmable bits are indicated with an 'X' in the register map. Some registers are accessed using I²C address 0x5E, which can be changed if necessary using the I2C_SLAVE_ADDR register (see [Section 5.12.39](#)). Other registers, which can only be accessed while in programming mode, are accessed using I²C address 0x38, which cannot be changed.

The OTP memory settings are set to 1b with a 7 V supply, in a process called "burning". Lower voltages may result in values not being stored or the bit flipping (from 1b to 0b) after some time has passed. To avoid this occurring, the IRQB pin should be probed with an oscilloscope during the prototyping phase of development to ensure it does not drop below 6.7 V during OTP memory burn in. Any bit can be burned from a 0b to a 1b, but once a bit is a 1b, it cannot go back to being a 0b. As a result, it is possible to burn an OTP program and then make minor changes and re-burn the OTP as long as all of the changes are 0b to 1b. For example, if the original OTP program had BUCK3_VID = 1 V (0011000b) then it can be changed to BUCK3_VID = 1.15 V (0011110b) without issue since it is just bits 1 and 2 being changed from 0b to 1b. However, if the new desired BUCK3_VID = 0.9 V (0010100b), then the second bank of OTP would need to be used since bit 3 cannot change from 1b to 0b. The switch from OTP Bank 0 to OTP Bank 1 is permanent as the pointer bit is also OTP.

Detailed information regarding the programming of the non-volatile one-time programmable (OTP) memory is available in the [TPS65086100 OTP Memory Programming Guide](#).

All OTP programmed settings should be validated during prototyping phase to ensure desired functionality because parts cannot be returned in case of incorrect programming. Any issues should be reported to http://e2e.ti.com/support/power_management/pmu/.

5.8 Power Sequencing and VR Control

The device has three different ways of sequencing the rails during power up and power down:

- Rail enabled by CTLx pin
- Rail enabled by Power Good (PG) of previously enabled rail
- Rail enabled by I²C software command

A delay can be added from any CTLx pin or PG to the enable of the subjected enabled rail. This creates a very flexible device capable of many sequence options. If a rail cannot be sequenced automatically, any rail can be enabled or disabled through an I²C command.

5.8.1 CTLx Sequencing

The device has six control-input pins (CTL1–CTL6) to control six SMPS regulators, three LDO regulators, and three load switches. This allows the user to define up to six distinctive groups, to which each VR can be assigned for highly flexible power sequencing. Of the six CTLx pins, CTL3 and CTL6 can be configured alternatively to active-low sleep enable pins. For instance, if a system level SLEEP state is defined such that BUCK1 output regulation voltage is lower than in the normal mode, then BUCK1 SLEEP state can be assigned to CTL3 or CTL6. By being pulled low, either CTL3 or CTL6 can be used to put BUCK1 into SLEEP state, and BUCK1 will regulate its output at a voltage defined by BUCK1_SLP_VID[6:0] in [Section 5.11.23](#). For a demonstration of this feature, [Figure 5-10](#) shows how BUCK1 is enabled from the CTL1 pin.

5.8.2 PG Sequencing

Any rail can be sequenced by the Power Good of a prior rail. This can be combined with the CTLx method to allow for further sequence control and create more distinctive groups of enables than the six from CTLx. This also allows some of the CTLx pins to be freed up for other purposes such as logic input gates. For a demonstration of this feature, [Figure 5-10](#) shows how the BUCK5 is enabled from the BUCK4 PG.

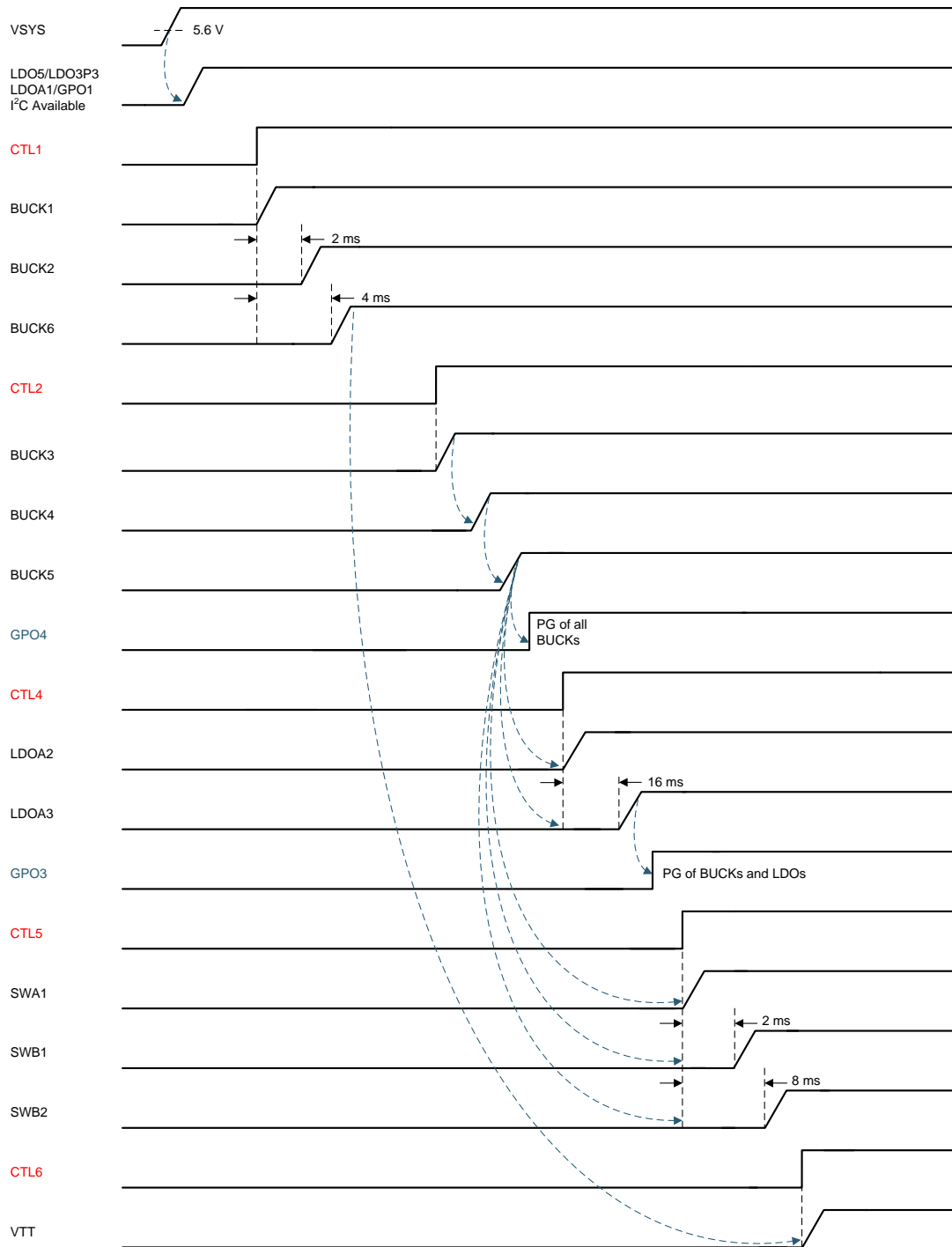


Figure 5-10. Generic Power-Up Sequence Example

5.8.3 Enable Delay

A delay can be added to the enable of any rail after the desired CTLx and PGs are met. This allows for the option to create additional timing groups from either CTLx pins or internal PGs. For a demonstration of this feature, Figure 5-10 shows how BUCK2 and BUCK6 are enabled after BUCK1 is enabled from CTL1 pin.

5.8.4 Power-Up Sequence

When a valid power supply is detected at the VSYS pin as V_{SYS} crosses above $V_{SYS_UVLO_5V} + V_{SYS_UVLO+5V_HYS}$, the power-up sequence is initiated by driving one of the control input pins high, followed by the rest of pins in order. [Figure 5-10](#) is an example where CTL1–CTL4 are defined to control four groups of VRs, while GPO3 and GPO4 are defined to provide a PGOOD status of two groups. The control input pins do not necessarily have to be pulled up in a staggered manner. For instance, if CTL2 is pulled up from the preceding group of VRs before PGOOD has been asserted at GPO1, the BUCK4 enable will be delayed until the PGOOD is asserted.

5.8.5 Power-Down Sequence

The power-down sequence can follow the CTLx pins, or be controlled with the I²C commands. If the internal PGs are used for sequencing or if some rails need to ramp down before others a delay can be added to the deassertion low of the internal enable of the subjected rail. This delay can be independent of the power-up delay option. Thus, power-up and power-down sequences can be different or similar to match the specific application sequences required.

Refer to [Figure 5-11](#) for an example of a power-down sequence demonstrating the delay disable of BUCK1 and BUCK2.

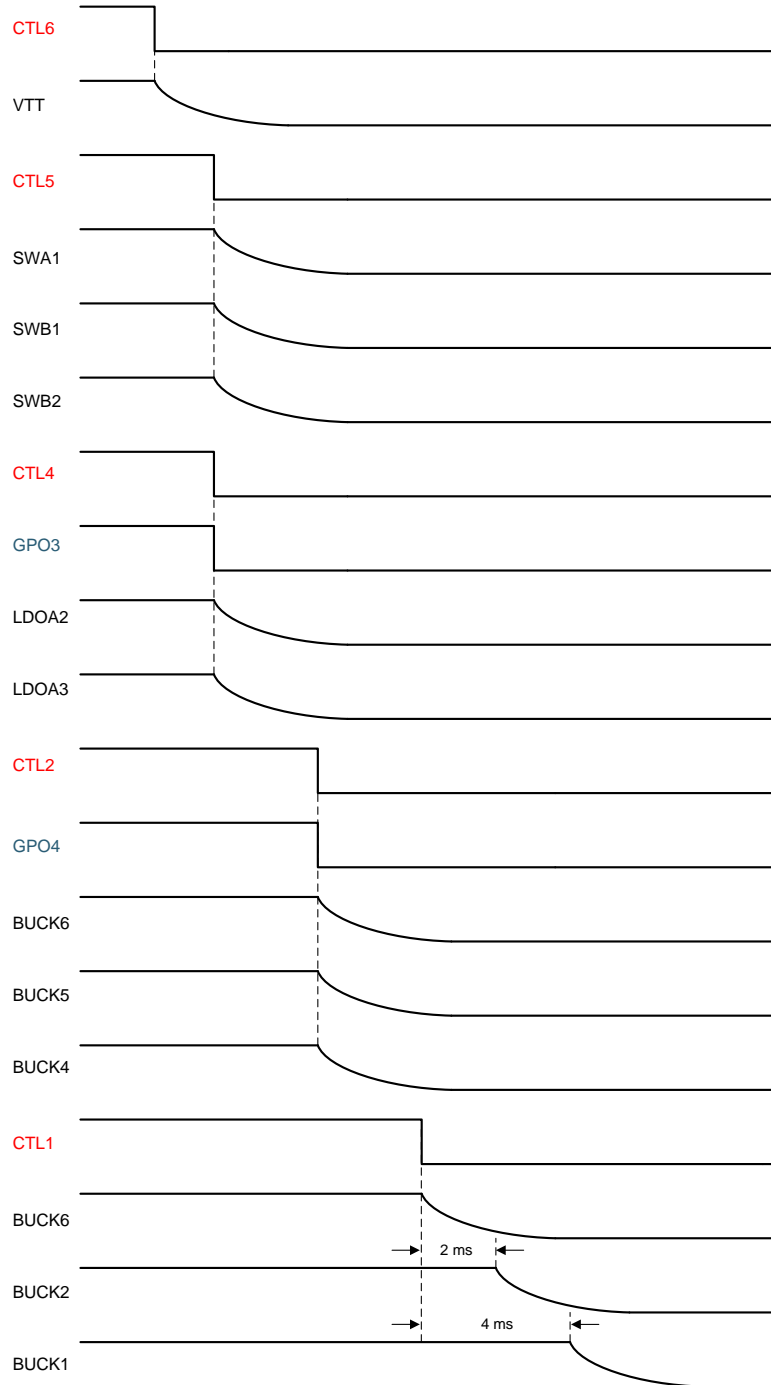


Figure 5-11. Generic Power-Down Sequence Example

5.8.6 Sleep State Entry and Exit

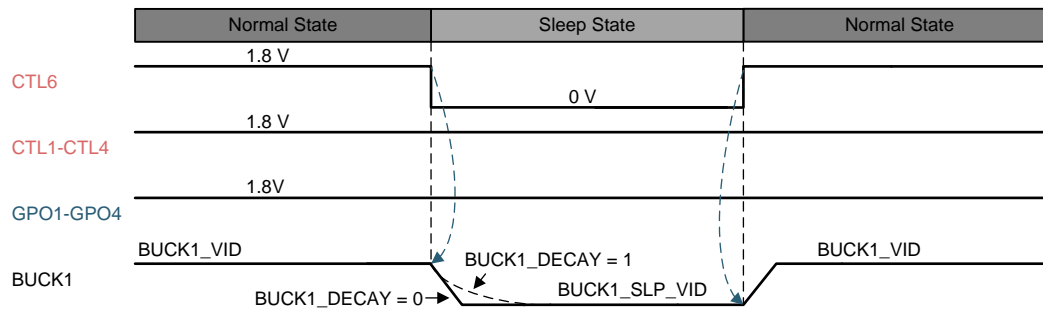


Figure 5-12. Sleep State Entry and Exit Sequence Example

Figure 5-12 shows an example where BUCK1 is defined to enter Sleep State in response to CTL6 going low.

NOTE

All PGOODs from GPO1–GPO4 can stay asserted during the entry and the exit. Depending on status of the BUCK1_DECAY bit defined in the BUCK1CTRL register, BUCK1 output will either decay or slew down to a new voltage defined in BUCK1_SLP_VID[6:0].

5.8.7 Emergency Shutdown

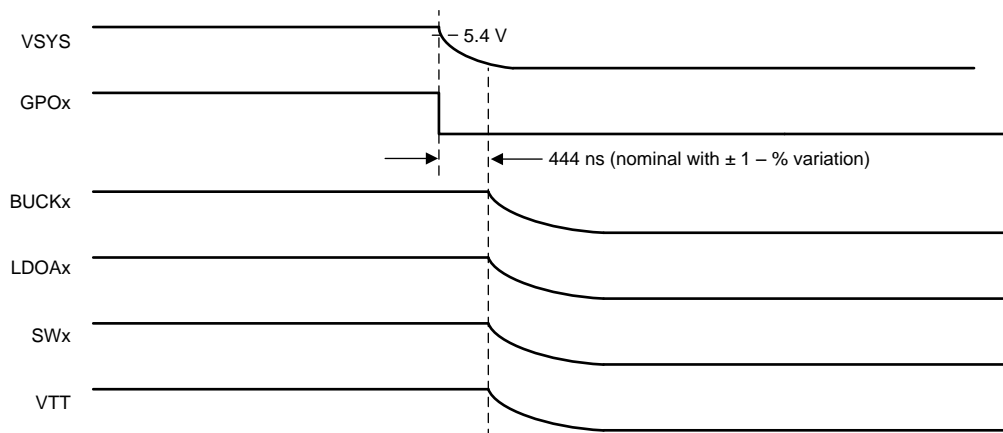


Figure 5-13. Emergency Shutdown Sequence

When V_{SYS} crosses below $V_{SYS_UVLO_5V}$, all Power Good pins will be deasserted, and after 444 ns (nom) of delay all VRs will shut down. Upon shutdown, all internal discharge resistors are set to 100 Ω to ensure timely decay of all VR outputs. Other conditions that will cause emergency shutdown are the die temperature rising above the critical temperature threshold (T_{CRIT}), deassertion of Power Good of any rail (configurable), or failure of any rail to reach power good within 10 ms of being enabled (configurable). If PMIC was shutdown by UVLO, it will wait until V_{SYS} rises above $V_{SYS_UVLO_5V} + V_{SYS_UVLO_5V_HYS}$ before reloading the default OTP and checking the state of the CTLx pins. If PMIC was shutdown by temperature, it will wait until temperature drops below $T_{CRIT} - T_{CRIT_HYS}$ before reloading OTP and checking the state of the CTLx pins. If the PMIC was shutdown by power fault, it will reload OTP after disabling all rails and check the state of the CTLx pins once OTP has finished reloading.

5.9 Device Functional Modes

5.9.1 Off Mode

When power supply at the VSYS pin is less than $V_{\text{SYS_UVLO_5V}}$ (5.4-V nominal) + $V_{\text{SYS_UVLO_5V_HYS}}$ (0.2-V nominal), the device is in off mode, where all output rails are disabled. If the supply voltage is greater than $V_{\text{SYS_UVLO_3V}}$ (3.6-V nominal) + $V_{\text{SYS_UVLO_3V_HYS}}$ (0.15-V nominal) while it is still less than $V_{\text{SYS_UVLO_5V}}$ + $V_{\text{SYS_UVLO_5V_HYS}}$, then the internal band-gap reference (VREF pin) along with LDO3P3 are enabled and regulated at target values.

5.9.2 Standby Mode

When power supply at the VSYS pin rises above $V_{\text{SYS_UVLO_5V}}$ + $V_{\text{SYS_UVLO_5V_HYS}}$, the device enters standby mode, where all internal reference and regulators (LDO3P3 and LDO5) are up and running, and I²C interface and CTL pins are ready to respond. All default registers defined in [Section 5.11](#) should have by now been loaded from one-time programmable (OTP) memory. Quiescent current consumption in standby mode is specified in [Section 4.5](#).

5.9.3 Active Mode

The device proceeds to active mode when any output rail is enabled either via an input pin as discussed in [Section 5.8](#) or by writing to EN bits through I²C. Output regulation voltage can also be changed by writing to VID bits defined in [Section 5.11](#).

5.10 I²C Interface

The I²C interface is a 2-wire serial interface developed by NXP™ (formerly Philips Semiconductor) (see I²C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, DATA and CLK. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The PMIC works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when V_{SYS} higher than $V_{\text{SYS_UVLO_5V}}$ is applied to the PMIC. The I²C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes are exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode.

The PMIC device supports 7-bit addressing; however, 10-bit addressing and general call address are not supported. The default device address is 0x5E, though it can be modified by programming. The programming registers are located in device address 0x38, which cannot be changed.

5.10.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high (see Figure 5-14). All I²C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 5-15). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 5-16), by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 5-14). This releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

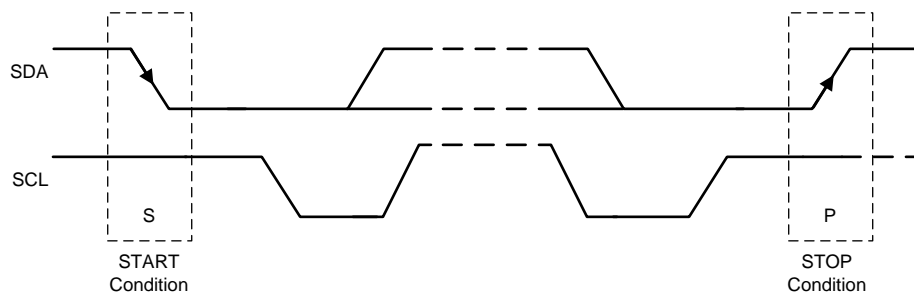


Figure 5-14. START and STOP Conditions

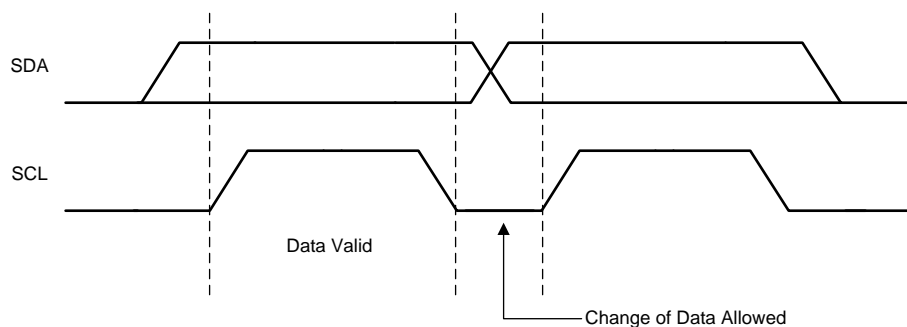


Figure 5-15. Bit Transfer on the I²C Bus

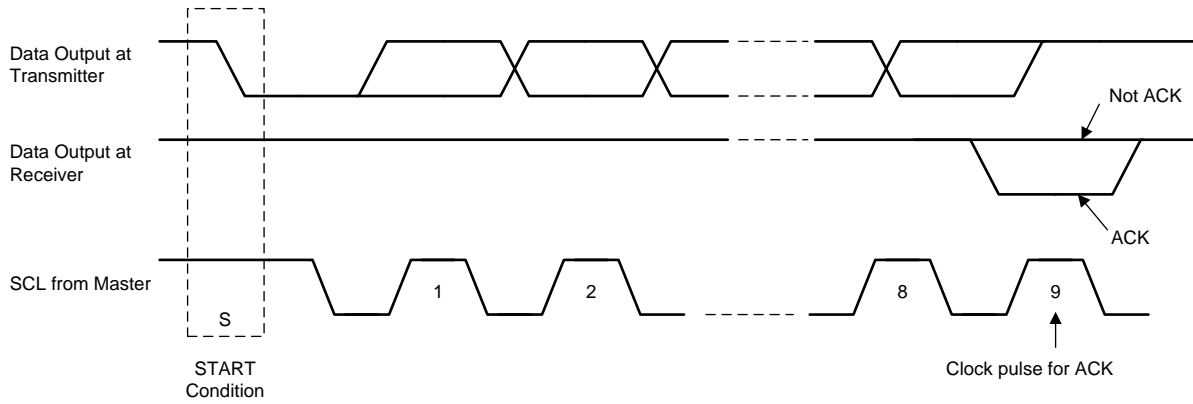


Figure 5-16. Acknowledge on the I²C Bus

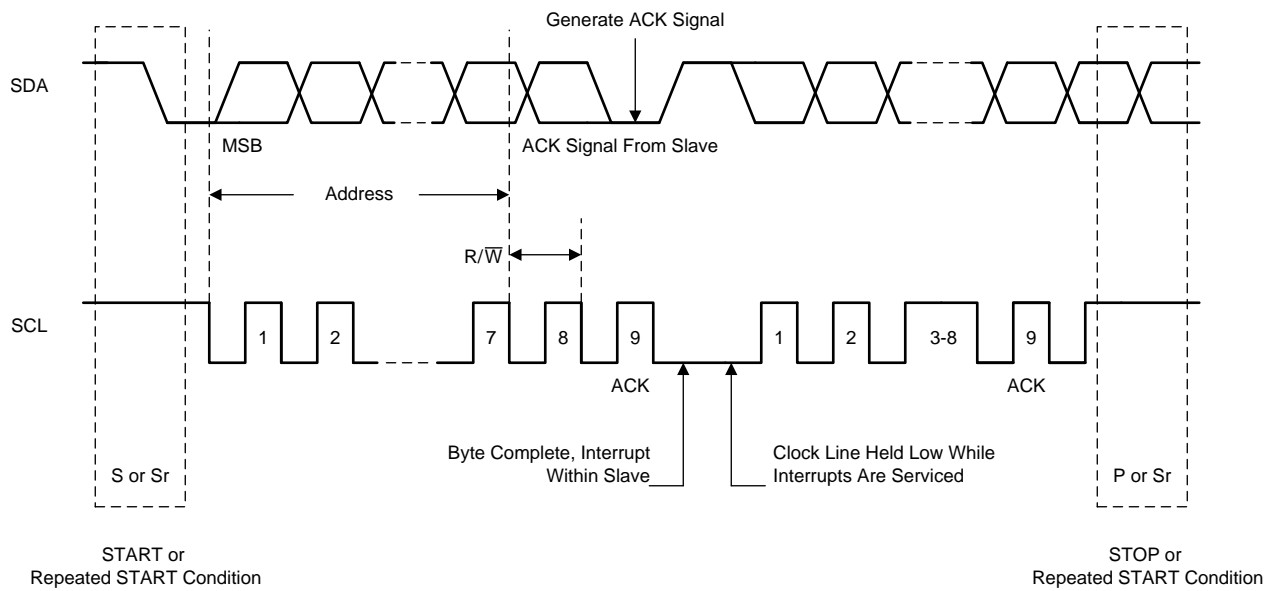


Figure 5-17. I²C Bus Protocol

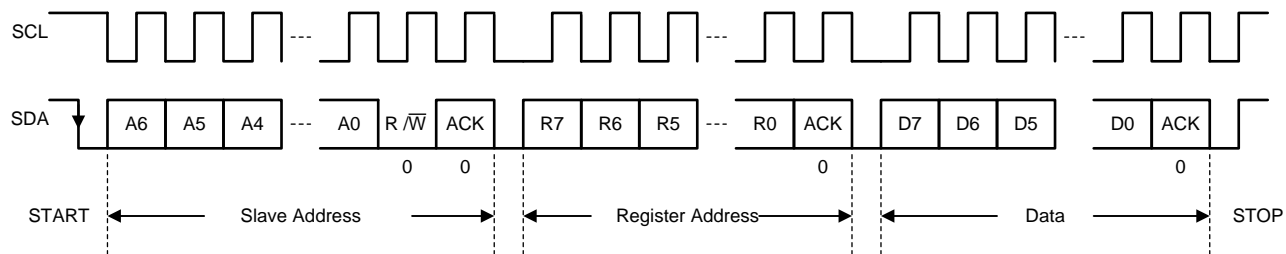


Figure 5-18. I²C Interface WRITE to TPS650861 in F/S Mode

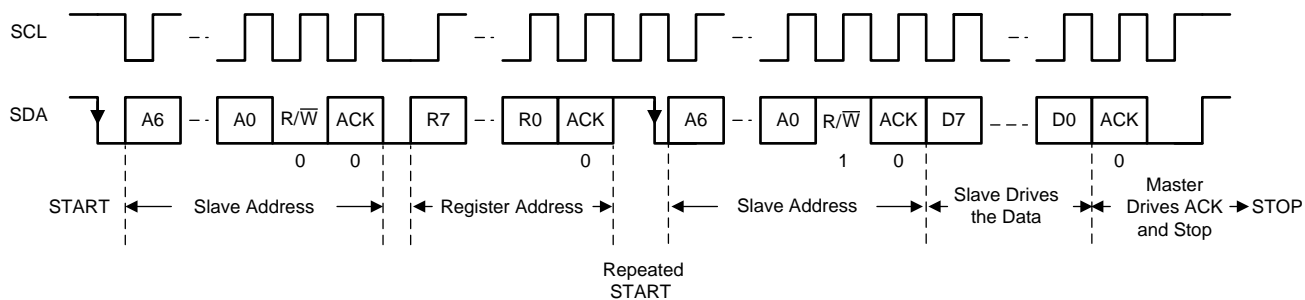


Figure 5-19. I²C Interface READ from TPS650861 in F/S Mode (Only Repeated START is Supported)

5.11 I²C Address: 0x5E Register Maps

5.11.1 Register Map Summary

This section describes the registers that can be accessed using I²C address 0x5E. These registers can be accessed without putting the device into programming mode. The DEVICEID1 and DEVICEID2 registers can only be written to while the device is in programming mode. The I²C address can be changed if necessary from the default 0x5E using the I2C_SLAVE_ADDR register (see [Section 5.12.39](#)). See the [TPS65086100 OTP Memory Programming Guide](#) for more information on putting the device into programming mode. Do not attempt to write a RESERVED R/W bit to the opposite value. When the reset value of a bit register is 0bX, it means the bit value is coming from the OTP memory.

Table 5-6. Register Map Summary

| Address | Name | Short Description |
|---------|----------------------|---|
| 00h | DEVICEID1 | Device ID code indicating revision |
| 01h | DEVICEID2 | Device ID code indicating revision |
| 02h | IRQ | Interrupt statuses |
| 03h | IRQ_MASK | Interrupt masking |
| 04h | PMIC_STAT | PMIC temperature indicator |
| 05h | SHUTDNSRC | Shutdown root cause indicator bits |
| 20h | BUCK1CTRL | BUCK1 decay control and voltage select |
| 21h | BUCK2CTRL | BUCK2 decay control and voltage select |
| 22h | BUCK3DECAY | BUCK3 decay control |
| 23h | BUCK3VID | BUCK3 voltage select |
| 24h | BUCK3SLPCTRL | BUCK3 voltage select for sleep state |
| 25h | BUCK4CTRL | BUCK4 control |
| 26h | BUCK5CTRL | BUCK5 control |
| 27h | BUCK6CTRL | BUCK6 control |
| 28h | LDOA2CTRL | LDOA2 control |
| 29h | LDOA3CTRL | LDOA3 control |
| 40h | DISCHCTRL1 | Discharge resistors for each rail control |
| 41h | DISCHCTRL2 | Discharge resistors for each rail control |
| 42h | DISCHCTRL3 | Discharge resistors for each rail control |
| 43h | PG_DELAY1 | System Power Good on GPO3 (if GPO3 is programmed to be system PG) |
| 91h | FORCESHUTDN | Software force shutdown |
| 92h | BUCK1SLPCTRL | BUCK1 voltage select for sleep state |
| 93h | BUCK2SLPCTRL | BUCK2 voltage select for sleep state |
| 94h | BUCK4VID | BUCK4 voltage select |
| 95h | BUCK4SLPVID | BUCK4 voltage select for sleep state |
| 96h | BUCK5VID | BUCK5 voltage select |
| 97h | BUCK5SLPVID | BUCK5 voltage select for sleep state |
| 98h | BUCK6VID | BUCK6 voltage select |
| 99h | BUCK6SLPVID | BUCK6 voltage select for sleep state |
| 9Ah | LDOA2VID | LDOA2 voltage select |
| 9Bh | LDOA3VID | LDOA3 voltage select |
| 9Ch | BUCK123CTRL | BUCK1, 2, and 3 disable and BUCK1, and 2 PFM/PWM mode control |
| 9Dh | PG_DELAY2 | System Power Good on GPO1, 2, and 4 (if GPOs are programmed to be system PG) |
| 9Fh | SWVTT_DIS | SWs and VTT I ² C disable bits |
| A0h | I2C_RAIL_EN1 | I ² C Enable control of individual rails |
| A1h | I2C_RAIL_EN2/GPOCTRL | I ² C Enable control of individual rails and I ² C controlled GPOs, high or low |
| A2h | PWR_FAULT_MASK1 | Power fault masking for individual rails |

Table 5-6. Register Map Summary (continued)

| Address | Name | Short Description |
|---------|-------------------|---|
| A3h | PWR_FAULT_MASK2 | Power fault masking for individual rails |
| A4h | GPO1PG_CTRL1 | Power good tree control for GPO1 |
| A5h | GPO1PG_CTRL2 | Power good tree control for GPO1 |
| A6h | GPO4PG_CTRL1 | Power good tree control for GPO4 |
| A7h | GPO4PG_CTRL2 | Power good tree control for GPO4 |
| A8h | GPO2PG_CTRL1 | Power good tree control for GPO2 |
| A9h | GPO2PG_CTRL2 | Power good tree control for GPO2 |
| AAh | GPO3PG_CTRL1 | Power good tree control for GPO3 |
| ABh | GPO3PG_CTRL2 | Power good tree control for GPO3 |
| ACH | MISCSYSPG | Power good tree control with CTL3 and CTL6 for GPO |
| ADh | VTT_DISCH_CTRL | Discharge resistor setting for VTT LDO |
| A Eh | LDOA1_SWB2_CTRL | LDOA1 and SWB2 control for discharge, voltage selection, and enable |
| B0h | PG_STATUS1 | Power good statuses for individual rails |
| B1h | PG_STATUS2 | Power good statuses for individual rails |
| B2h | PWR_FAULT_STATUS1 | Power fault statuses for individual rails |
| B3h | PWR_FAULT_STATUS2 | Power fault statuses for individual rails |
| B4h | TEMPCRIT | Critical temperature indicators |
| B5h | TEMPHOT | Hot temperature indicators |

Complex bit access types are encoded to fit into small table cells. [Table 5-7](#) shows the codes that are used for access types in this section.

Table 5-7. Access Type Codes

| Access Type | Code | Description |
|-------------|------|-------------|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |

5.11.2 DEVICEID1: 1st PMIC Device and Revision ID Register (offset = 00h) [reset = X]

Figure 5-20. DEVICEID1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit Name | PART_NUMBER[7] | PART_NUMBER[6] | PART_NUMBER[5] | PART_NUMBER[4] | PART_NUMBER[3] | PART_NUMBER[2] | PART_NUMBER[1] | PART_NUMBER[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

Table 5-8. DEVICEID1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7:4 | PART_NUMBER[7:4] | R | X | Device part number ID 0000 : TPS65086x0x 0001 : TPS65086x1x ... 1111 : TPS65086xFx |
| 3:0 | PART_NUMBER[3:0] | R | X | Device part number ID 0000 : TPS65086xx0 0001 : TPS65086xx1 ... 1111 : TPS65086xxF |

5.11.3 DEVICEID2: 2nd PMIC Device and Revision ID Register (offset = 01h) [reset = X]

Figure 5-21. DEVICEID2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------------|----------------|-----------------|-----------------|----------------|----------------|
| Bit Name | REVID[1] | REVID[0] | OTP_VERSION[1] | OTP_VERSION[0] | PART_NUMBER[11] | PART_NUMBER[10] | PART_NUMBER[9] | PART_NUMBER[8] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Access | R | R | R | R | R | R | R | R |

Table 5-9. DEVICEID2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7:6 | REVID[1:0] | R | X | Silicon revision ID |
| 5:4 | OTP_VERSION[1:0] | R | X | OTP variation ID 00 : A 01 : B 10 : C 11 : D |
| 3:0 | PART_NUMBER[11:8] | R | X | Device part number ID 0001 : TPS650861xx |

5.11.4 IRQ: PMIC Interrupt Register (offset = 02h) [reset = 0000 0000]

Figure 5-22. IRQ Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-------|----------|----------|----------|--------|----------|----------|---------|
| Bit Name | FAULT | RESERVED | RESERVED | RESERVED | SHUTDN | RESERVED | RESERVED | DIETEMP |
| TPS650861 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R | R | R | R/W | R | R | R/W |

Table 5-10. IRQ Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 7 | FAULT | R/W | 0 | Fault interrupt. Asserted when either condition occurs: power fault of any rail, or die temperature crosses over the critical temperature threshold (T_{CRIT}). The user can read Reg. 0xB2–0xB6 to determine what has caused the interrupt. 0: Not asserted 1: Asserted. Host to write 1b to clear. |
| 3 | SHUTDN | R/W | 0 | Asserted when PMIC shuts down. To clear indicator, SHUTDNSRC must be cleared first, see Section 5.11.7 0: Not asserted. 1: Asserted. Host to write 1b to clear. |
| 0 | DIETEMP | R/W | 0 | Die temp interrupt. Asserted when PMIC die temperature crosses above the hot temperature threshold (T_{HOT}). 0: Not asserted. 1: Asserted. Host to write 1b to clear. |

5.11.5 IRQ_MASK: PMIC Interrupt Mask Register (offset = 03h) [reset = 1111 1111]

Figure 5-23. IRQ_MASK Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|--------|----------|----------|----------|---------|----------|----------|----------|
| Bit Name | MFAULT | RESERVED | RESERVED | RESERVED | msHUTDN | RESERVED | RESERVED | MDIETEMP |
| TPS650861 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Access | R/W | R | R | R | R/W | R | R | R/W |

Table 5-11. IRQ_MASK Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | MFAULT | R/W | 1 | FAULT interrupt mask. 0: Not masked. 1: Masked. |
| 3 | msHUTDN | R/W | 1 | PMIC shutdown event interrupt mask 0: Not masked. 1: Masked. |
| 0 | MDIETEMP | R/W | 1 | Die temp interrupt mask. 0: Not masked. 1: Masked. |

5.11.6 PMICSTAT: PMIC Status Register (offset = 04h) [reset = 0000 0000]

Figure 5-24. PMICSTAT Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | SDIETEMP |
| TPS650861 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

Table 5-12. PMICSTAT Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 0 | SDIETEMP | R | 0 | PMIC die temperature status. 0: PMIC die temperature is below T_{HOT} . 1: PMIC die temperature is above T_{HOT} . |

5.11.7 SHUTDNSRC: PMIC Shut-Down Event Register (offset = 05h) [reset = 0000 0000]

Figure 5-25. SHUTDNSRC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----------|----------|----------|----------|---------|------|-----------|----------|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | COLDOFF | UVLO | PWR_FAULT | CRITTEMP |
| TPS650861 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W |

Table 5-13. SHUTDNSRC Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 3 | COLDOFF | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear. 0: Cleared 1: N/A. Not enabled for existing OTPs. |
| 2 | UVLO | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear. 0: Cleared 1: PMIC was shut down due to a UVLO event (V_{SYS} crosses below 5.4 V). Assertion of this bit sets the SHUTDN bit in Section 5.11.4 . |
| 1 | PWR_FAULT | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear. 0: Cleared 1: PMIC was shut down due to an unmasked power fault event. Assertion of this bit sets the SHUTDN bit in Section 5.11.4 . The source of the power fault can be determined from the PWR_FAULT registers (0xB2 and 0xB3). Overcurrent protection will limit I_{OUT} and typically cause a power fault as V_{OUT} droops. |
| 0 | CRITTEMP | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear. 0: Cleared 1: PMIC was shut down due to the rise of PMIC die temperature above critical temperature threshold (T_{CRIT}). Assertion of this bit sets the SHUTDN bit in Section 5.11.4 . |

5.11.8 BUCK1CTRL: BUCK1 Control Register (offset = 20h) [reset = X]

Figure 5-26. BUCK1CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|
| Bit Name | BUCK1_ VID[6] | BUCK1_ VID[5] | BUCK1_ VID[4] | BUCK1_ VID[3] | BUCK1_ VID[2] | BUCK1_ VID[1] | BUCK1_ VID[0] | BUCK1_ DECAY |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-14. BUCK1CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7:1 | BUCK1_VID[6:0] | R/W | X | This field sets the BUCK1 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK1_DECAY | R/W | X | Decay Bit 0: The output slews down to a lower voltage set by the VID bits. 1: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

5.11.9 BUCK2CTRL: BUCK2 Control Register (offset = 21h) [reset = X]

Figure 5-27. BUCK2CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|
| Bit Name | BUCK2_ VID[6] | BUCK2_ VID[5] | BUCK2_ VID[4] | BUCK2_ VID[3] | BUCK2_ VID[2] | BUCK2_ VID[1] | BUCK2_ VID[0] | BUCK2_ DECAY |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-15. BUCK2CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7:1 | BUCK2_VID[6:0] | R/W | X | This field sets the BUCK2 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK2_DECAY | R/W | X | Decay Bit 0: The output slews down to a lower voltage set by the VID bits. 1: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

5.11.10 BUCK3DECAY: BUCK3 Decay Control Register (offset = 22h) [reset = X]

Figure 5-28. BUCK3DECAY Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------------|
| Bit Name | SPARE | SPARE | SPARE | SPARE | SPARE | SPARE | SPARE | BUCK3_DECAY |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-16. BUCK3DECAY Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7:1 | SPARE | R/W | X | Unused. Typically mirror BUCK3_VID by default in OTP. |
| 0 | BUCK3_DECAY | R/W | X | Decay Bit 0: The output slews down to a lower voltage set by the VID bits. 1: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

5.11.11 BUCK3VID: BUCK3 VID Register (offset = 23h) [reset = X]

Figure 5-29. BUCK3VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|----------|
| Bit Name | BUCK3_VID[6] | BUCK3_VID[5] | BUCK3_VID[4] | BUCK3_VID[3] | BUCK3_VID[2] | BUCK3_VID[1] | BUCK3_VID[0] | RESERVED |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

Table 5-17. BUCK3VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7:1 | BUCK3_VID[6:0] | R/W | X | This field sets the BUCK3 regulator output regulation voltage in normal mode. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |

5.11.12 BUCK3SLPCTRL: BUCK3 Sleep Control VID Register (offset = 24h) [reset = X]

Figure 5-30. BUCK3SLPCTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--------------|
| Bit Name | BUCK3_SLP_VID[6] | BUCK3_SLP_VID[5] | BUCK3_SLP_VID[4] | BUCK3_SLP_VID[3] | BUCK3_SLP_VID[2] | BUCK3_SLP_VID[1] | BUCK3_SLP_VID[0] | BUCK3_SLP_EN |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-18. BUCK3SLPCTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7:1 | BUCK3_SLP_VID[6:0] | R/W | X | This field sets the BUCK3 regulator output regulation voltage in sleep mode if BUCK3_SLP_EN = 1b. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK3_SLP_EN | R/W | X | BUCK3 sleep mode enable. BUCK3 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0: Disable. Uses BUCK3_VID in all cases. 1: Enabled. Uses BUCK3_SLP_VID when assigned sleep pin is low. |

5.11.13 BUCK4CTRL: BUCK4 Control Register (offset = 25h) [reset = X]

Figure 5-31. BUCK4CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|-----------------|----------|----------|------------|-----------|
| Bit Name | RESERVED | RESERVED | BUCK4_SLP_EN[1] | BUCK4_SLP_EN[0] | RESERVED | RESERVED | BUCK4_MODE | BUCK4_DIS |
| TPS65086100 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-19. BUCK4CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 5:4 | BUCK4_SLP_EN | R/W | X | BUCK4 sleep mode enable. BUCK4 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 00: Disable. Uses BUCK4_VID in all cases. 11: Enabled. Uses BUCK4_SLP_VID when assigned sleep pin is low. 01,10: Reserved. Do not write these values. |
| 3:2 | RESERVED | R/W | 11 | Reserved bits. Always write to 11. |
| 1 | BUCK4_MODE | R/W | X | This field sets the BUCK4 regulator operating mode. 0: Reserved 1: Forced PWM mode |
| 0 | BUCK4_DIS | R/W | X | BUCK4 Disable Bit. Writing 0 to this bit forces BUCK4 to turn off regardless of any control input pin (CTL1–CTL6) status. 0: Disable 1: Enable |

5.11.14 BUCK5CTRL: BUCK5 Control Register (offset = 26h) [reset = X]

Figure 5-32. BUCK5CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|-----------------|----------|----------|------------|-----------|
| Bit Name | RESERVED | RESERVED | BUCK5_SLP_EN[1] | BUCK5_SLP_EN[0] | RESERVED | RESERVED | BUCK5_MODE | BUCK5_DIS |
| TPS65086100 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-20. BUCK5CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 5:4 | BUCK5_SLP_EN | R/W | X | BUCK5 sleep mode enable. BUCK5 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 00 : Disable. Uses BUCK5_VID in all cases. 11 : Enabled. Uses BUCK5_SLP_VID when assigned sleep pin is low. 01,10 : Reserved. Do not write these values. |
| 3:2 | RESERVED | R/W | 11 | Reserved bits. Always write to 11. |
| 1 | BUCK5_MODE | R/W | X | This field sets the BUCK5 regulator operating mode. 0 : Reserved 1 : Forced PWM mode |
| 0 | BUCK5_DIS | R/W | X | BUCK5 Disable Bit. Writing 0 to this bit forces BUCK5 to turn off regardless of any control input pin (CTL1–CTL6) status. 0 : Disable. 1 : Enable. |

5.11.15 BUCK6CTRL: BUCK6 Control Register (offset = 27h) [reset = X]

Figure 5-33. BUCK6CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|-----------------|----------|----------|------------|-----------|
| Bit Name | RESERVED | RESERVED | BUCK6_SLP_EN[1] | BUCK6_SLP_EN[0] | RESERVED | RESERVED | BUCK6_MODE | BUCK6_DIS |
| TPS65086100 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-21. BUCK6CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 5:4 | BUCK6_SLP_EN | R/W | X | BUCK6 sleep mode enable. BUCK6 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 00 : Disable. Uses BUCK6_VID in all cases. 11 : Enabled. Uses BUCK6_SLP_VID when assigned sleep pin is low. 01,10 : Reserved. Do not write these values. |
| 3:2 | RESERVED | R/W | 11 | Reserved bits. Always write to 11. |
| 1 | BUCK6_MODE | R/W | X | This field sets the BUCK6 regulator operating mode. 0 : Automatic mode 1 : Forced PWM mode |
| 0 | BUCK6_DIS | R/W | X | BUCK6 Disable Bit. Writing 0 to this bit forces BUCK6 to turn off regardless of any control input pin (CTL1–CTL6) status. 0 : Disable. 1 : Enable. |

5.11.16 LDOA2CTRL: LDOA2 Control Register (offset = 28h) [reset = X]

Figure 5-34. LDOA2CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|-----------------|----------|----------|----------|-----------|
| Bit Name | RESERVED | RESERVED | LDOA2_SLP_EN[1] | LDOA2_SLP_EN[0] | RESERVED | RESERVED | RESERVED | LDOA2_DIS |
| TPS65086100 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-22. LDOA2CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 5:4 | LDOA2_SLP_EN | R/W | X | LDOA2 sleep mode enable. LDOA2 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 00 : Disable. Uses LDOA2_VID in all cases. 11 : Enabled. Uses LDOA2_SLP_VID when assigned sleep pin is low. 01,10 : Reserved. Do not write these values. |
| 3:1 | RESERVED | R/W | 110 | Reserved bits. Always write to '110'. |
| 0 | LDOA2_DIS | R/W | X | LDOA2 Disable Bit. Writing 0 to this bit forces LDOA2 to turn off regardless of any control input pin (CTL1–CTL6) status. 0 : Disable. 1 : Enable. |

5.11.17 LDOA3CTRL: LDOA3 Control Register (offset = 29h) [reset = X]

Figure 5-35. LDOA3CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|-----------------|----------|----------|----------|-----------|
| Bit Name | RESERVED | RESERVED | LDOA3_SLP_EN[1] | LDOA3_SLP_EN[0] | RESERVED | RESERVED | RESERVED | LDOA3_DIS |
| TPS65086100 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-23. LDOA3CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 5:4 | LDOA3_SLP_EN | R/W | X | LDOA3 sleep mode enable. LDOA3 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 00 : Disable. Uses LDOA3_VID in all cases. 11 : Enabled. Uses LDOA3_SLP_VID when assigned sleep pin is low. 01,10 : Reserved. Do not write these values. |
| 3:1 | RESERVED | R/W | 110 | Reserved bits. Always write to '110'. |
| 0 | LDOA3_DIS | R/W | X | LDOA3 Disable Bit. Writing 0 to this bit forces LDOA3 to turn off regardless of any control input pin (CTL1–CTL6) status. 0 : Disable 1 : Enable |

5.11.18 DISCHCTRL1: 1st Discharge Control Register (offset = 40h) [reset = X]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

Figure 5-36. DISCHCTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| Bit Name | BUCK4_ DISCHG[1] | BUCK4_ DISCHG[0] | BUCK3_ DISCHG[1] | BUCK3_ DISCHG[0] | BUCK2_ DISCHG[1] | BUCK2_ DISCHG[0] | BUCK1_ DISCHG[1] | BUCK1_ DISCHG[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-24. DISCHCTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7:6 | BUCK4_DISCHG[1:0] | R/W | X | BUCK4 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 5:4 | BUCK3_DISCHG[1:0] | R/W | X | BUCK3 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 3:2 | BUCK2_DISCHG[1:0] | R/W | X | BUCK2 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 1:0 | BUCK1_DISCHG[1:0] | R/W | X | BUCK1 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |

5.11.19 DISCHCTRL2: 2nd Discharge Control Register (offset = 41h) [reset = X]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

Figure 5-37. DISCHCTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---------------------|--------------------|--------------------|---------------------|---------------------|---------------------|---------------------|
| Bit Name | LDOA2_ DISCHG[1] | LDOA2_ DISCHG[0] | SWA1_ DISCHG[1] | SWA1_ DISCHG[0] | BUCK6_ DISCHG[1] | BUCK6_ DISCHG[0] | BUCK5_ DISCHG[1] | BUCK5_ DISCHG[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-25. DISCHCTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7:6 | LDOA2_DISCHG[1:0] | R/W | X | LDOA2 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 5:4 | SWA1_DISCHG[1:0] | R/W | X | SWA1 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 3:2 | BUCK6_DISCHG[1:0] | R/W | X | BUCK6 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 1:0 | BUCK5_DISCHG[1:0] | R/W | X | BUCK5 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |

5.11.20 DISCHCTRL3: 3rd Discharge Control Register (offset = 42h) [reset = X]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

Figure 5-38. DISCHCTRL3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------------|----------------|----------------|----------------|-----------------|-----------------|
| Bit Name | RESERVED | RESERVED | SWB2_DISCHG[1] | SWB2_DISCHG[0] | SWB1_DISCHG[1] | SWB1_DISCHG[0] | LDOA3_DISCHG[1] | LDOA3_DISCHG[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-26. DISCHCTRL3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 5:4 | SWB2_DISCHG[1:0] | R/W | X | SWB2 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 3:2 | SWB1_DISCHG[1:0] | R/W | X | SWB1 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |
| 1:0 | LDOA3_DISCHG[1:0] | R/W | X | LDOA3 discharge resistance 00 : no discharge 01 : 100 Ω 10 : 200 Ω 11 : 500 Ω |

5.11.21 PG_DELAY1: 1st Power Good Delay Register (offset = 43h) [reset = X]

Programmable Power Good delay for GPO3 pin, measured from the moment when all VRs assigned to GPO3 pin reach their regulation range to Power Good assertion. This is an optional register as the PMIC can be programmed for system PG, level shifter or I²C controller GPO.

Figure 5-39. PG_DELAY1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|----------|------------------|------------------|------------------|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | GPO3_PG_DELAY[2] | GPO3_PG_DELAY[1] | GPO3_PG_DELAY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R/W | R/W | R/W |

Table 5-27. PG_DELAY1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 2:0 | GPO3_PG_DELAY[2:0] | R/W | X | Programmable delay Power Good or level shifter for GPO3 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation. 000 : 2.5 ms 001 : 5.0 ms 010 : 10 ms 011 : 15 ms 100 : 20 ms 101 : 50 ms 110 : 75 ms 111 : 100 ms —: Bits not used. If GPO3 is controlled by I ² C rather than PG and is not used internally for VTT LDO enable, these bits have no impact. Default is set to 0b. |

5.11.22 FORCESHUTDN: Force Emergency Shutdown Control Register (offset = 91h) [reset = 0000 0000]

Figure 5-40. FORCESHUTDN Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----------|----------|----------|----------|----------|----------|----------|------|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | SDWN |
| TPS650861 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R/W |

Table 5-28. FORCESHUTDN Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | SDWN | R/W | 0 | Forces reset of the PMIC and reset of all registers. The bit is self-clearing. PMIC does not generate I ² C ACK for this command because it goes into emergency shutdown. 0: No action. 1: PMIC initiates emergency shutdown. |

5.11.23 BUCK1SLPCTRL: BUCK1 Sleep Control Register (offset = 92h) [reset = X]

Figure 5-41. BUCK1SLPCTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--------------|
| Bit Name | BUCK1_SLP_VID[6] | BUCK1_SLP_VID[5] | BUCK1_SLP_VID[4] | BUCK1_SLP_VID[3] | BUCK1_SLP_VID[2] | BUCK1_SLP_VID[1] | BUCK1_SLP_VID[0] | BUCK1_SLP_EN |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-29. BUCK1SLPCTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7:1 | BUCK1_SLP_VID[6:0] | R/W | X | This field sets the BUCK1 regulator output regulation voltage in normal mode. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK1_SLP_EN | R/W | X | BUCK1 sleep mode enable. BUCK1 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0: Disable. Uses BUCK1_VID in all cases. 1: Enabled. Uses BUCK1_SLP_VID when assigned sleep pin is low. |

5.11.24 BUCK2SLPCTRL: BUCK2 Sleep Control Register (offset = 93h) [reset = X]

Figure 5-42. BUCK2SLPCTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--------------|
| Bit Name | BUCK2_SLP_VID[6] | BUCK2_SLP_VID[5] | BUCK2_SLP_VID[4] | BUCK2_SLP_VID[3] | BUCK2_SLP_VID[2] | BUCK2_SLP_VID[1] | BUCK2_SLP_VID[0] | BUCK2_SLP_EN |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-30. BUCK2SLPCTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7:1 | BUCK2_SLP_VID[6:0] | R/W | X | This field sets the BUCK2 regulator output regulation voltage in normal mode. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK2_SLP_EN | R/W | X | BUCK2 sleep mode enable. BUCK2 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0: Disable. Uses BUCK2_VID in all cases. 1: Enabled. Uses BUCK2_SLP_VID when assigned sleep pin is low. |

5.11.25 BUCK4VID: BUCK4 VID Register (offset = 94h) [reset = X]

Figure 5-43. BUCK4VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|
| Bit Name | BUCK4_VID[6] | BUCK4_VID[5] | BUCK4_VID[4] | BUCK4_VID[3] | BUCK4_VID[2] | BUCK4_VID[1] | BUCK4_VID[0] | BUCK4_DECAY |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-31. BUCK4VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7:1 | BUCK4_VID[6:0] | R/W | X | This field sets the BUCK4 regulator output regulation voltage in normal mode. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK4_DECAY | R/W | X | Decay Bit 0: The output slews down to a lower voltage set by the VID bits. 1: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

5.11.26 BUCK4SLPVID: BUCK4 Sleep VID Register (offset = 95h) [reset = X]

Figure 5-44. BUCK4SLPVID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------|
| Bit Name | BUCK4_SLP_VID[6] | BUCK4_SLP_VID[5] | BUCK4_SLP_VID[4] | BUCK4_SLP_VID[3] | BUCK4_SLP_VID[2] | BUCK4_SLP_VID[1] | BUCK4_SLP_VID[0] | RESERVED |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

Table 5-32. BUCK4SLPVID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7:1 | BUCK4_SLP_VID[6:0] | R/W | X | This field sets the BUCK4 regulator output regulation voltage in sleep mode. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |

5.11.27 BUCK5VID: BUCK5 VID Register (offset = 96h) [reset = X]

Figure 5-45. BUCK5VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|
| Bit Name | BUCK5_VID[6] | BUCK5_VID[5] | BUCK5_VID[4] | BUCK5_VID[3] | BUCK5_VID[2] | BUCK5_VID[1] | BUCK5_VID[0] | BUCK5_DECAY |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-33. BUCK5VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7:1 | BUCK5_VID[6:0] | R/W | X | This field sets the BUCK5 regulator output regulation voltage in normal mode. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK5_DECAY | R/W | X | Decay Bit 0: The output slews down to a lower voltage set by the VID bits. 1: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

5.11.28 BUCK5SLPVID: BUCK5 Sleep VID Register (offset = 97h) [reset = X]

Figure 5-46. BUCK5SLPVID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------|
| Bit Name | BUCK5_SLP_VID[6] | BUCK5_SLP_VID[5] | BUCK5_SLP_VID[4] | BUCK5_SLP_VID[3] | BUCK5_SLP_VID[2] | BUCK5_SLP_VID[1] | BUCK5_SLP_VID[0] | RESERVED |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

Table 5-34. BUCK5SLPVID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7:1 | BUCK5_SLP_VID[6:0] | R/W | X | This field sets the BUCK5 regulator output regulation voltage in sleep mode. See Table 5-3 for 25-mV step ranges for V _{OUT} options. |

5.11.29 BUCK6VID: BUCK6 VID Register (offset = 98h) [reset = X]

Figure 5-47. BUCK6VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|
| Bit Name | BUCK6_VID[6] | BUCK6_VID[5] | BUCK6_VID[4] | BUCK6_VID[3] | BUCK6_VID[2] | BUCK6_VID[1] | BUCK6_VID[0] | BUCK6_DECAY |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-35. BUCK6VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7:1 | BUCK6_VID[6:0] | R/W | X | This field sets the BUCK6 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V _{OUT} options. |
| 0 | BUCK6_DECAY | R/W | X | Decay Bit 0: The output slews down to a lower voltage set by the VID bits. 1: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

5.11.30 BUCK6SLPVID: BUCK6 Sleep VID Register (offset = 99h) [reset = X]

Figure 5-48. BUCK6SLPVID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------|
| Bit Name | BUCK6_SLP_VID[6] | BUCK6_SLP_VID[5] | BUCK6_SLP_VID[4] | BUCK6_SLP_VID[3] | BUCK6_SLP_VID[2] | BUCK6_SLP_VID[1] | BUCK6_SLP_VID[0] | RESERVED |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

Table 5-36. BUCK6SLPVID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7:1 | BUCK6_SLP_VID[6:0] | R/W | X | This field sets the BUCK6 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V _{OUT} options. |

5.11.31 LDOA2VID: LDOA2 VID Register (offset = 9Ah) [reset = X]

Figure 5-49. LDOA2VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|--------------|--------------|--------------|--------------|
| Bit Name | LDOA2_SLP_VID[3] | LDOA2_SLP_VID[2] | LDOA2_SLP_VID[1] | LDOA2_SLP_VID[0] | LDOA2_VID[3] | LDOA2_VID[2] | LDOA2_VID[1] | LDOA2_VID[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-37. LDOA2VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7:4 | LDOA2_SLP_VID[3:0] | R/W | X | This field sets the LDOA2 regulator output regulation voltage in sleep mode. See Table 5-5 for V _{out} options. |
| 3:0 | LDOA2_VID[3:0] | R/W | X | This field sets the LDOA2 regulator output regulation voltage in normal mode. See Table 5-5 for V _{out} options. |

5.11.32 LDOA3VID: LDOA3 VID Register (offset = 9Bh) [reset = X]

Figure 5-50. LDOA3VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|--------------|--------------|--------------|--------------|
| Bit Name | LDOA3_SLP_VID[3] | LDOA3_SLP_VID[2] | LDOA3_SLP_VID[1] | LDOA3_SLP_VID[0] | LDOA3_VID[3] | LDOA3_VID[2] | LDOA3_VID[1] | LDOA3_VID[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-38. LDOA3VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7:4 | LDOA3_SLP_VID[3:0] | R/W | X | This field sets the LDOA3 regulator output regulation voltage in sleep mode. See Table 5-5 for V_{out} options. |
| 3:0 | LDOA3_VID[3:0] | R/W | X | This field sets the LDOA3 regulator output regulation voltage in normal mode. See Table 5-5 for V_{out} options. |

5.11.33 BUCK123CTRL: BUCK1-3 Control Register (offset = 9Ch) [reset = X]

Figure 5-51. BUCK123CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|------------|------------|------------|-----------|-----------|-----------|
| Bit Name | RESERVED | RESERVED | BUCK3_MODE | BUCK2_MODE | BUCK1_MODE | BUCK3_DIS | BUCK2_DIS | BUCK1_DIS |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-39. BUCK123CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|--|
| 5 | BUCK3_MODE | R/W | X | This field sets the BUCK3 regulator operating mode. 0: Reserved 1: Forced PWM mode |
| 4 | BUCK2_MODE | R/W | X | This field sets the BUCK2 regulator operating mode. 0: Automatic mode 1: Forced PWM mode |
| 3 | BUCK1_MODE | R/W | X | This field sets the BUCK1 regulator operating mode. 0: Automatic mode 1: Forced PWM mode |
| 2 | BUCK3_DIS | R/W | X | BUCK3 Disable Bit. Writing 0 to this bit forces BUCK3 to turn off regardless of any control input pin (CTL1–CTL6) status. 0: Disable 1: Enable |
| 1 | BUCK2_DIS | R/W | X | BUCK2 Disable Bit. Writing 0 to this bit forces BUCK2 to turn off regardless of any control input pin (CTL1–CTL6) status. 0: Disable 1: Enable |
| 0 | BUCK1_DIS | R/W | X | BUCK1 Disable Bit. Writing 0 to this bit forces BUCK1 to turn off regardless of any control input pin (CTL1–CTL6) status. 0: Disable 1: Enable |

5.11.34 PG_DELAY2: 2nd Power Good Delay Register (offset = 9Dh) [reset = X]

Programmable Power Good delay for GPO1, GPO2, and GPO4 pins, measured from the moment when all VRs assigned to respective GPO reach their regulation range to Power Good assertion. This is an optional register as the PMIC can be programmed for system PG, level shifter or I²C controller GPO.

Figure 5-52. PG_DELAY2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit Name | GPO2_PG_DELAY[2] | GPO2_PG_DELAY[1] | GPO2_PG_DELAY[0] | GPO4_PG_DELAY[2] | GPO4_PG_DELAY[1] | GPO4_PG_DELAY[0] | GPO1_PG_DELAY[1] | GPO1_PG_DELAY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-40. PG_DELAY2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7:5 | GPO2_PG_DELAY[2:0] | R/W | X | Programmable delay Power Good or level shifter for GPO2 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation. 000 : 0 ms 001 : 5.0 ms 010 : 10 ms 011 : 15 ms 100 : 20 ms 101 : 50 ms 110 : 75 ms 111 : 100 ms —: Bits not used. If GPO2 is controlled by I ² C rather than PG and is not used internally for VTT LDO enable, these bits have no impact. Default is set to 0b. |
| 4:2 | GPO4_PG_DELAY[2:0] | R/W | X | Programmable delay Power Good or level shifter for GPO4 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation. 000 : 0 ms 001 : 5.0 ms 010 : 10 ms 011 : 15 ms 100 : 20 ms 101 : 50 ms 110 : 75 ms 111 : 100 ms —: Bits not used. If GPO4 is controlled by I ² C rather than PG, these bits have no impact. Default is set to 0b. |
| 1:0 | GPO1_PG_DELAY[1:0] | R/W | X | Programmable delay Power Good or level shifter for GPO1 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation. 00 : 0 ms 01 : 5.0 ms 10 : 10 ms 11 : 15 ms —: Bits not used. If GPO1 is controlled by I ² C rather than PG, these bits have no impact. Default is set to 0b. |

5.11.35 SWVTT_DIS: SWVTT Disable Register (offset = 9Fh) [reset = X]

Figure 5-53. SWVTT_DIS Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|----------|----------|---------|----------|----------|----------|----------|
| Bit Name | SWB2_LDO A1_DIS | SWB1_DIS | SWA1_DIS | VTT_DIS | Reserved | Reserved | Reserved | Reserved |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-41. SWVTT_DIS Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | SWB2_LDOA1_DIS | R/W | X | SWB2 or LDOA1 Disable Bit. Writing 0 to this bit forces SWB2 or LDOA1 to turn off regardless of any control input pin (CTL1–CTL6) status. OTP setting selects either SWB2 or LDOA1. 0: Disable. 1: Enable. SWB2 for: OTP Dependent LDOA1 for: OTP Dependent |
| 6 | SWB1_DIS | R/W | X | SWB1 Disable Bit. Writing 0 to this bit forces SWB1 to turn off regardless of any control input pin (CTL1–CTL6) status. 0: Disable. 1: Enable. |
| 5 | SWA1_DIS | R/W | X | SWA1 Disable Bit. Writing 0 to this bit forces SWA1 to turn off regardless of any control input pin (CTL1–CTL6) status. 0: Disable. 1: Enable. |
| 4 | VTT_DIS | R/W | X | VTT Disable Bit. Writing 0 to this bit forces VTT to turn off regardless of any control input pin (CTL1–CTL6) status. 0: Disable. 1: Enable. |
| 3:0 | Reserved | R/W | 0000 | Reserved bits. Always write to 0000. |

5.11.36 I2C_RAIL_EN1: 1st VR Pin Enable Override Register (offset = A0h) [reset = X]
Figure 5-54. I2C_RAIL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|---------|----------|----------|----------|----------|----------|----------|
| Bit Name | LDOA2_EN | SWA1_EN | BUCK6_EN | BUCK5_EN | BUCK4_EN | BUCK3_EN | BUCK2_EN | BUCK1_EN |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-42. I2C_RAIL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | LDOA2_EN | R/W | X | LDOA2 I ² C Enable 0: LDOA2 is enabled or disabled by one of the control input pins or internal PG signal. 1: LDOA2 is forced on unless LDOA2_DIS = 0b. |
| 6 | SWA1_EN | R/W | X | SWA1 I ² C Enable 0: SWA1 is enabled or disabled by one of the control input pins or internal PG signal. 1: SWA1 is forced on unless SWA1_DIS = 0b. |
| 5 | BUCK6_EN | R/W | X | BUCK6 I ² C Enable 0: BUCK6 is enabled or disabled by one of the control input pins or internal PG signal. 1: BUCK6 is forced on unless BUCK6_DIS = 0b. |
| 4 | BUCK5_EN | R/W | X | BUCK5 I ² C Enable 0: BUCK5 is enabled or disabled by one of the control input pins or internal PG signal. 1: BUCK5 is forced on unless BUCK5_DIS = 0b. |
| 3 | BUCK4_EN | R/W | X | BUCK4 I ² C Enable 0: BUCK4 is enabled or disabled by one of the control input pins or internal PG signal. 1: BUCK4 is forced on unless BUCK4_DIS = 0b. |
| 2 | BUCK3_EN | R/W | X | BUCK3 I ² C Enable 0: BUCK3 is enabled or disabled by one of the control input pins or internal PG signal. 1: BUCK3 is forced on unless BUCK3_DIS = 0b. |
| 1 | BUCK2_EN | R/W | X | BUCK2 I ² C Enable 0: BUCK2 is enabled or disabled by one of the control input pins or internal PG signal. 1: BUCK2 is forced on unless BUCK2_DIS = 0b. |
| 0 | BUCK1_EN | R/W | X | BUCK1 I ² C Enable 0: BUCK1 is enabled or disabled by one of the control input pins or internal PG signal. 1: BUCK1 is forced on unless BUCK1_DIS = 0b. |

5.11.37 I2C_RAIL_EN2/GPOCTRL: 2nd VR Pin Enable Override and GPO Control Register (offset = A1h) [reset = X]

Figure 5-55. I2C_RAIL_EN2/GPOCTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|--------|-------------------|---------|----------|
| Bit Name | GPO4_LVL | GPO3_LVL | GPO2_LVL | GPO1_LVL | VTT_EN | SWB2_LDO A1_EN | SWB1_EN | LDOA3_EN |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-43. I2C_RAIL_EN2/GPOCTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7 | GPO4_LVL | R/W | X | The field is to set GPO4 pin output if the pin is factory-configured as an I ² C controlled open-drain general-purpose output. 0: The pin is driven to logic low. 1: The pin is driven to logic high. —: Bit not used in this version; GPO4 is controlled by GPO4 PG tree. Default is set to 0b. |
| 6 | GPO3_LVL | R/W | X | The field is to set GPO3 pin output if the pin is factory-configured as either an I ² C controlled open-drain or a push-pull general-purpose output. 0: The pin is driven to logic low. 1: The pin is driven to logic high. —: Bit not used in this version; GPO3 is controlled by GPO3 PG tree. Default is set to 0b. |
| 5 | GPO2_LVL | R/W | X | The field is to set GPO2 pin output if the pin is factory-configured as either an I ² C controlled open-drain or a push-pull general-purpose output. 0: The pin is driven to logic low. 1: The pin is driven to logic high. —: Bit not used in this version; GPO2 is controlled by GPO2 PG tree. Default is set to 0b. |
| 4 | GPO1_LVL | R/W | X | The field is to set GPO1 pin output if the pin is factory-configured as either an I ² C controlled open-drain or a push-pull general-purpose output. 0: The pin is driven to logic low. 1: The pin is driven to logic high. —: Bit not used in this version; GPO1 is controlled by GPO1 PG tree. Default is set to 0b. |
| 3 | VTT_EN | R/W | X | VTT LDO I ² C Enable 0: VTT LDO is enabled or disabled by one of the control input pins or internal PG signals. 1: VTT LDO is forced on unless VTT_DIS = 0b. |
| 2 | SWB2_LDOA1_EN | R/W | X | SWB2 or LDOA1 I ² C Enable. Internal setting selects either SWB2 or LDOA1. 0: SWB2 or LDOA1 is enabled or disabled by one of the control input pins or internal PG signals. 1: SWB2 or LDOA1 is forced on unless SWB2_LDOA1_DIS = 0b. SWB2 for: OTP Dependent LDOA1 for: OTP Dependent |
| 1 | SWB1_EN | R/W | X | SWB1 I ² C Enable 0: SWB1 is enabled or disabled by one of the control input pins or internal PG signals. 1: SWB1 is forced on unless SWB1_DIS = 0b. |
| 0 | LDOA3_EN | R/W | X | LDOA3 I ² C Enable 0: LDOA3 is enabled or disabled by one of the control input pins or internal PG signals. 1: LDOA3 is forced on unless LDOA3_DIS = 0b. |

5.11.38 PWR_FAULT_MASK1: 1st VR Power Fault Mask Register (offset = A2h) [reset = X]
Figure 5-56. PWR_FAULT_MASK1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit Name | LDOA2_FLTmsK | SWA1_FLTmsK | BUCK6_FLTmsK | BUCK5_FLTmsK | BUCK4_FLTmsK | BUCK3_FLTmsK | BUCK2_FLTmsK | BUCK1_FLTmsK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-44. PWR_FAULT_MASK1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | LDOA2_FLTmsK | R/W | X | LDOA2 Power Fault Mask. When masked, power fault from LDOA2 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 6 | SWA1_FLTmsK | R/W | X | SWA1 Power Fault Mask. When masked, power fault from SWA1 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 5 | BUCK6_FLTmsK | R/W | X | BUCK6 Power Fault Mask. When masked, power fault from BUCK6 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 4 | BUCK5_FLTmsK | R/W | X | BUCK5 Power Fault Mask. When masked, power fault from BUCK5 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 3 | BUCK4_FLTmsK | R/W | X | BUCK4 Power Fault Mask. When masked, power fault from BUCK4 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 2 | BUCK3_FLTmsK | R/W | X | BUCK3 Power Fault Mask. When masked, power fault from BUCK3 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 1 | BUCK2_FLTmsK | R/W | X | BUCK2 Power Fault Mask. When masked, power fault from BUCK2 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 0 | BUCK1_FLTmsK | R/W | X | BUCK1 Power Fault Mask. When masked, power fault from BUCK1 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |

5.11.39 PWR_FAULT_MASK2: 2nd VR Power Fault Mask Register (offset = A3h) [reset = X]

Figure 5-57. PWR_FAULT_MASK2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|--------------|------------|-------------|-------------|--------------|
| Bit Name | RESERVED | RESERVED | RESERVED | LDOA1_FLTmsK | VTT_FLTmsK | SWB2_FLTmsK | SWB1_FLTmsK | LDOA3_FLTmsK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-45. PWR_FAULT_MASK2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 6 | RESERVED | R/W | 0 | Reserved bit. Always write to 0b. |
| 5 | RESERVED | R/W | 1 | Reserved bit. Always write to 1b. |
| 4 | LDOA1_FLTmsK | R/W | X | LDOA1 Power Fault Mask. When masked, power fault from LDOA1 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 3 | VTT_FLTmsK | R/W | X | VTT LDO Power Fault Mask. When masked, power fault from VTT LDO does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 2 | SWB2_FLTmsK | R/W | X | SWB2 Power Fault Mask. When masked, power fault from SWB2 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 1 | SWB1_FLTmsK | R/W | X | SWB1 Power Fault Mask. When masked, power fault from SWB1 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |
| 0 | LDOA3_FLTmsK | R/W | X | LDOA3 Power Fault Mask. When masked, power fault from LDOA3 does not cause PMIC to shutdown. 0: Not Masked 1: Masked |

5.11.40 GPO1PG_CTRL1: 1st GPO1 PG Control Register (offset = A4h) [reset = X]
Figure 5-58. GPO1PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Name | LDOA2_msK | SWA1_msK | BUCK6_msK | BUCK5_msK | BUCK4_msK | BUCK3_msK | BUCK2_msK | BUCK1_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-46. GPO1PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | LDOA2_msK | R/W | X | 0: LDOA2 PG is part of Power Good tree of GPO1 pin. 1: LDOA2 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | 0: SWA1 PG is part of Power Good tree of GPO1 pin. 1: SWA1 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | 0: BUCK6 PG is part of Power Good tree of GPO1 pin. 1: BUCK6 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | 0: BUCK5 PG is part of Power Good tree of GPO1 pin. 1: BUCK5 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | 0: BUCK4 PG is part of Power Good tree of GPO1 pin. 1: BUCK4 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | 0: BUCK3 PG is part of Power Good tree of GPO1 pin. 1: BUCK3 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | 0: BUCK2 PG is part of Power Good tree of GPO1 pin. 1: BUCK2 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | 0: BUCK1 PG is part of Power Good tree of GPO1 pin. 1: BUCK1 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |

5.11.41 GPO1PG_CTRL2: 2nd GPO1 PG Control Register (offset = A5h) [reset = X]

Figure 5-59. GPO1PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|---------|--------------------|----------|-----------|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDO A1_msK | SWB1_msK | LDOA3_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-47. GPO1PG_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | CTL5_msK | R/W | X | 0: CTL5 pin status is part of Power Good tree of GPO1 pin. 1: CTL5 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | 0: CTL4 pin status is part of Power Good tree of GPO1 pin. 1: CTL4 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | 0: CTL2 pin status is part of Power Good tree of GPO1 pin. 1: CTL2 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | 0: CTL1 pin status is part of Power Good tree of GPO1 pin. 1: CTL1 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 3 | VTT_msK | R/W | X | 0: VTT LDO PG is part of Power Good tree of GPO1 pin. 1: VTT LDO PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | 0: SWB2_LDOA1 PG is part of Power Good tree of GPO1 pin. 1: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO1 pin and is ignored. SWB2 for: OTP Dependent LDOA1 for: OTP Dependent |
| 1 | SWB1_msK | R/W | X | 0: SWB1 PG is part of Power Good tree of GPO1 pin. 1: SWB1 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | 0: LDOA3 PG is part of Power Good tree of GPO1 pin. 1: LDOA3 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |

5.11.42 GPO4PG_CTRL1: 1st GPO4 PG Control Register (offset = A6h) [reset = X]
Figure 5-60. GPO4PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Name | LDOA2_msK | SWA1_msK | BUCK6_msK | BUCK5_msK | BUCK4_msK | BUCK3_msK | BUCK2_msK | BUCK1_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-48. GPO4PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | LDOA2_msK | R/W | X | 0: LDOA2 PG is part of Power Good tree of GPO4 pin. 1: LDOA2 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | 0: SWA1 PG is part of Power Good tree of GPO4 pin. 1: SWA1 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | 0: BUCK6 PG is part of Power Good tree of GPO4 pin. 1: BUCK6 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | 0: BUCK5 PG is part of Power Good tree of GPO4 pin. 1: BUCK5 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | 0: BUCK4 PG is part of Power Good tree of GPO4 pin. 1: BUCK4 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | 0: BUCK3 PG is part of Power Good tree of GPO4 pin. 1: BUCK3 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | 0: BUCK2 PG is part of Power Good tree of GPO4 pin. 1: BUCK2 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | 0: BUCK1 PG is part of Power Good tree of GPO4 pin. 1: BUCK1 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |

5.11.43 GPO4PG_CTRL2: 2nd GPO4 PG Control Register (offset = A7h) [reset = X]

Figure 5-61. GPO4PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|---------|--------------------|----------|-----------|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDO A1_msK | SWB1_msK | LDOA3_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-49. GPO4PG_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | CTL5_msK | R/W | X | 0: CTL5 pin status is part of Power Good tree of GPO4 pin. 1: CTL5 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | 0: CTL4 pin status is part of Power Good tree of GPO4 pin. 1: CTL4 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | 0: CTL2 pin status is part of Power Good tree of GPO4 pin. 1: CTL2 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | 0: CTL1 pin status is part of Power Good tree of GPO4 pin. 1: CTL1 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 3 | VTT_msK | R/W | X | 0: VTT LDO PG is part of Power Good tree of GPO4 pin. 1: VTT LDO PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | 0: SWB2_LDOA1 PG is part of Power Good tree of GPO4 pin. 1: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO4 pin and is ignored. SWB2 for: OTP Dependent LDOA1 for: OTP Dependent |
| 1 | SWB1_msK | R/W | X | 0: SWB1 PG is part of Power Good tree of GPO4 pin. 1: SWB1 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | 0: LDOA3 PG is part of Power Good tree of GPO4 pin. 1: LDOA3 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |

5.11.44 GPO2PG_CTRL1: 1st GPO2 PG Control Register (offset = A8h) [reset = X]
Figure 5-62. GPO2PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Name | LDOA2_msK | SWA1_msK | BUCK6_msK | BUCK5_msK | BUCK4_msK | BUCK3_msK | BUCK2_msK | BUCK1_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-50. GPO2PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | LDOA2_msK | R/W | X | 0: LDOA2 PG is part of Power Good tree of GPO2 pin. 1: LDOA2 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | 0: SWA1 PG is part of Power Good tree of GPO2 pin. 1: SWA1 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | 0: BUCK6 PG is part of Power Good tree of GPO2 pin. 1: BUCK6 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | 0: BUCK5 PG is part of Power Good tree of GPO2 pin. 1: BUCK5 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | 0: BUCK4 PG is part of Power Good tree of GPO2 pin. 1: BUCK4 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | 0: BUCK3 PG is part of Power Good tree of GPO2 pin. 1: BUCK3 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | 0: BUCK2 PG is part of Power Good tree of GPO2 pin. 1: BUCK2 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | 0: BUCK1 PG is part of Power Good tree of GPO2 pin. 1: BUCK1 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |

5.11.45 GPO2PG_CTRL2: 2nd GPO2 PG Control Register (offset = A9h) [reset = X]

Figure 5-63. GPO2PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|---------|--------------------|----------|---------------|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDO A1_msK | SWB1_msK | LDOA3_ msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-51. GPO2PG_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | CTL5_msK | R/W | X | 0: CTL5 pin status is part of Power Good tree of GPO2 pin. 1: CTL5 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | 0: CTL4 pin status is part of Power Good tree of GPO2 pin. 1: CTL4 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | 0: CTL2 pin status is part of Power Good tree of GPO2 pin. 1: CTL2 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | 0: CTL1 pin status is part of Power Good tree of GPO2 pin. 1: CTL1 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 3 | VTT_msK | R/W | X | 0: VTT LDO PG is part of Power Good tree of GPO2 pin. 1: VTT LDO PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | 0: SWB2_LDOA1 PG is part of Power Good tree of GPO2 pin. 1: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO2 pin and is ignored. SWB2 for: OTP Dependent LDOA1 for: OTP Dependent |
| 1 | SWB1_msK | R/W | X | 0: SWB1 PG is part of Power Good tree of GPO2 pin. 1: SWB1 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | 0: LDOA3 PG is part of Power Good tree of GPO2 pin. 1: LDOA3 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |

5.11.46 GPO3PG_CTRL1: 1st GPO3 PG Control Register (offset = AAh) [reset = X]
Figure 5-64. GPO3PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Name | LDOA2_msK | SWA1_msK | BUCK6_msK | BUCK5_msK | BUCK4_msK | BUCK3_msK | BUCK2_msK | BUCK1_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-52. GPO3PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | LDOA2_msK | R/W | X | 0: LDOA2 PG is part of Power Good tree of GPO3 pin. 1: LDOA2 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | 0: SWA1 PG is part of Power Good tree of GPO3 pin. 1: SWA1 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | 0: BUCK6 PG is part of Power Good tree of GPO3 pin. 1: BUCK6 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | 0: BUCK5 PG is part of Power Good tree of GPO3 pin. 1: BUCK5 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | 0: BUCK4 PG is part of Power Good tree of GPO3 pin. 1: BUCK4 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | 0: BUCK3 PG is part of Power Good tree of GPO3 pin. 1: BUCK3 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | 0: BUCK2 PG is part of Power Good tree of GPO3 pin. 1: BUCK2 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | 0: BUCK1 PG is part of Power Good tree of GPO3 pin. 1: BUCK1 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |

5.11.47 GPO3PG_CTRL2: 2nd GPO3 PG Control Register (offset = ABh) [reset = X]

Figure 5-65. GPO3PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|---------|--------------------|----------|-----------|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDO A1_msK | SWB1_msK | LDOA3_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-53. GPO3PG_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | CTL5_msK | R/W | X | 0: CTL5 pin status is part of Power Good tree of GPO3 pin. 1: CTL5 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | 0: CTL4 pin status is part of Power Good tree of GPO3 pin. 1: CTL4 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | 0: CTL2 pin status is part of Power Good tree of GPO3 pin. 1: CTL2 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | 0: CTL1 pin status is part of Power Good tree of GPO3 pin. 1: CTL1 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 3 | VTT_msK | R/W | X | 0: VTT LDO PG is part of Power Good tree of GPO3 pin. 1: VTT LDO PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | 0: SWB2_LDOA1 PG is part of Power Good tree of GPO3 pin. 1: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO3 pin and is ignored. SWB2 for: OTP Dependent LDOA1 for: OTP Dependent |
| 1 | SWB1_msK | R/W | X | 0: SWB1 PG is part of Power Good tree of GPO3 pin. 1: SWB1 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | 0: LDOA3 PG is part of Power Good tree of GPO3 pin. 1: LDOA3 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |

5.11.48 MISCSYSPG Register (offset = ACh) [reset = X]
Figure 5-66. MISCSYSPG Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit Name | GPO1_ CTL3_msK | GPO1_ CTL6_msK | GPO4_ CTL3_msK | GPO4_ CTL6_msK | GPO2_ CTL3_msK | GPO2_ CTL6_msK | GPO3_ CTL3_msK | GPO3_ CTL6_msK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-54. MISCSYSPG Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7 | GPO1_CTL3_msK | R/W | X | 0: CTL3 pin status is part of Power Good tree of GPO1 pin. 1: CTL3 pin status is NOT part of Power Good tree of GPO1 pin. |
| 6 | GPO1_CTL6_msK | R/W | X | 0: CTL6 pin status is part of Power Good tree of GPO1 pin. 1: CTL6 pin status is NOT part of Power Good tree of GPO1 pin. |
| 5 | GPO4_CTL3_msK | R/W | X | 0: CTL3 pin status is part of Power Good tree of GPO4 pin. 1: CTL3 pin status is NOT part of Power Good tree of GPO4 pin. |
| 4 | GPO4_CTL6_msK | R/W | X | 0: CTL6 pin status is part of Power Good tree of GPO4 pin. 1: CTL6 pin status is NOT part of Power Good tree of GPO4 pin. |
| 3 | GPO2_CTL3_msK | R/W | X | 0: CTL3 pin status is part of Power Good tree of GPO2 pin. 1: CTL3 pin status is NOT part of Power Good tree of GPO2 pin. |
| 2 | GPO2_CTL6_msK | R/W | X | 0: CTL6 pin status is part of Power Good tree of GPO2 pin. 1: CTL6 pin status is NOT part of Power Good tree of GPO2 pin. |
| 1 | GPO3_CTL3_msK | R/W | X | 0: CTL3 pin status is part of Power Good tree of GPO3 pin. 1: CTL3 pin status is NOT part of Power Good tree of GPO3pin. |
| 0 | GPO3_CTL6_msK | R/W | X | 0: CTL6 pin status is part of Power Good tree of GPO3 pin. 1: CTL6 pin status is NOT part of Power Good tree of GPO3 pin. |

5.11.48.1 VTT_DISCH_CTRL Register (offset = ADh) [reset = X]

Figure 5-67. VTT_DISCH_CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|------------|----------|----------|----------|----------|
| Bit Name | RESERVED | RESERVED | RESERVED | VTT_DISCHG | RESERVED | RESERVED | RESERVED | RESERVED |
| TPS65086100 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-55. VTT_DISCH_CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|--|
| 7:5 | RESERVED | R/W | X | Reserved bits. Always write to match OTP settings. |
| 4 | VTT_DISCHG | R/W | X | 0: no discharge 1: 100 Ω |
| 3:0 | RESERVED | R/W | X | Reserved bits. Always write to match OTP settings. |

5.11.49 LDOA1_SWB2_CTRL: LDOA1 and SWB2 Control Register (offset = AEh) [reset = X]

Figure 5-68. LDOA1_SWB2_CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|------------------------|--------------|--------------|--------------|--------------|---------------|
| Bit Name | LDOA1_DISCHG[1] | LDOA1_DISCHG[0] | LDOA1_SWB2_SDWN_CONFIG | LDOA1 VID[3] | LDOA1 VID[2] | LDOA1 VID[1] | LDOA1 VID[0] | LDOA1_SWB2_EN |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-56. LDOA1_SWB2_CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|---|
| 7:6 | LDOA1_DISCHG[1:0] | R/W | X | LDOA1 discharge resistance 00: no discharge 01: 100 Ω 10: 200 Ω 11: 500 Ω |
| 5 | LDOA1_SWB2_SDWN_CONFIG | R/W | X | Control for Disabling LDOA1 or SWB2 (OTP dependent) during Emergency Shutdown. When LDOA1 is used in sequence and SWB1 and SWB2 are not merged, this will control SWB2. 0: LDOA1 or SWB2 will turn off during Emergency Shutdown for factory-programmable duration of 1 ms, 5 ms, 10 ms, or 100 ms. 1: LDOA1 or SWB2 is controlled by LDOA1_SWB2_EN bit only. LDOA1 for: OTP Dependent SWB2 for: OTP Dependent Unused for: OTP Dependent |
| 4:1 | LDOA1 VID[3:0] | R/W | X | This field sets the LDOA1 regulator output regulation voltage. See Table 5-4 for V _{OUT} options. |
| 0 | LDOA1_SWB2_EN | R/W | X | LDOA1 or SWB2 Enable Bit. 0: Disable. 1: Enable. LDOA1 for: OTP Dependent SWB2 for: OTP Dependent Unused for: OTP Dependent |

5.11.50 PG_STATUS1: 1st Power Good Status Register (offset = B0h) [reset = 0000 0000]
Figure 5-69. PG_STATUS1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------|------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Bit Name | LDOA2_PGOOD | SWA1_PGOOD | BUCK6_PGOOD | BUCK5_PGOOD | BUCK4_PGOOD | BUCK3_PGOOD | BUCK2_PGOOD | BUCK1_PGOOD |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

Table 5-57. PG_STATUS1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7 | LDOA2_PGOOD | R | 0 | LDOA2 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 6 | SWA1_PGOOD | R | 0 | SWA1 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 5 | BUCK6_PGOOD | R | 0 | BUCK6 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 4 | BUCK5_PGOOD | R | 0 | BUCK5 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 3 | BUCK4_PGOOD | R | 0 | BUCK4 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 2 | BUCK3_PGOOD | R | 0 | BUCK3 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 1 | BUCK2_PGOOD | R | 0 | BUCK2 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 0 | BUCK1_PGOOD | R | 0 | BUCK1 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |

5.11.51 PG_STATUS2: 2nd Power Good Status Register (offset = B1h) [reset = 0000 0000]

Figure 5-70. PG_STATUS2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|------------|-------------|-----------|------------|------------|-------------|
| Bit Name | RESERVED | RESERVED | LDO5_PGOOD | LDOA1_PGOOD | VTT_PGOOD | SWB2_PGOOD | SWB1_PGOOD | LDOA3_PGOOD |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

Table 5-58. PG_STATUS2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 5 | LDO5_PGOOD | R | 0 | LDO5 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 4 | LDOA1_PGOOD | R | 0 | LDOA1 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 3 | VTT_PGOOD | R | 0 | VTT LDO Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 2 | SWB2_PGOOD | R | 0 | SWB2 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 1 | SWB1_PGOOD | R | 0 | SWB1 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |
| 0 | LDOA3_PGOOD | R | 0 | LDOA3 Power Good status. 0: The output is not in target regulation range. 1: The output is in target regulation range. |

5.11.52 PWR_FAULT_STATUS1: 1st Power Fault Status Register (offset = B2h) [reset = 0000 0000]
Figure 5-71. PWR_FAULT_STATUS1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit Name | LDOA2_PWRFLT | SWA1_PWRFLT | BUCK6_PWRFLT | BUCK5_PWRFLT | BUCK4_PWRFLT | BUCK3_PWRFLT | BUCK2_PWRFLT | BUCK1_PWRFLT |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-59. PWR_FAULT_STATUS1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | LDOA2_PWRFLT | R | 0 | This fields indicates that LDOA2 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 6 | SWA1_PWRFLT | R | 0 | This fields indicates that SWA1 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 5 | BUCK6_PWRFLT | R | 0 | This fields indicates that BUCK6 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 4 | BUCK5_PWRFLT | R | 0 | This fields indicates that BUCK5 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 3 | BUCK4_PWRFLT | R | 0 | This fields indicates that BUCK4 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 2 | BUCK3_PWRFLT | R | 0 | This fields indicates that BUCK3 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 1 | BUCK2_PWRFLT | R | 0 | This fields indicates that BUCK2 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 0 | BUCK1_PWRFLT | R | 0 | This fields indicates that BUCK1 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |

5.11.53 PWR_FAULT_STATUS2: 2nd Power Fault Status Register (offset = B3h) [reset = 0000 0000]

Figure 5-72. PWR_FAULT_STATUS2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|--------------|------------|-------------|-------------|--------------|
| Bit Name | RESERVED | RESERVED | RESERVED | LDOA1_PWRFLT | VTT_PWRFLT | SWB2_PWRFLT | SWB1_PWRFLT | LDOA3_PWRFLT |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-60. PWR_FAULT_STATUS2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4 | LDOA1_PWRFLT | R/W | 0 | This fields indicates that LDOA1 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 3 | VTT_PWRFLT | R/W | 0 | This fields indicates that VTT LDO has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 2 | SWB2_PWRFLT | R/W | 0 | This fields indicates that SWB2 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 1 | SWB1_PWRFLT | R/W | 0 | This fields indicates that SWB1 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |
| 0 | LDOA3_PWRFLT | R/W | 0 | This fields indicates that LDOA3 has lost its regulation. 0: No Fault. 1: Power fault has occurred. The host to write 1 to clear. |

5.11.54 **TEMPCRIT: Temperature Fault Status Register (offset = B4h) [reset = 0000 0000]**

Asserted when an internal temperature sensor detects rise of die temperature above the CRITICAL temperature threshold (T_{CRIT}). There are 5 temperature sensors across the die.

Figure 5-73. TEMPCRIT Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|----------|----------------|---------------|-------------------|
| Bit Name | RESERVED | RESERVED | RESERVED | DIE_CRIT | VTT_CRIT | TOP-RIGHT_CRIT | TOP-LEFT_CRIT | BOTTOM-RIGHT_CRIT |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R/W |

Table 5-61. TEMPCRIT Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 4 | DIE_CRIT | R/W | 0 | Temperature of rest of die has exceeded T_{CRIT} . 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 3 | VTT_CRIT | R/W | 0 | Temperature of VTT LDO has exceeded T_{CRIT} . 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 2 | TOP-RIGHT_CRIT | R/W | 0 | Temperature of die Top-Right has exceeded T_{CRIT} . Top-Right corner of die from top view given pin1 is in Top-Left corner. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 1 | TOP-LEFT_CRIT | R/W | 0 | Temperature of die Top-Left has exceeded T_{CRIT} . Top-Left corner of die from top view given pin1 is in Top-Left corner. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 0 | BOTTOM-RIGHT_CRIT | R/W | 0 | Temperature of die Bottom-Right has exceeded T_{CRIT} . Bottom-Right corner of die from top view given pin1 is in Top-Left corner. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |

5.11.55 *TEMPHOT: Temperature Hot Status Register (offset = B5h) [reset = 0000 0000]*

Asserted when an internal temperature sensor detects rise of die temperature above the HOT temperature threshold (T_{HOT}). There are 5 temperature sensors across the die.

Figure 5-74. TEMPHOT Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|---------|---------|---------------|--------------|------------------|
| Bit Name | RESERVED | RESERVED | RESERVED | DIE_HOT | VTT_HOT | TOP-RIGHT_HOT | TOP-LEFT_HOT | BOTTOM-RIGHT_HOT |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R/W |

Table 5-62. TEMPHOT Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 4 | DIE_HOT | R/W | 0 | Temperature of rest of die has exceeded T_{HOT} . 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 3 | VTT_HOT | R/W | 0 | Temperature of VTT LDO has exceeded T_{HOT} . 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 2 | TOP-RIGHT_HOT | R/W | 0 | Temperature of Top-Right has exceeded T_{HOT} . Top-Right corner of die from top view given pin1 is in Top-Left corner. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 1 | TOP-LEFT_HOT | R/W | 0 | Temperature of Top-Left has exceeded T_{HOT} . Top-Left corner of die from top view given pin1 is in Top-Left corner. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 0 | BOTTOM-RIGHT_HOT | R/W | 0 | Temperature of Bottom-Right has exceeded T_{HOT} . Bottom-Right corner of die from top view given pin1 is in Top-Left corner. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |

5.11.56 OC_STATUS: Overcurrent Fault Status Register (offset = B6h) [reset = 0000 0000]

Asserted when overcurrent condition is detected from a LSD FET.

Figure 5-75. OC_STATUS Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | BUCK6_OC | BUCK2_OC | BUCK1_OC |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R/W | R/W | R/W |

Table 5-63. OC_STATUS Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 2 | BUCK6_OC | R/W | 0 | BUCK6 LSD FET overcurrent has been detected. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 1 | BUCK2_OC | R/W | 0 | BUCK2 LSD FET overcurrent has been detected. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |
| 0 | BUCK1_OC | R/W | 0 | BUCK1 LSD FET overcurrent has been detected. 0: Not asserted. 1: Asserted. The host to write 1 to clear. |

5.12 I²C Address: 0x38 Register Maps

5.12.1 Register Map Summary

This section describes the registers that can be accessed using I²C address 0x38. These registers can only be accessed by putting the device into programming mode. See the [TPS65086100 OTP Memory Programming Guide](#) for more information on putting the device into programming mode. It is recommended to use the OTP generator tool to make changes to these OTP settings. Do not attempt to write a RESERVED R/W bit to the opposite value. When the reset value of a bit register is 0bX, it means the bit value is coming from the OTP memory.

NOTE

There are additional registers not shown that are set by the OTP generator tool.

Table 5-64.

| Address | Name | Short Description |
|---------|----------------|--|
| 02h | OTP_CTRL1 | OTP control register for programming. |
| 03h | OTP_CTRL2 | OTP control register for selecting OTP bank. |
| 07h | BUCK1_CTRL_EN1 | BUCK1 enable control register 1. |
| 08h | BUCK1_CTRL_EN2 | BUCK1 enable control register 2. |
| 09h | BUCK1_CTRL_EN3 | BUCK1 enable control register 3. |
| 0Ah | BUCK2_CTRL_EN1 | BUCK2 enable control register 1. |
| 0Bh | BUCK2_CTRL_EN2 | BUCK2 enable control register 2. |
| 0Ch | BUCK2_CTRL_EN3 | BUCK2 enable control register 3. |
| 0Dh | BUCK3_CTRL_EN1 | BUCK3 enable control register 1. |
| 0Eh | BUCK3_CTRL_EN2 | BUCK3 enable control register 2. |
| 0Fh | BUCK3_CTRL_EN3 | BUCK3 enable control register 3. |
| 10h | BUCK4_CTRL_EN1 | BUCK4 enable control register 1. |
| 11h | BUCK4_CTRL_EN2 | BUCK4 enable control register 2. |

Table 5-64. (continued)

| Address | Name | Short Description |
|---------|---------------------|---|
| 12h | BUCK4_CTRL_EN3 | BUCK4 enable control register 3. |
| 13h | BUCK5_CTRL_EN1 | BUCK5 enable control register 1. |
| 14h | BUCK5_CTRL_EN2 | BUCK5 enable control register 2. |
| 15h | BUCK5_CTRL_EN3 | BUCK5 enable control register 3. |
| 16h | BUCK6_CTRL_EN1 | BUCK6 enable control register 1. |
| 17h | BUCK6_CTRL_EN2 | BUCK6 enable control register 2. |
| 18h | BUCK6_CTRL_EN3 | BUCK6 enable control register 3. |
| 19h | SWA1_CTRL_EN1 | SWA1 enable control register 1. |
| 1Ah | SWA1_CTRL_EN2 | SWA1 enable control register 2. |
| 1Bh | SWA1_CTRL_EN3 | SWA1 enable control register 3. |
| 1Ch | LDOA2_CTRL_EN1 | LDOA2 enable control register 1. |
| 1Dh | LDOA2_CTRL_EN2 | LDOA2 enable control register 2. |
| 1Eh | LDOA2_CTRL_EN3 | LDOA2 enable control register 3. |
| 1Fh | LDOA3_CTRL_EN1 | LDOA3 enable control register 1. |
| 20h | LDOA3_CTRL_EN2 | LDOA3 enable control register 2. |
| 21h | LDOA3_CTRL_EN3 | LDOA3 enable control register 3. |
| 22h | SWB1_CTRL_EN1 | SWB1 enable control register 1. |
| 23h | SWB1_CTRL_EN2 | SWB1 enable control register 2. |
| 24h | SWB1_CTRL_EN3 | SWB1 enable control register 3. |
| 25h | SWB2_LDOA1_CTRL_EN1 | SWB2 or LDOA1 enable control register 1. |
| 26h | SWB2_LDOA1_CTRL_EN2 | SWB2 or LDOA1 enable control register 2. |
| 27h | SWB2_LDOA1_CTRL_EN3 | SWB2 or LDOA1 enable control register 3. |
| 29h | SLP_PIN | Sleep pin select for BUCK1-6, LDOA2, and LDOA3. |
| 2Ah | OUTPUT_MODE | GPO output mode control. |
| 5Fh | I2C_SLAVE_ADDR | I ² C address control |

5.12.2 OTP_CTRL1 (offset = 02h) [reset = 0010 0000]
Figure 5-76. OTP_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|----------|----------|----------|----------|----------|-------------|----------|
| Bit Name | PROGRAMMING_STATE | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PROGRAM_OTP | RESERVED |
| TPS65086100 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-65. OTP_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7 | PROGRAMMING_STATE | R/W | 0 | 0: Programming mode not enabled (unless 7 V is applied to CTL4 pin). 1: Programming mode enabled, regardless of CTL4 pin voltage. |
| 1 | PROGRAM_OTP | R/W | 0 | Burns current register settings into selected OTP bank. Self clearing. 0: Not asserted. 1: Asserted. |

5.12.3 OTP_CTRL2 (offset = 03h) [reset = X]

Figure 5-77. OTP_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | OTP_BANK |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-66. OTP_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 0 | OTP_BANK | R/W | X | Determines which OTP bank to program into when PROGRAM_OTP is asserted. 0: Bank 0. 1: Bank 1. |

5.12.4 BUCK1_CTRL_EN1 (offset = 07h) [reset = X]

Figure 5-78. BUCK1_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | BUCK1_LDOA3_PGM | BUCK1_LDOA2_PGM | BUCK1_SWA1_PGM | BUCK1_BUCK6_PGM | BUCK1_BUCK5_PGM | BUCK1_BUCK4_PGM | BUCK1_BUCK3_PGM | BUCK1_BUCK2_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-67. BUCK1_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | BUCK1_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | BUCK1_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | BUCK1_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | BUCK1_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: BUCK6 PGOOD is part of Enable Logic. 1: BUCK6 PGOOD is masked and is not part of enable logic. |
| 3 | BUCK1_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 2 | BUCK1_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 1 | BUCK1_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK1_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |

5.12.5 BUCK1_CTRL_EN2 (offset = 08h) [reset = X]

Figure 5-79. BUCK1_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | RESERVED | RESERVED | BUCK1_STEP_SIZE | BUCK1_PINEN_SEL[2] | BUCK1_PINEN_SEL[1] | BUCK1_PINEN_SEL[0] | BUCK1_SWB2_LDOA1_PGM | BUCK1_SWB1_PGM |
| TPS65086100 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-68. BUCK1_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|--|
| 5 | BUCK1_STEP_SIZE ⁽¹⁾ | R/W | X | BUCK1 step size. 0: 10 mV 1: 25 mV |
| 4:2 | BUCK1_PINEN_SEL[2:0] | R/W | X | BUCK1 Enable pin select. 000: CTL1 001: CTL2 010: CTL5 011: CTL4 100: CTL3 101: CTL3 and CTL4 110: CTL6 111: 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | BUCK1_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0: SWB2_LDOA1 PGOOD is part of Enable Logic. 1: SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK1_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0: SWB1 PGOOD is part of Enable Logic. 1: SWB1 PGOOD is masked and is not part of enable logic. |

(1) Should only be changed using the OTP generator tool.

5.12.6 BUCK1_CTRL_EN3 (offset = 09h) [reset = X]
Figure 5-80. BUCK1_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | RESERVED | RESERVED | BUCK1_FALLING_EDGE_DLY[2] | BUCK1_FALLING_EDGE_DLY[1] | BUCK1_FALLING_EDGE_DLY[0] | BUCK1_RISING_EDGE_DLY[2] | BUCK1_RISING_EDGE_DLY[1] | BUCK1_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-69. BUCK1_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 5:3 | BUCK1_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of BUCK1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | BUCK1_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of BUCK1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.7 BUCK2_CTRL_EN1 (offset = 0Ah) [reset = X]

Figure 5-81. BUCK2_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | BUCK2_LDOA3_PGM | BUCK2_LDOA2_PGM | BUCK2_SWA1_PGM | BUCK2_BUCK6_PGM | BUCK2_BUCK5_PGM | BUCK2_BUCK4_PGM | BUCK2_BUCK3_PGM | BUCK2_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-70. BUCK2_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | BUCK2_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | BUCK2_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | BUCK2_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | BUCK2_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: BUCK6 PGOOD is part of Enable Logic. 1: BUCK6 PGOOD is masked and is not part of enable logic. |
| 3 | BUCK2_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 2 | BUCK2_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 1 | BUCK2_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK2_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.8 BUCK2_CTRL_EN2 (offset = 0Bh) [reset = X]

Figure 5-82. BUCK2_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | RESERVED | RESERVED | BUCK2_STEP_SIZE | BUCK2_PINEN_SEL[2] | BUCK2_PINEN_SEL[1] | BUCK2_PINEN_SEL[0] | BUCK2_SWB2_LDOA1_PGM | BUCK2_SWB1_PGM |
| TPS65086100 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-71. BUCK2_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|--|
| 5 | BUCK2_STEP_SIZE ⁽¹⁾ | R/W | X | BUCK2 step size. 0: 10 mV 1: 25 mV |
| 4:2 | BUCK2_PINEN_SEL[2:0] | R/W | X | BUCK2 Enable pin select. 000: CTL1 001: CTL2 010: CTL5 011: CTL4 100: CTL3 101: CTL3 and CTL4 110: CTL6 111: 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | BUCK2_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0: SWB2_LDOA1 PGOOD is part of Enable Logic. 1: SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK2_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0: SWB1 PGOOD is part of Enable Logic. 1: SWB1 PGOOD is masked and is not part of enable logic. |

(1) Should only be changed using the OTP generator tool.

5.12.9 BUCK2_CTRL_EN3 (offset = 0Ch) [reset = X]

Figure 5-83. BUCK2_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | RESERVED | RESERVED | BUCK2_FALLING_EDGE_DLY[2] | BUCK2_FALLING_EDGE_DLY[1] | BUCK2_FALLING_EDGE_DLY[0] | BUCK2_RISING_EDGE_DLY[2] | BUCK2_RISING_EDGE_DLY[1] | BUCK2_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-72. BUCK2_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 5:3 | BUCK2_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of BUCK2 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | BUCK2_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of BUCK2 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.10 BUCK3_CTRL_EN1 (offset = 0Ah) [reset = X]
Figure 5-84. BUCK3_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | BUCK3_LDOA3_PGM | BUCK3_LDOA2_PGM | BUCK3_SWA1_PGM | BUCK3_BUCK6_PGM | BUCK3_BUCK5_PGM | BUCK3_BUCK4_PGM | BUCK3_BUCK2_PGM | BUCK3_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-73. BUCK3_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | BUCK3_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | BUCK3_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | BUCK3_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | BUCK3_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: BUCK6 PGOOD is part of Enable Logic. 1: BUCK6 PGOOD is masked and is not part of enable logic. |
| 3 | BUCK3_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 2 | BUCK3_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 1 | BUCK3_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK3_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.11 BUCK3_CTRL_EN2 (offset = 0Eh) [reset = X]

Figure 5-85. BUCK3_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | RESERVED | RESERVED | RESERVED | BUCK3_PINEN_SEL[2] | BUCK3_PINEN_SEL[1] | BUCK3_PINEN_SEL[0] | BUCK3_SWB2_LDOA1_PGM | BUCK3_SWB1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-74. BUCK3_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 4:2 | BUCK3_PINEN_SEL[2:0] | R/W | X | BUCK3 Enable pin select. 000 : CTL1 001 : CTL2 010 : CTL5 011 : CTL4 100 : CTL3 101 : CTL3 and CTL4 110 : CTL6 111 : 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | BUCK3_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0 : SWB2_LDOA1 PGOOD is part of Enable Logic. 1 : SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK3_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0 : SWB1 PGOOD is part of Enable Logic. 1 : SWB1 PGOOD is masked and is not part of enable logic. |

5.12.12 BUCK3_CTRL_EN3 (offset = 0Fh) [reset = X]
Figure 5-86. BUCK3_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | RESERVED | RESERVED | BUCK3_FALLING_EDGE_DLY[2] | BUCK3_FALLING_EDGE_DLY[1] | BUCK3_FALLING_EDGE_DLY[0] | BUCK3_RISING_EDGE_DLY[2] | BUCK3_RISING_EDGE_DLY[1] | BUCK3_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-75. BUCK3_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 5:3 | BUCK3_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of BUCK3 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | BUCK3_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of BUCK3 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.13 BUCK4_CTRL_EN1 (offset = 10h) [reset = X]

Figure 5-87. BUCK4_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | BUCK4_LDOA3_PGM | BUCK4_LDOA2_PGM | BUCK4_SWA1_PGM | BUCK4_BUCK6_PGM | BUCK4_BUCK5_PGM | BUCK4_BUCK3_PGM | BUCK4_BUCK2_PGM | BUCK4_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-76. BUCK4_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | BUCK4_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | BUCK4_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | BUCK4_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | BUCK4_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: BUCK6 PGOOD is part of Enable Logic. 1: BUCK6 PGOOD is masked and is not part of enable logic. |
| 3 | BUCK4_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 2 | BUCK4_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | BUCK4_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK4_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.14 BUCK4_CTRL_EN2 (offset = 11h) [reset = X]
Figure 5-88. BUCK4_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | RESERVED | RESERVED | RESERVED | BUCK4_PINEN_SEL[2] | BUCK4_PINEN_SEL[1] | BUCK4_PINEN_SEL[0] | BUCK4_SWB2_LDOA1_PGM | BUCK4_SWB1_PGM |
| TPS65086100 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-77. BUCK4_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 4:2 | BUCK4_PINEN_SEL[2:0] | R/W | X | BUCK4 Enable pin select. 000 : CTL1 001 : CTL2 010 : CTL5 011 : CTL4 100 : CTL3 101 : CTL3 and CTL4 110 : CTL6 111 : 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | BUCK4_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0 : SWB2_LDOA1 PGOOD is part of Enable Logic. 1 : SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK4_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0 : SWB1 PGOOD is part of Enable Logic. 1 : SWB1 PGOOD is masked and is not part of enable logic. |

5.12.15 BUCK4_CTRL_EN3 (offset = 12h) [reset = X]

Figure 5-89. BUCK4_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | RESERVED | RESERVED | BUCK4_FALLING_EDGE_DLY[2] | BUCK4_FALLING_EDGE_DLY[1] | BUCK4_FALLING_EDGE_DLY[0] | BUCK4_RISING_EDGE_DLY[2] | BUCK4_RISING_EDGE_DLY[1] | BUCK4_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-78. BUCK4_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 5:3 | BUCK4_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of BUCK4 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | BUCK4_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of BUCK4 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.16 BUCK5_CTRL_EN1 (offset = 13h) [reset = X]
Figure 5-90. BUCK5_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | BUCK5_LDOA3_PGM | BUCK5_LDOA2_PGM | BUCK5_SWA1_PGM | BUCK5_BUCK6_PGM | BUCK5_BUCK4_PGM | BUCK5_BUCK3_PGM | BUCK5_BUCK2_PGM | BUCK5_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-79. BUCK5_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | BUCK5_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | BUCK5_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | BUCK5_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | BUCK5_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: BUCK6 PGOOD is part of Enable Logic. 1: BUCK6 PGOOD is masked and is not part of enable logic. |
| 3 | BUCK5_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 2 | BUCK5_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | BUCK5_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK5_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.17 BUCK5_CTRL_EN2 (offset = 14h) [reset = X]

Figure 5-91. BUCK5_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | RESERVED | RESERVED | RESERVED | BUCK5_PINEN_SEL[2] | BUCK5_PINEN_SEL[1] | BUCK5_PINEN_SEL[0] | BUCK5_SWB2_LDOA1_PGM | BUCK5_SWB1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-80. BUCK5_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 4:2 | BUCK5_PINEN_SEL[2:0] | R/W | X | BUCK5 Enable pin select. 000 : CTL1 001 : CTL2 010 : CTL5 011 : CTL4 100 : CTL3 101 : CTL3 and CTL4 110 : CTL6 111 : 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | BUCK5_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0 : SWB2_LDOA1 PGOOD is part of Enable Logic. 1 : SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK5_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0 : SWB1 PGOOD is part of Enable Logic. 1 : SWB1 PGOOD is masked and is not part of enable logic. |

5.12.18 BUCK5_CTRL_EN3 (offset = 15h) [reset = X]
Figure 5-92. BUCK5_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | RESERVED | RESERVED | BUCK5_FALLING_EDGE_DLY[2] | BUCK5_FALLING_EDGE_DLY[1] | BUCK5_FALLING_EDGE_DLY[0] | BUCK5_RISING_EDGE_DLY[2] | BUCK5_RISING_EDGE_DLY[1] | BUCK5_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-81. BUCK5_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 5:3 | BUCK5_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of BUCK5 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | BUCK5_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of BUCK5 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.19 BUCK6_CTRL_EN1 (offset = 16h) [reset = X]

Figure 5-93. BUCK6_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | BUCK6_LDOA3_PGM | BUCK6_LDOA2_PGM | BUCK6_SWA1_PGM | BUCK6_BUCK5_PGM | BUCK6_BUCK4_PGM | BUCK6_BUCK3_PGM | BUCK6_BUCK2_PGM | BUCK6_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-82. BUCK6_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | BUCK6_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | BUCK6_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | BUCK6_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | BUCK6_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 3 | BUCK6_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 2 | BUCK6_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | BUCK6_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK6_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.20 BUCK6_CTRL_EN2 (offset = 17h) [reset = X]
Figure 5-94. BUCK6_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|-----------------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | RESERVED | RESERVED | BUCK6_STEP_SIZE | BUCK6_PINEN_SEL[2] | BUCK6_PINEN_SEL[1] | BUCK6_PINEN_SEL[0] | BUCK6_SWB2_LDOA1_PGM | BUCK6_SWB1_PGM |
| TPS65086100 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-83. BUCK6_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|--|
| 5 | BUCK6_STEP_SIZE ⁽¹⁾ | R/W | X | BUCK6 step size. 0: 10 mV 1: 25 mV |
| 4:2 | BUCK6_PINEN_SEL[2:0] | R/W | X | BUCK6 Enable pin select. 000: CTL1 001: CTL2 010: CTL5 011: CTL4 100: CTL3 101: CTL3 and CTL4 110: CTL6 111: 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | BUCK6_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0: SWB2_LDOA1 PGOOD is part of Enable Logic. 1: SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | BUCK6_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0: SWB1 PGOOD is part of Enable Logic. 1: SWB1 PGOOD is masked and is not part of enable logic. |

(1) Should only be changed using the OTP generator tool.

5.12.21 BUCK6_CTRL_EN3 (offset = 18h) [reset = X]

Figure 5-95. BUCK6_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | RESERVED | RESERVED | BUCK6_FALLING_EDGE_DLY[2] | BUCK6_FALLING_EDGE_DLY[1] | BUCK6_FALLING_EDGE_DLY[0] | BUCK6_RISING_EDGE_DLY[2] | BUCK6_RISING_EDGE_DLY[1] | BUCK6_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-84. BUCK6_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 5:3 | BUCK6_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of BUCK6 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | BUCK6_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of BUCK6 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.22 SWA1_CTRL_EN1 (offset = 19h) [reset = X]
Figure 5-96. SWA1_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit Name | SWA1_LDOA3_PGM | SWA1_LDOA2_PGM | SWA1_BUCK6_PGM | SWA1_BUCK5_PGM | SWA1_BUCK4_PGM | SWA1_BUCK3_PGM | SWA1_BUCK2_PGM | SWA1_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-85. SWA1_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | SWA1_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | SWA1_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | SWA1_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | SWA1_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 3 | SWA1_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 2 | SWA1_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | SWA1_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | SWA1_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.23 SWA1_CTRL_EN2 (offset = 1Ah) [reset = X]

Figure 5-97. SWA1_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------------|----------------|-------------------|-------------------|-------------------|---------------------|---------------|
| Bit Name | RESERVED | SWA1_PG_SEL[1] | SWA1_PG_SEL[0] | SWA1_PINEN_SEL[2] | SWA1_PINEN_SEL[1] | SWA1_PINEN_SEL[0] | SWA1_SWB2_LDOA1_PGM | SWA1_SWB1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-86. SWA1_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 6:5 | SWA1_PG_SEL[1:0] | R/W | X | SWA1 PGOOD select.. 00 : 1.5 V 01 : 1.8 V 10 : 2.5 V 11 : 3.3 V |
| 4:2 | SWA1_PINEN_SEL[2:0] | R/W | X | SWA1 Enable pin select. 000 : CTL1 001 : CTL2 010 : CTL5 011 : CTL4 100 : CTL3 101 : CTL3 and CTL4 110 : CTL6 111 : 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | SWA1_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0 : SWB2_LDOA1 PGOOD is part of Enable Logic. 1 : SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | SWA1_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0 : SWB1 PGOOD is part of Enable Logic. 1 : SWB1 PGOOD is masked and is not part of enable logic. |

5.12.24 SWA1_CTRL_EN3 (offset = 1Bh) [reset = X]
Figure 5-98. SWA1_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|------------|--------------------------|--------------------------|--------------------------|-------------------------|-------------------------|-------------------------|
| Bit Name | RESERVED | VTT_EN_SEL | SWA1_FALLING_EDGE_DLY[2] | SWA1_FALLING_EDGE_DLY[1] | SWA1_FALLING_EDGE_DLY[0] | SWA1_RISING_EDGE_DLY[2] | SWA1_RISING_EDGE_DLY[1] | SWA1_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-87. SWA1_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 6 | VTT_EN_SEL | R/W | X | Pin Select for VTT EN Logic 0 : CTL3 1 : CTL6 |
| 5:3 | SWA1_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of SWA1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | SWA1_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of SWA1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.25 LDOA2_CTRL_EN1 (offset = 1Ch) [reset = X]

Figure 5-99. LDOA2_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | LDOA2_LDOA3_PGM | LDOA2_SWA1_PGM | LDOA2_BUCK6_PGM | LDOA2_BUCK5_PGM | LDOA2_BUCK4_PGM | LDOA2_BUCK3_PGM | LDOA2_BUCK2_PGM | LDOA2_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-88. LDOA2_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | LDOA2_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | LDOA2_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | LDOA2_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | LDOA2_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 3 | LDOA2_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 2 | LDOA2_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | LDOA2_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | LDOA2_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.26 LDOA2_CTRL_EN2 (offset = 1Dh) [reset = X]
Figure 5-100. LDOA2_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | RESERVED | RESERVED | RESERVED | LDOA2_PINEN_SEL[2] | LDOA2_PINEN_SEL[1] | LDOA2_PINEN_SEL[0] | LDOA2_SWB2_LDOA1_PGM | LDOA2_SWB1_PGM |
| TPS65086100 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-89. LDOA2_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 4:2 | LDOA2_PINEN_SEL[2:0] | R/W | X | LDOA2 Enable pin select. 000 : CTL1 001 : CTL2 010 : CTL5 011 : CTL4 100 : CTL3 101 : CTL3 and CTL4 110 : CTL6 111 : 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | LDOA2_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0 : SWB2_LDOA1 PGOOD is part of Enable Logic. 1 : SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | LDOA2_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0 : SWB1 PGOOD is part of Enable Logic. 1 : SWB1 PGOOD is masked and is not part of enable logic. |

5.12.27 LDOA2_CTRL_EN3 (offset = 1Eh) [reset = X]

Figure 5-101. LDOA2_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|--------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | ECLDO_DLY[1] | ECLDO_DLY[0] | LDOA2_FALLING_EDGE_DLY[2] | LDOA2_FALLING_EDGE_DLY[1] | LDOA2_FALLING_EDGE_DLY[0] | LDOA2_RISING_EDGE_DLY[2] | LDOA2_RISING_EDGE_DLY[1] | LDOA2_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-90. LDOA2_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 7:6 | LDOA1_SWB2_DLY[1:0] | R/W | X | Sets the off time for LDOA1 during shutdown (all Values have 10% variations). 00 : 1 ms 01 : 5 ms 10 : 10 ms 11 : 100 ms |
| 5:3 | LDOA2_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of LDOA2 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | LDOA2_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of LDOA2 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.28 LDOA3_CTRL_EN1 (offset = 1Fh) [reset = X]
Figure 5-102. LDOA3_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit Name | LDOA3_LDOA2_PGM | LDOA3_SWA1_PGM | LDOA3_BUCK6_PGM | LDOA3_BUCK5_PGM | LDOA3_BUCK4_PGM | LDOA3_BUCK3_PGM | LDOA3_BUCK2_PGM | LDOA3_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-91. LDOA3_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | LDOA3_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | LDOA3_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | LDOA3_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | LDOA3_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 3 | LDOA3_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 2 | LDOA3_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | LDOA3_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | LDOA3_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.29 LDOA3_CTRL_EN2 (offset = 20h) [reset = X]

Figure 5-103. LDOA3_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|----------|----------|--------------------|--------------------|--------------------|----------------------|----------------|
| Bit Name | BUCK6_VSEL_OPTION | RESERVED | RESERVED | LDOA3_PINEN_SEL[2] | LDOA3_PINEN_SEL[1] | LDOA3_PINEN_SEL[0] | LDOA3_SWB2_LDOA1_PGM | LDOA3_SWB1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-92. LDOA3_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7 | BUCK6_VSEL_OPTION | R/W | X | Determines whether high level on CTRL2 can set BUCK6 to 1.2 V. If step size is 25 mV the voltage will be 2.4 V. SLP pin will override this voltage. 0: CTRL2 has no effect. 1: CTRL2 controls output voltage. |
| 4:2 | LDOA3_PINEN_SEL[2:0] | R/W | X | LDOA3 Enable pin select. 000: CTL1 001: CTL2 010: CTL5 011: CTL4 100: CTL3 101: CTL3 and CTL4 110: CTL6 111: 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | LDOA3_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0: SWB2_LDOA1 PGOOD is part of Enable Logic. 1: SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | LDOA3_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0: SWB1 PGOOD is part of Enable Logic. 1: SWB1 PGOOD is masked and is not part of enable logic. |

5.12.30 LDOA3_CTRL_EN3 (offset = 21h) [reset = X]
Figure 5-104. LDOA3_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Bit Name | SWB12_EN | LDOA1_SWB2 | LDOA3_FALLING_EDGE_DLY[2] | LDOA3_FALLING_EDGE_DLY[1] | LDOA3_FALLING_EDGE_DLY[0] | LDOA3_RISING_EDGE_DLY[2] | LDOA3_RISING_EDGE_DLY[1] | LDOA3_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-93. LDOA3_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 7 | SWB12_EN | R/W | X | If set, combines the Enable logic for SWB1 and SWB2. 0 : Normal functionality. 1 : Enable logic for SWB1 is also used to enable SWB2. |
| 6 | LDOA1_SWB2 | R/W | X | Used to swap enable logic for LDOA1 and SWB2. 0 : Normal functionality. 1 : Enable logic for SWB2 (SWB2_LDOA1_CTRL_EN1, SWB2_LDOA1_CTRL_EN2, SWB2_LDOA1_CTRL_EN3, SWB2_LDOA1_msK, SWB2_LDOA1_EN, SWB2_LDOA1_DIS) is used for LDOA1 and Enable logic for LDOA1 (LDOA1_SWB2_EN, LDOA1_SWB2_DLY, LDOA1_SWB2_SDWN_CON FIG) is used for SWB2. |
| 5:3 | LDOA3_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of LDOA3 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | LDOA3_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of LDOA3 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.31 SWB1_CTRL_EN1 (offset = 22h) [reset = X]

Figure 5-105. SWB1_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit Name | SWB1_LDOA2_PGM | SWB1_SWA1_PGM | SWB1_BUCK6_PGM | SWB1_BUCK5_PGM | SWB1_BUCK4_PGM | SWB1_BUCK3_PGM | SWB1_BUCK2_PGM | SWB1_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-94. SWB1_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | SWB1_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 6 | SWB1_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 5 | SWB1_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: BUCK6 PGOOD is part of Enable Logic. 1: BUCK6 PGOOD is masked and is not part of enable logic. |
| 4 | SWB1_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 3 | SWB1_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 2 | SWB1_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | SWB1_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | SWB1_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.32 SWB1_CTRL_EN2 (offset = 23h) [reset = X]
Figure 5-106. SWB1_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------------|----------------|-------------------|-------------------|-------------------|---------------------|----------------|
| Bit Name | RESERVED | SWB1_PG_SEL[1] | SWB1_PG_SEL[0] | SWB1_PINEN_SEL[2] | SWB1_PINEN_SEL[1] | SWB1_PINEN_SEL[0] | SWB1_SWB2_LDOA1_PGM | SWB1_LDOA3_PGM |
| TPS65086100 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-95. SWB1_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 6:5 | SWB1_PG_SEL[2:0] | R/W | X | SWB1 PGOOD select.. 00 : 1.5 V 01 : 1.8 V 10 : 2.5 V 11 : 3.3 V |
| 4:2 | SWB1_PINEN_SEL[2:0] | R/W | X | SWB1 Enable pin select. 000 : CTL1 001 : CTL2 010 : CTL5 011 : CTL4 100 : CTL3 101 : CTL3 and CTL4 110 : CTL6 111 : 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | SWB1_SWB2_LDOA1_PGM | R/W | X | SWB2_LDOA1 PGOOD masked 0 : SWB2_LDOA1 PGOOD is part of Enable Logic. 1 : SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | SWB1_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0 : LDOA3 PGOOD is part of Enable Logic. 1 : LDOA3 PGOOD is masked and is not part of enable logic. |

5.12.33 SWB1_CTRL_EN3 (offset = 24h) [reset = X]

Figure 5-107. SWB1_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|--------------------------|--------------------------|--------------------------|-------------------------|-------------------------|-------------------------|
| Bit Name | RESERVED | RESERVED | SWB1_FALLING_EDGE_DLY[2] | SWB1_FALLING_EDGE_DLY[1] | SWB1_FALLING_EDGE_DLY[0] | SWB1_RISING_EDGE_DLY[2] | SWB1_RISING_EDGE_DLY[1] | SWB1_RISING_EDGE_DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-96. SWB1_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 5:3 | SWB1_FALLING_EDGE_DLY[2:0] | R/W | X | Delay for falling edge of SWB1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | SWB1_RISING_EDGE_DLY[2:0] | R/W | X | Delay for rising edge of SWB1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.34 SWB2_LDOA1_CTRL_EN1 (offset = 25h) [reset = X]
Figure 5-108. SWB2_LDOA1_CTRL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Bit Name | SWB2_LDOA1_LDOA2_PGM | SWB2_LDOA1_SWA1_PGM | SWB2_LDOA1_BUCK6_PGM | SWB2_LDOA1_BUCK5_PGM | SWB2_LDOA1_BUCK4_PGM | SWB2_LDOA1_BUCK3_PGM | SWB2_LDOA1_BUCK2_PGM | SWB2_LDOA1_BUCK1_PGM |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-97. SWB2_LDOA1_CTRL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7 | SWB2_LDOA1_LDOA2_PGM | R/W | X | LDOA2 PGOOD masked 0: LDOA3 PGOOD is part of Enable Logic. 1: LDOA3 PGOOD is masked and is not part of enable logic. |
| 6 | SWB2_LDOA1_SWA1_PGM | R/W | X | SWA1 PGOOD masked 0: LDOA2 PGOOD is part of Enable Logic. 1: LDOA2 PGOOD is masked and is not part of enable logic. |
| 5 | SWB2_LDOA1_BUCK6_PGM | R/W | X | BUCK6 PGOOD masked 0: SWA1 PGOOD is part of Enable Logic. 1: SWA1 PGOOD is masked and is not part of enable logic. |
| 4 | SWB2_LDOA1_BUCK5_PGM | R/W | X | BUCK5 PGOOD masked 0: BUCK5 PGOOD is part of Enable Logic. 1: BUCK5 PGOOD is masked and is not part of enable logic. |
| 3 | SWB2_LDOA1_BUCK4_PGM | R/W | X | BUCK4 PGOOD masked 0: BUCK4 PGOOD is part of Enable Logic. 1: BUCK4 PGOOD is masked and is not part of enable logic. |
| 2 | SWB2_LDOA1_BUCK3_PGM | R/W | X | BUCK3 PGOOD masked 0: BUCK3 PGOOD is part of Enable Logic. 1: BUCK3 PGOOD is masked and is not part of enable logic. |
| 1 | SWB2_LDOA1_BUCK2_PGM | R/W | X | BUCK2 PGOOD masked 0: BUCK2 PGOOD is part of Enable Logic. 1: BUCK2 PGOOD is masked and is not part of enable logic. |
| 0 | SWB2_LDOA1_BUCK1_PGM | R/W | X | BUCK1 PGOOD masked 0: BUCK1 PGOOD is part of Enable Logic. 1: BUCK1 PGOOD is masked and is not part of enable logic. |

5.12.35 SWB2_LDOA1_CTRL_EN2 (offset = 26h) [reset = X]

Figure 5-109. SWB2_LDOA1_CTRL_EN2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|------------------------------|------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-----------------------------|----------------------------------|
| Bit Name | RESERVED | SWB2_LDO A1_ PG_SEL[1] | SWB2_LDO A1_ PG_SEL[0] | SWB2_LDO A1_ PINEN_ SEL[2] | SWB2_LDO A1_ PINEN_ SEL[1] | SWB2_LDO A1_ PINEN_ SEL[0] | SWB2_LDO A1_ SWB1_PGM | SWB2_LDO A1_ LDOA3_PG M |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-98. SWB2_LDOA1_CTRL_EN2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|---|
| 6:5 | SWB2_LDOA1_PG_SEL[1:0] | R/W | X | SWB2_LDOA1 PGOOD select.. 00 : 1.5 V 01 : 1.8 V 10 : 2.5 V 11 : 3.3 V |
| 4:2 | SWB2_LDOA1_PINEN_SEL[2:0] | R/W | X | SWB2_LDOA1 Enable pin select. 000 : CTL1 001 : CTL2 010 : CTL5 011 : CTL4 100 : CTL3 101 : CTL3 and CTL4 110 : CTL6 111 : 1 is inserted into CTL MUX. No pin is required to enable. |
| 1 | SWB2_LDOA1_SWB1_PGM | R/W | X | SWB1 PGOOD masked 0 : SWB2_LDOA1 PGOOD is part of Enable Logic. 1 : SWB2_LDOA1 PGOOD is masked and is not part of enable logic. |
| 0 | SWB2_LDOA1_LDOA3_PGM | R/W | X | LDOA3 PGOOD masked 0 : LDOA3 PGOOD is part of Enable Logic. 1 : LDOA3 PGOOD is masked and is not part of enable logic. |

5.12.36 SWB2_LDOA1_CTRL_EN3 (offset = 27h) [reset = X]
Figure 5-110. SWB2_LDOA1_CTRL_EN3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|--|--|--|---|---|---|
| Bit Name | RESERVED | RESERVED | SWB2_LDO A1_ FALLING_ EDGE_ DLY[2] | SWB2_LDO A1_ FALLING_ EDGE_ DLY[1] | SWB2_LDO A1_ FALLING_ EDGE_ DLY[0] | SWB2_LDO A1_ RISING_ EDGE_ DLY[2] | SWB2_LDO A1_ RISING_ EDGE_ DLY[1] | SWB2_LDO A1_ RISING_ EDGE_ DLY[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-99. SWB2_LDOA1_CTRL_EN3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------------|------|-------|---|
| 5:3 | SWB2_LDOA1_FALLING_ EDGE_DLY[2:0] | R/W | X | Delay for falling edge of SWB2_LDOA1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |
| 2:0 | SWB2_LDOA1_RISING_ EDGE_DLY[2:0] | R/W | X | Delay for rising edge of SWB2_LDOA1 Enable pin (all Values have 10% variations). 000 : No Delay. 001 : 2 ms Delay. 010 : 4 ms Delay. 011 : 8 ms Delay. 100 : 16 ms Delay. 101 : 24 ms Delay. 110 : 32 ms Delay. 111 : 64 ms Delay. |

5.12.37 SLP_PIN (offset = 29h) [reset = X]

Figure 5-111. SLP_PIN Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Bit Name | LDOA3_SLP_PIN | LDOA2_SLP_PIN | BUCK6_SLP_PIN | BUCK5_SLP_PIN | BUCK4_SLP_PIN | BUCK3_SLP_PIN | BUCK2_SLP_PIN | BUCK1_SLP_PIN |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-100. SLP_PIN Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--------------------------------------|
| 7 | LDOA3_SLP_PIN | R/W | X | LDOA3 SLP pin. 0: CTL3 1: CTL6 |
| 6 | LDOA2_SLP_PIN | R/W | X | LDOA2 SLP pin. 0: CTL3 1: CTL6 |
| 5 | BUCK6_SLP_PIN | R/W | X | BUCK6 SLP pin. 0: CTL3 1: CTL6 |
| 4 | BUCK5_SLP_PIN | R/W | X | BUCK5 SLP pin. 0: CTL3 1: CTL6 |
| 3 | BUCK4_SLP_PIN | R/W | X | BUCK4 SLP pin. 0: CTL3 1: CTL6 |
| 2 | BUCK3_SLP_PIN | R/W | X | BUCK3 SLP pin. 0: CTL3 1: CTL6 |
| 1 | BUCK2_SLP_PIN | R/W | X | BUCK2 SLP pin. 0: CTL3 1: CTL6 |
| 0 | BUCK1_SLP_PIN | R/W | X | BUCK1 SLP pin. 0: CTL3 1: CTL6 |

5.12.38 OUTPUT_MODE (offset = 2Ah) [reset = X]
Figure 5-112. OUTPUT_MODE Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|----------|----------|----------|----------|---------|---------|---------|
| Bit Name | GPO4_CTL | GPO3_CTL | GPO2_CTL | GPO1_CTL | RESERVED | GPO3_MD | GPO2_MD | GPO1_MD |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-101. OUTPUT_MODE Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | GPO4_CTL | R/W | X | GPO4 output control. 0: PGOOD logic 1: I ² C register |
| 6 | GPO3_CTL | R/W | X | GPO3 output control. 0: PGOOD logic 1: I ² C register |
| 5 | GPO2_CTL | R/W | X | GPO2 output control. 0: PGOOD logic 1: I ² C register |
| 4 | GPO1_CTL | R/W | X | GPO1 output control. 0: PGOOD logic 1: I ² C register |
| 2 | GPO3_MD | R/W | X | GPO3 mode. 0: Push-pull 1: Open drain |
| 1 | GPO2_MD | R/W | X | GPO2 mode. 0: Push-pull 1: Open drain |
| 0 | GPO1_MD | R/W | X | GPO1 mode. 0: Push-pull 1: Open drain |

5.12.39 I2C_SLAVE_ADDR (offset = 5Fh) [reset = X]

Figure 5-113. I2C_SLAVE_ADDR Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Bit Name | SLV_ADDR_SEL | SLV_ADDR[6] | SLV_ADDR[5] | SLV_ADDR[4] | SLV_ADDR[3] | SLV_ADDR[2] | SLV_ADDR[1] | SLV_ADDR[0] |
| TPS65086100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 5-102. I2C_SLAVE_ADDR Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7 | SLV_ADDR_SEL | R/W | X | Slave address select bit. 0 : Use default 0x5E address 1 : Use programmable slave address |
| 6:0 | SLV_ADDR[6:0] | R/W | X | 6 bit programmable slave address. 0000000 : Reserved due to I ² C standard specifications. ... 0001000 : Reserved due to I ² C standard specifications. 0001001 : 0x08 ... 0110111 : 0x37 0111000 : Reserved for registers accessible by I ² C address 0x38. 0111001 : 0x39 ... 1110111 : 0x77 1111000 : Reserved due to I ² C standard specifications. ... 1111111 : Reserved due to I ² C standard specifications. |

6 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

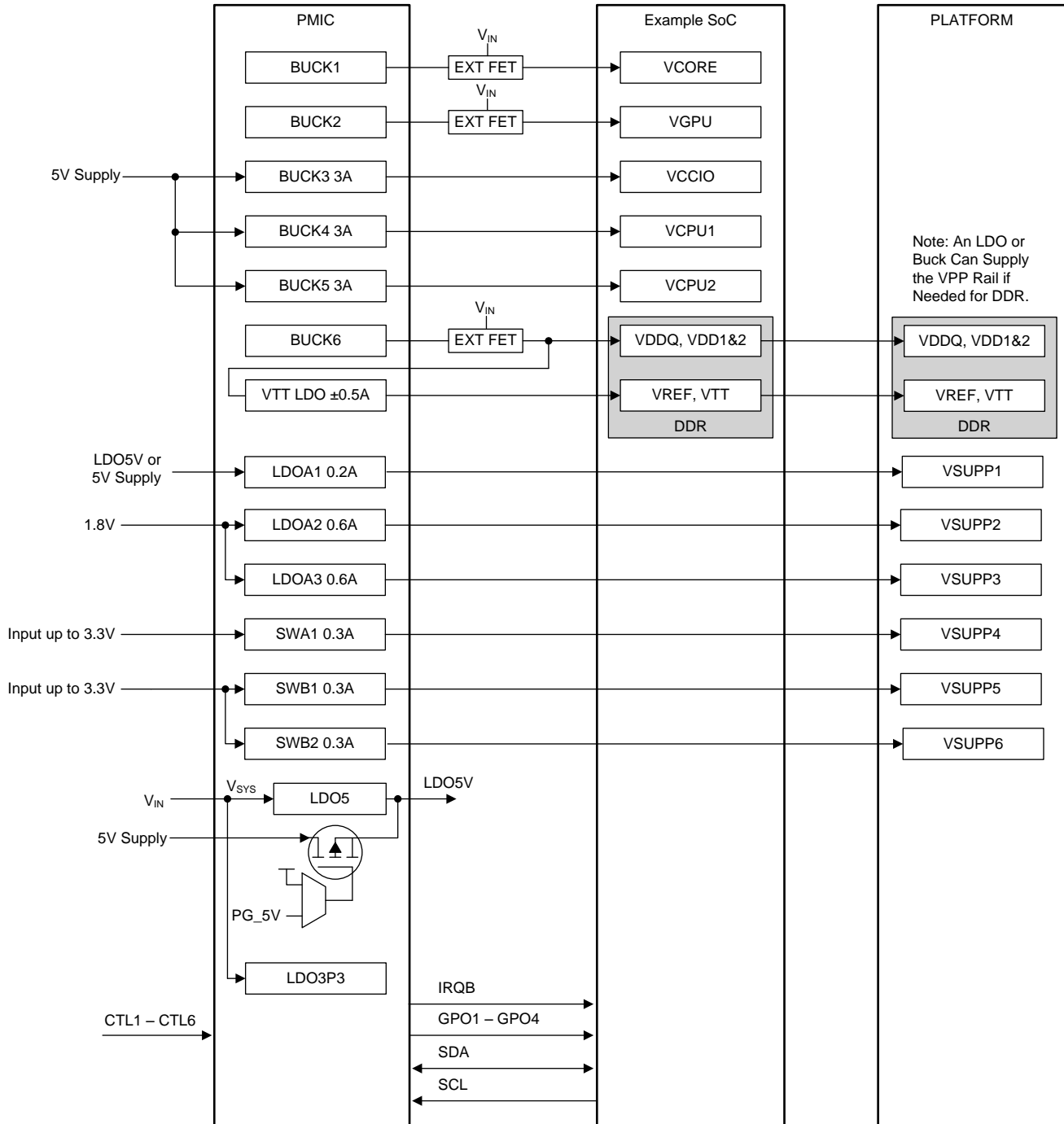
6.1 Application Information

For a detailed description about application usage, refer to the [TPS65086x Design Guide](#) and to the [TPS65086x Schematic and Layout Checklist](#).

6.2 Typical Application

6.2.1 Typical Application Example

This section describes the general application information and provides a more detailed description on the PMIC that powers a generic multicore-processor application. An example system block diagram for the device powering an SoC and the rest of platform is shown in [Figure 6-1](#). The functional block diagram in [Figure 5-1](#) outlines the typical external components necessary for proper device functionality.



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Figure 6-1. Typical Application Example

6.2.1.1 Design Requirements

The PMIC requires decoupling caps on the supply pins. Follow the values for recommended capacitance on these supplies given in [Section 4](#). The controllers, converter, LDOs, and some other features can be adjusted to meet specific application needs. [Section 6.2.1.2](#) describes how to design and adjust the external components to achieve desired performance.

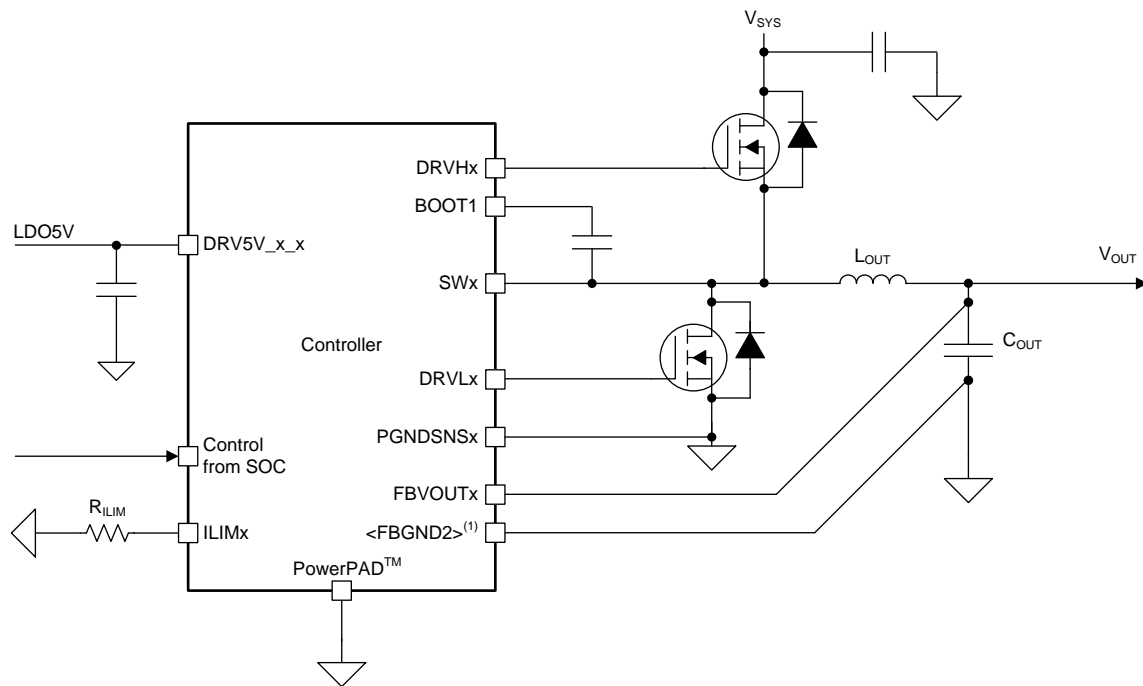
6.2.1.2 Detailed Design Procedure

6.2.1.2.1 Controller Design Procedure

Designing the controller can be broken down into the following steps:

1. Design the output filter
2. Select the FETs
3. Select the bootstrap capacitor
4. Select the input capacitors
5. Set the current limits

Controllers BUCK1, BUCK2, and BUCK6 require a 5-V supply and capacitors at their corresponding DRV5V_x_x pins. For most applications, the DRV5V_x_x input should come from the LDO5P0 pin to ensure uninterrupted supply voltage; a 2.2- μ F, X5R, 20%, 10-V, or similar capacitor must be used for decoupling.



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(1) <FBGND2> is only present for BUCK2.

Figure 6-2. Controller Diagram

6.2.1.2.1.1 Selecting the Inductor

Placement of an inductor is required between the external FETs and the output capacitors. Together, the inductor and output capacitors make the double-pole that contributes to stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases, the ripple current decreases, which typically results in an increased efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

Equation 5 shows the calculation for the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times I_{OUT(MAX)} \times K_{IND}}$$

where

- V_{OUT} is the typical output voltage
- V_{IN} is the typical input voltage
- f_{sw} is the typical switching frequency when loaded, 1 MHz unless otherwise noted
- $I_{OUT(MAX)}$ is the maximum load current
- K_{IND} is the ratio of $I_{L(ripple)}$ to the $I_{OUT(MAX)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4. Higher values have improved transient performance, lower values have improved efficiency

(5)

With the chosen inductance value, the peak current for the inductor in steady state operation, $I_{L(max)}$, can be calculated using Equation 6. The rated saturation current of the inductor must be higher than the $I_{L(max)}$ current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{sw} \times L}$$

(6)

6.2.1.2.1.2 Selecting the Output Capacitors

TI recommends using ceramic capacitors with low ESR values to provide the lowest output voltage ripple. The output capacitor requires an X7R or an X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the controller operates in PFM mode, and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

TI recommends the use of small ceramic capacitors placed between the inductor and load with many vias to the PGND plane for the output capacitors of the BUCK controllers. This solution typically provides the smallest and lowest cost solution available for D-CAP2 controllers.

The selection of the output capacitor is typically driven by the output transient response. Equation 7 and Equation 8 provide a rough estimate of the minimum required capacitance to ensure proper transient response. Because the transient response is significantly affected by the board layout, some experimentation is expected in order to confirm that values derived in this section are applicable to any particular use case. These are not meant to be an absolute requirement, but rather a rough starting point. Alternatively, some known combination values from which to begin are provided in Table 6-1. V_{UNDER} and V_{OVER} values should be greater than or equal to 3% of V_{OUT} setting in order for equations to be meaningful. The equations provide some margin so that actual capacitance requirement may be lower than calculated.

$$C_{OUT} > \frac{I_{TRAN(MAX)}^2 \times L}{(V_{IN} - V_{OUT}) \times V_{UNDER}}$$

where

- $I_{\text{TRAN(max)}}$ is the maximum load current step
- L is the chosen inductance
- V_{IN} is the maximum input voltage
- V_{OUT} is the minimum programmed output voltage
- V_{UNDER} is the maximum allowable undershoot from programmed voltage

$$C_{\text{OUT}} > \frac{I_{\text{TRAN(MAX)}}^2 \times L}{V_{\text{OUT}} \times V_{\text{OVER}}}$$

where

- V_{OVER} is the maximum allowable overshoot from programmed voltage

Another key performance factor can be the ripple voltage while in pulsed frequency modulation mode, also known as discontinuous conduction mode. At light load, the controller will disable the low side FET once it detects a zero-crossing event on the inductor current. It will stay disabled until V_{OUT} crosses below the set VID threshold. This architecture allows significant power savings at light load conditions by minimizing power loss through the low side FET and through switching. The disadvantage is that there is higher voltage ripple since the ripple current is only positive. Additionally, for even higher efficiency, $T_{\text{ON(PFM)}}$ for this device is typically 80% longer than $T_{\text{ON(PWM)}}$, which can be calculated by dividing the duty cycle by the switching frequency. An estimate for the required capacitance for a given allowable ripple voltage at light load is shown in [Equation 9](#). ESR of the output capacitor is neglected here because ceramic capacitors, which typically have low ESR, are recommended. V_{OVER} should not be set lower than 3% of V_{OUT} value.

$$C_{\text{OUT}} > \frac{T_{\text{ON_EXT}}^2 \times V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{2 \times V_{\text{IN}} \times f_{\text{SW}}^2 \times V_{\text{OVER}} \times L}$$

where

- $T_{\text{ON_EXT}}$ is the PFM on time extension constant, 1.8 unless otherwise noted in the part number specific section
- V_{OUT} is the maximum programmed output voltage
- V_{IN} is the maximum input voltage
- f_{SW} is the typical switching frequency when loaded, 1 MHz unless otherwise noted
- V_{OVER} is the maximum allowable overshoot from programmed voltage
- L is the chosen inductance

In cases where the transient current change is very low and ripple voltage allowance is large, the DC stability may become important. DCAP2 is a very stable architecture so this value is likely to be the smallest of those calculated. [Equation 10](#) approximates the amount of capacitance necessary to maintain DC stability. Again, this is provided as a starting point; actual values will vary on a board-to-board case.

$$C_{\text{OUT}} > \frac{V_{\text{OUT}} \times 50 \mu\text{s}}{V_{\text{IN}} \times f_{\text{SW}} \times L}$$

where

- V_{OUT} is the maximum programmed output voltage
- 50 μs is based on internal ramp setup
- V_{IN} is the minimum input voltage
- f_{SW} is the typical switching frequency
- L is the chosen inductance

Choosing the maximum value between [Equation 7](#), [Equation 8](#), [Equation 9](#), and [Equation 10](#) is recommended as a starting point to get the desired performance. All equations are estimates and have not been validated at all variable corners. Removing excess capacitance or adding extra capacitance may be necessary during board evaluation. Testing can typically be performed on the evaluation module or on prototype boards.

Table 6-1. Known LC Combinations for 1 μ s Load Rise and Fall Time

| $I_{\text{TRAN(max)}} (A)$ | $L (\mu H)$ | $V_{\text{OUT}} (V)$ | $V_{\text{UNDER}} (V)$ | $V_{\text{OVER}} (V)$ | $C_{\text{OUT}}(\mu F)$ |
|----------------------------|-------------|----------------------|------------------------|-----------------------|-------------------------|
| 3.5 | 0.47 | 1 | 0.05 | 0.05 | 110 |
| 4 | 0.47 | 1 | 0.05 | 0.05 | 220 |
| 5 | 0.47 | 1.35 | 0.068 | 0.068 | 220 |
| 8 | 0.33 | 1 | 0.05 | 0.06 | 440 |
| 20 | 0.22 | 1 | 0.05 | 0.16 | 550 |

6.2.1.2.1.3 Selecting the FETs

This controller is designed to drive two NMOS FETs. Typically, lower $R_{\text{DS(on)}}$ values are better for improving the overall efficiency of the controller, however higher gate charge thresholds will result in lower efficiency so the two need to be balanced for optimal performance. As the $R_{\text{DS(on)}}$ for the low-side FET decreases, the minimum current limit increases; therefore, ensure selection of the appropriate values for the FETs, inductor, output capacitors, and current limit resistor. TI's [CSD85301Q2](#), [CSD87331Q3D](#), [CSD87381P](#), [CSD87588N](#), and [CSD87350Q5D](#) devices are recommended for the controllers, depending on the required maximum current.

6.2.1.2.1.4 Bootstrap Capacitor

To ensure the internal high-side gate drivers are supplied with a stable low-noise supply voltage, a capacitor must be connected between the SWx pins and the respective BOOTx pins. TI recommends placing ceramic capacitors with the value of 0.1 μ F for the controllers. During testing, a 0.1- μ F, size 0402, 10-V capacitor is used for the controllers.

TI recommends reserving a small resistor in series with the bootstrap capacitor in case the turnon and turnoff of the FETs must be slowed to reduce voltage ringing on the switch node, which is a common practice for controller design.

6.2.1.2.1.5 Setting the Current Limit

The current-limiting resistor value must be chosen based on [Equation 1](#).

6.2.1.2.1.6 Selecting the Input Capacitors

Due to the nature of the switching controller with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and also for minimizing the interference with other circuits caused by high input-voltage spikes. For the controller, a typical 2.2- μ F capacitor can be used for the DRV5V_x_x pin to handle the transients on the driver. For the FET input, 10 μ F of input capacitance (after derating) is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

NOTE

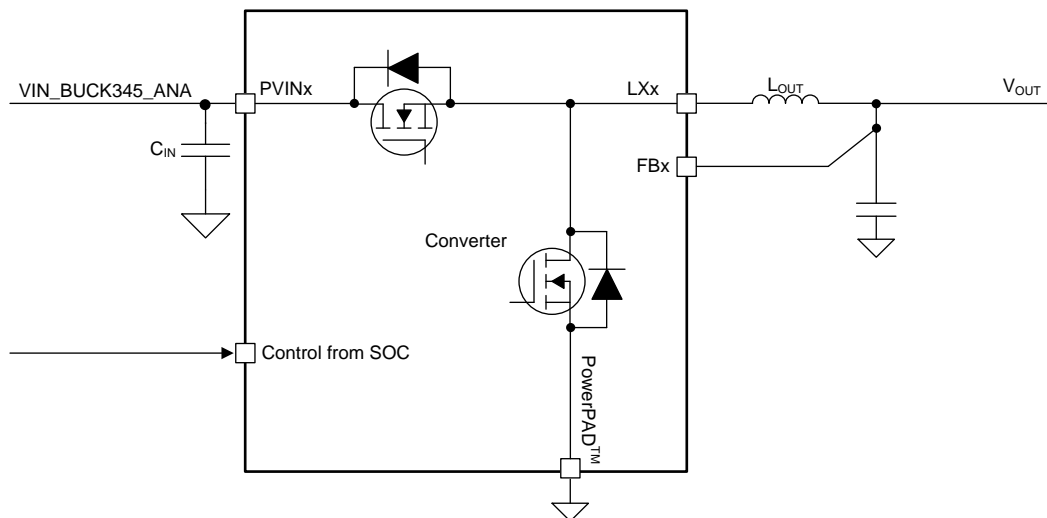
Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

TI recommends placing a ceramic capacitor as close as possible to the FET across the respective VSYS and PGND pins of the FETs. The preferred capacitors for the controllers are two Murata GRM21BR61E226ME44: 22- μ F, 0805, 25-V, $\pm 20\%$, or similar capacitors.

6.2.1.2.2 Converter Design Procedure

Designing the converter has only two steps: design the output filter and select the input capacitors.

[Figure 6-3](#) shows a diagram of the converter.



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Figure 6-3. Converter Diagram

6.2.1.2.2.1 Selecting the Inductor

Internal parameters for the converters are optimized for either a 0.47 μH or 1 μH inductor, however it is possible to use other inductor values as long as they are chosen carefully and thoroughly tested. The equations from [Section 6.2.1.2.1.1](#) can be utilized again with the parameters changed to match those of the converters. Switching frequency estimates can be found in [Section 4.15](#).

6.2.1.2.2.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values are recommended because they provide the lowest output voltage ripple. The output capacitor requires either an X7R or X5R rating. Y5V and Z5U capacitors, aside from the wide variation in capacitance over temperature, become resistive at high frequencies.

For the output capacitors of the BUCK converters, TI recommends placing small ceramic capacitors between the inductor and load with many vias to the PGND plane. This solution typically provides the smallest and lowest-cost solution available.

The minimum output capacitance recommended is 22 μF for stability. [Equation 7](#) and [Equation 8](#) can be used to estimate the required output capacitance for a given load transient. Note that V_{IN} will be different for the converters and that the switching frequency can be estimated using [Section 4.15](#). [Equation 9](#) can be neglected for converters as there is no on time extension and the $V_{\text{IN}} - V_{\text{OUT}}$ term is typically smaller.

6.2.1.2.2.3 Selecting the Input Capacitors

Due to the nature of the switching converter with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For the PVINx pin, 2.5 μF of input capacitance (after derating) is required for most applications. A ceramic capacitor is recommended to achieve the low ESR requirement. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. The input capacitor can be increased without any limit for better input-voltage filtering.

NOTE

Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

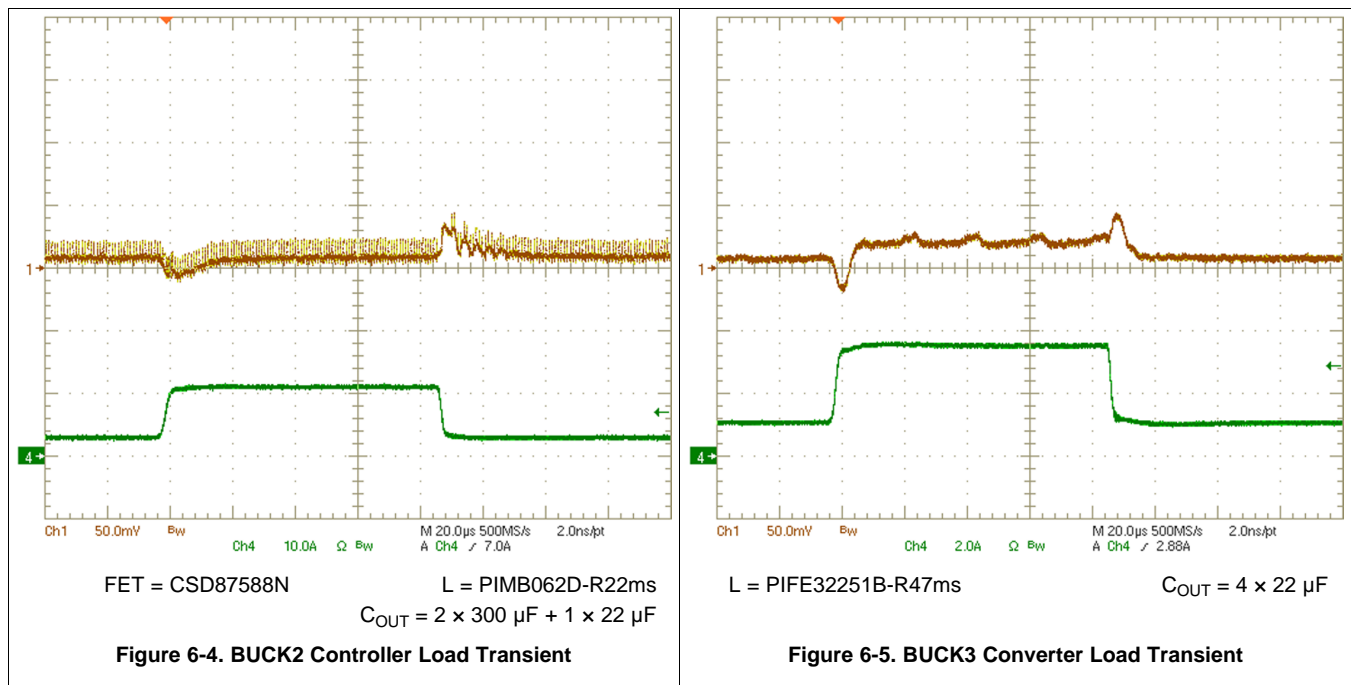
The preferred capacitor for the converters is one Samsung CL05A106MP5NUNC: 10- μF , 0402, 10-V, $\pm 20\%$, or similar capacitor.

6.2.1.2.3 LDO Design Procedure

The VTT LDO must handle the fast load transients from the DDR memory for termination. Therefore, it is recommended to use ceramic capacitors to maintain a high amount of capacitance with low ESR on the VTT LDO outputs and inputs. The preferred output capacitors for the VTT LDO are the GRM188R60J226MEA0 from Murata (22 μ F, 0603, 6.3 V, \pm 20%, or similar capacitors). The preferred input capacitor for the VTT LDO is the CL05A106MP5NUNC from Samsung (10- μ F, 0402, 10-V, \pm 20%, or similar capacitor).

The remaining LDOs must have input and output capacitors chosen based on the values in [Section 4.9](#).

6.2.1.3 Application Curves



6.2.1.4 Layout

6.2.1.4.1 Layout Guidelines

For a detailed description regarding layout recommendations, refer to the [TPS65086x Design Guide](#) and to the [TPS65086x Schematic and Layout Checklist](#). For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can have stability problems and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the device. Use a common-ground node for power ground and use a different, isolated node for control ground to minimize the effects of ground noise. Connect these ground nodes close to the AGND pin by one or two vias. Use of the design guide is highly encouraged in addition to the following list of other basic requirements:

- Do **not** allow the AGND, PGNDNSx, or FBGND2 to connect to the thermal pad on the top layer.
- To ensure proper sensing based on FET $R_{DS(ON)}$, PGNDNSx must not connect to PGND until very close to the PGND pin of the FET.
- All inductors, input and output capacitors, and FETs for the converters and controller must be on the same board layer as the IC.
- To achieve the best regulation performance, place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible.

- Bootstrap capacitors must be placed close to the device.
- The internal reference regulators must have their input and output capacitors placed close to the device pins.
- Route DRVHx and SWx as a differential pair. Ensure that there is a PGND path routed in parallel with DRVLx, which provides optimal driver loops.

6.2.1.4.2 Layout Example

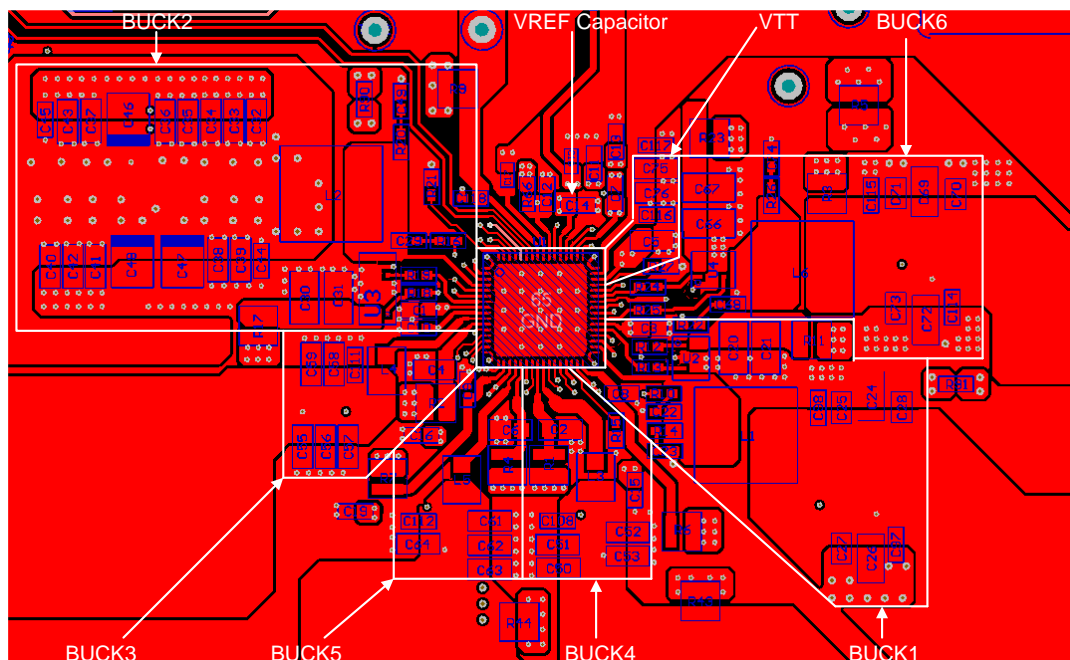
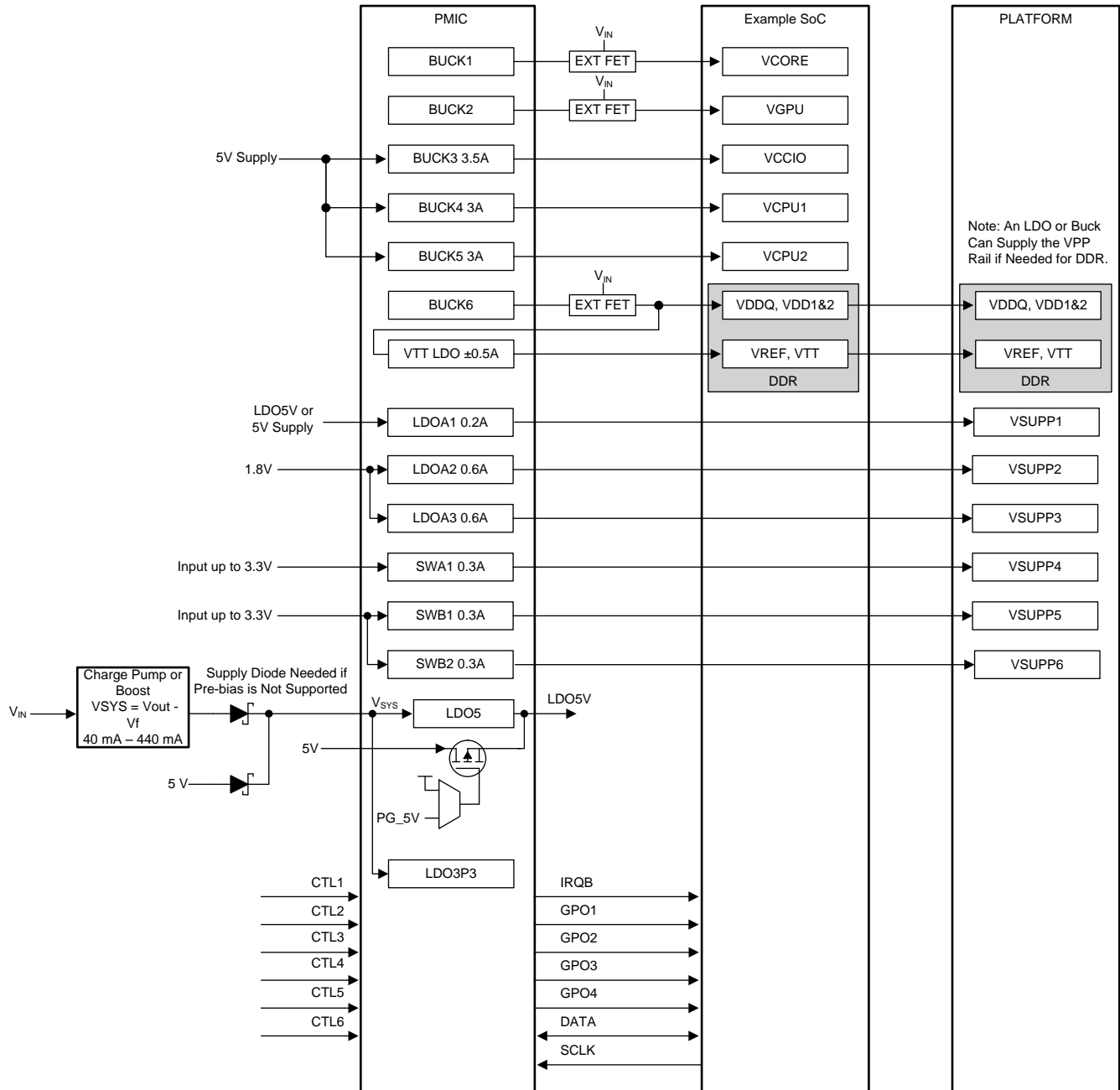


Figure 6-6. EVM Layout Example With All Components on the Top Layer

6.2.2 VIN 5-V Application

The PMIC can be operated by a 5-V input voltage to the system because the power path of the controller does not go through the device itself. The concept is simple: supply the controller VINs with the 5-V input, and supply the VSYS with a 5.8-V step-up of the 5 V with a boost or charge pump. The 5.8 V is recommended because the UVLO of the internal LDO5 is at 5.6 V and the device measures the voltage at VSYS and determines the optimum internal compensation and controller settings thus, it is ideal the VSYS be close to the VIN of the controllers.



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Figure 6-7. VIN 5-V Application

6.2.2.1 Design Requirements

The PMIC requires a step-up voltage from the 5-V input to 5.8 V for the VSYS supply. TI recommends keeping the VSYS near 5.8 V for optimization of the controllers.

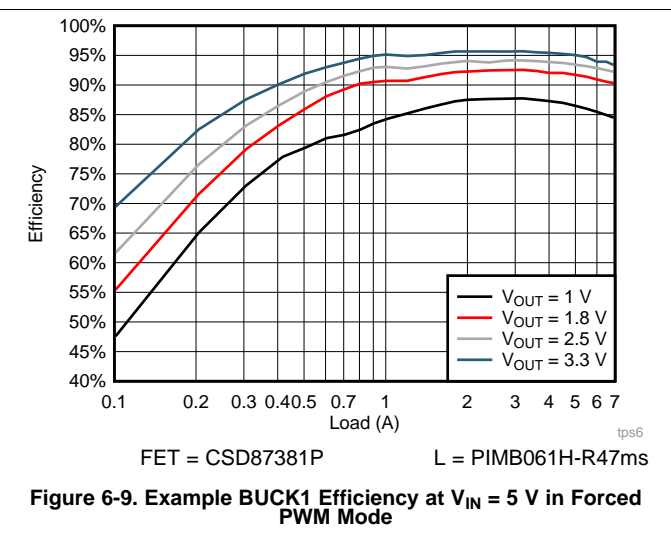
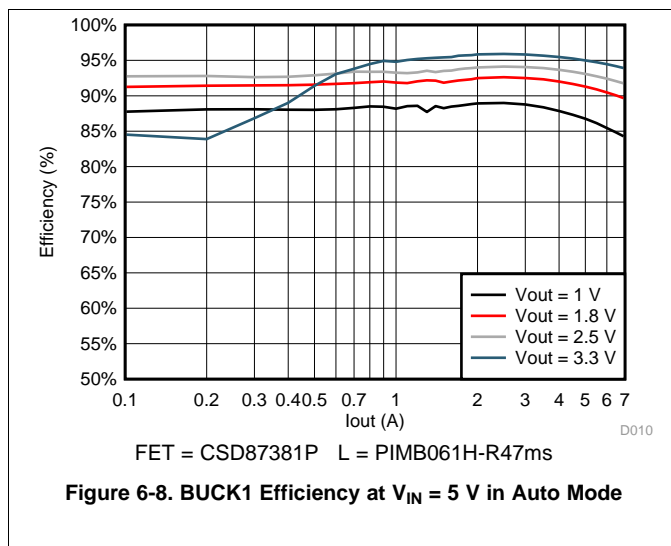
Depending on the application use cases, the supply current to the VSYS can require from 40 mA with the drivers being supplied by the 5-V input to 440 mA with the drivers being supplied by the LDO5 and the LDOA1 being operated at max loading. This means that a charge pump may be used in some applications like the 5-V input but in others, a small boost may be required.

A Schottky diode from the 5-V input to the VSYS is recommended to ensure the VSYS is biased and the internal reference LDOs are on before the step-up regulator is enabled or fully ramped up. If the step-up cannot tolerate pre-bias condition then, 2 diodes may be needed to prevent the initial 5-V supply biasing the output of the step-up.

6.2.2.2 Design Procedure

To design a 5-V input application, first provide a step-up voltage from the 5-V input to the VSYS. Design the step-up to output a voltage near 5.8 V. Next, route the 5-V input to the controller and converter VINs. Thus, all power paths (*all high currents*) are routed through the controllers or directly to the converters. None of the high currents are required from the step-up supply. After the input stage is complete, the rest of the system can be designed as normal following the typical application procedure, using 5 V as the input value to the controllers.

6.2.2.3 Application Curves



6.3 Power Supply Coupling and Bulk Capacitors

This device is designed to work with several different input voltages. The minimum voltage on the VSYS pin is 5.6 V for the device to start up; however, this is a low power rail. The input to the FETs must be from 4.5 V to 21 V as long as the proper BOM choices are made. Input to the converters should be between 3.3 V and 5 V. For the device to output maximum power, the input power must be sufficient. For the controllers, VIN must be able to supply sufficient input current for the output power of the application. For the converters, PVINx must be able to typically supply 2 A.

A best practice here is to determine power usage by the system and back-calculate the necessary power input based on expected efficiency values.

6.4 Do's and Don'ts

- Connect the LDO5V output to the DRV5V_x_x inputs for situations where an external 5-V supply is not initially available or is not available the entire time PMIC is on. If the external 5-V supply is always present, then DRV5V_x_x can be directly connected to remove the V5ANA-to-LDO5P0 load switch $R_{\text{DS(on)}}$.
- Ensure that none of the control pins are potentially floating.
- Include 0- Ω resistors on the DRVH or BOOT pins of controllers on prototype boards, which allows for slowing the controllers if the system is unable to handle the noise generated by the large switching or if switching voltage is too large due to layout.
- Do **not** connect the V5ANA power input to a different source other than PVINx. A mismatch here causes reference circuits to regulate incorrectly.
- Do **not** supply the V5ANA power input before the VSYS. Reference biasing of the internal FETs may turn on the HS FET passing the input to the output until VSYS is biased.
- Do **not** change the values of the reserved bits when writing I²C. This can have unexpected consequences. Expected values for each OTP are shown in the register map.

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

For documentation related to device development see the following:

- Texas Instruments, [TPS65086x Schematic and Layout Checklist](#)
- Texas Instruments, [TPS65086x Design Guide](#)

7.2 Documentation Support

7.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [CSD85301Q2 20 V Dual N-Channel NexFET™ Power MOSFETs data sheet](#)
- Texas Instruments, [CSD87331Q3D Synchronous Buck NexFET™ Power Block data sheet](#)
- Texas Instruments, [CSD87588N Synchronous Buck NexFET™ Power Block II data sheet](#)
- Texas Instruments, [CSD87381P Synchronous Buck NexFET™ Power Block II data sheet](#)
- Texas Instruments, [CSD87350Q5D Synchronous Buck NexFET™ Power Block data sheet](#)
- Texas Instruments, [MSP430G2121 Mixed Signal Microcontroller data sheet](#)
- Texas Instruments, [Power management integrated buck controllers for distant point-of-load applications white paper](#)
- Texas Instruments, [TPS65086x Evaluation Module user's guide](#)

7.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.5 Trademarks

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7.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



7.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| TPS65086100RSKR | ACTIVE | VQFN | RSK | 64 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T65086100 PG1.0 |  |
| TPS65086100RSKT | ACTIVE | VQFN | RSK | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T65086100 PG1.0 |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65086100RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086100RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086100RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086100RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |

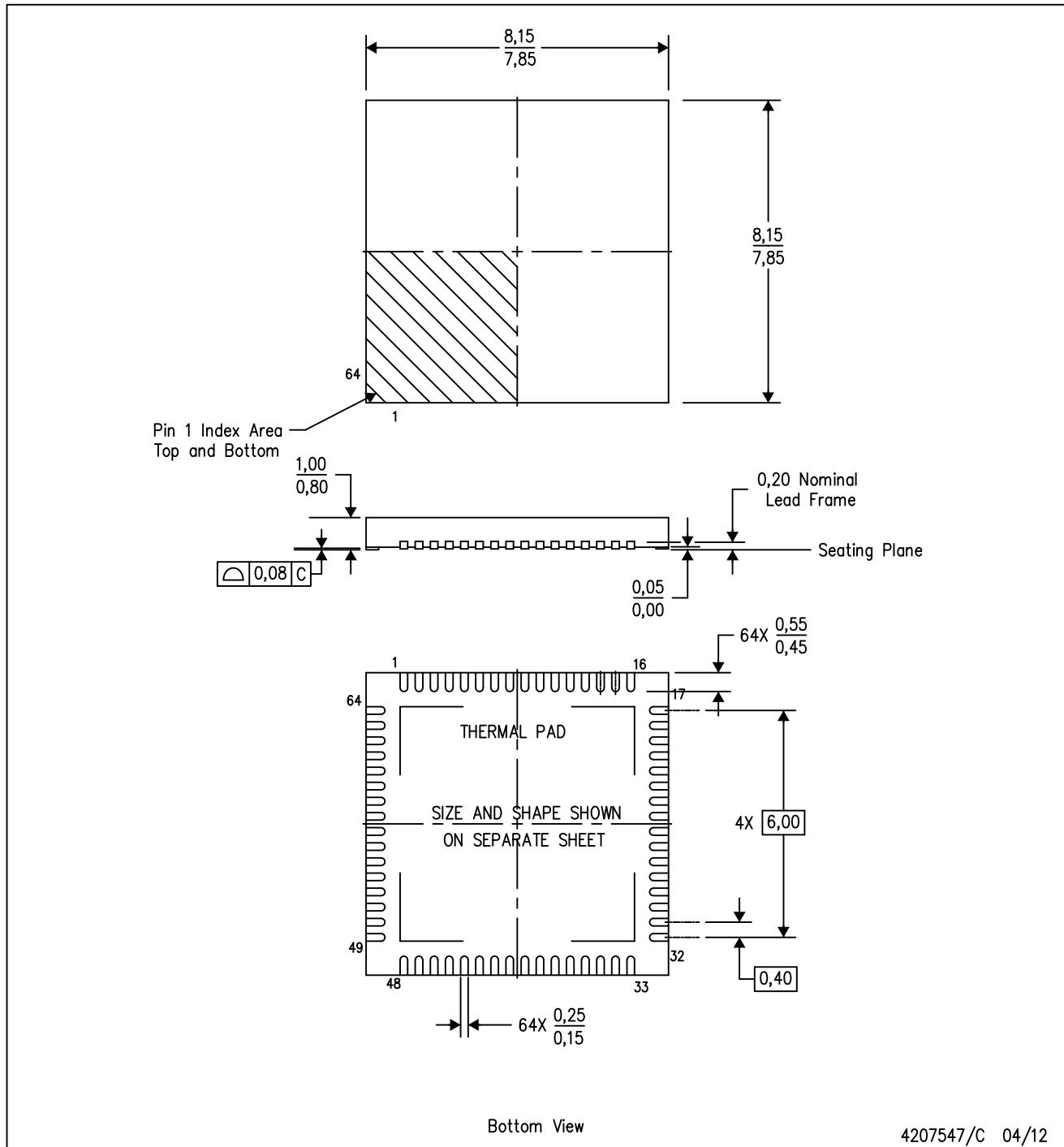
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65086100RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 35.0 |
| TPS65086100RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS65086100RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65086100RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |

RSK (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RSK (S-PVQFN-N64)

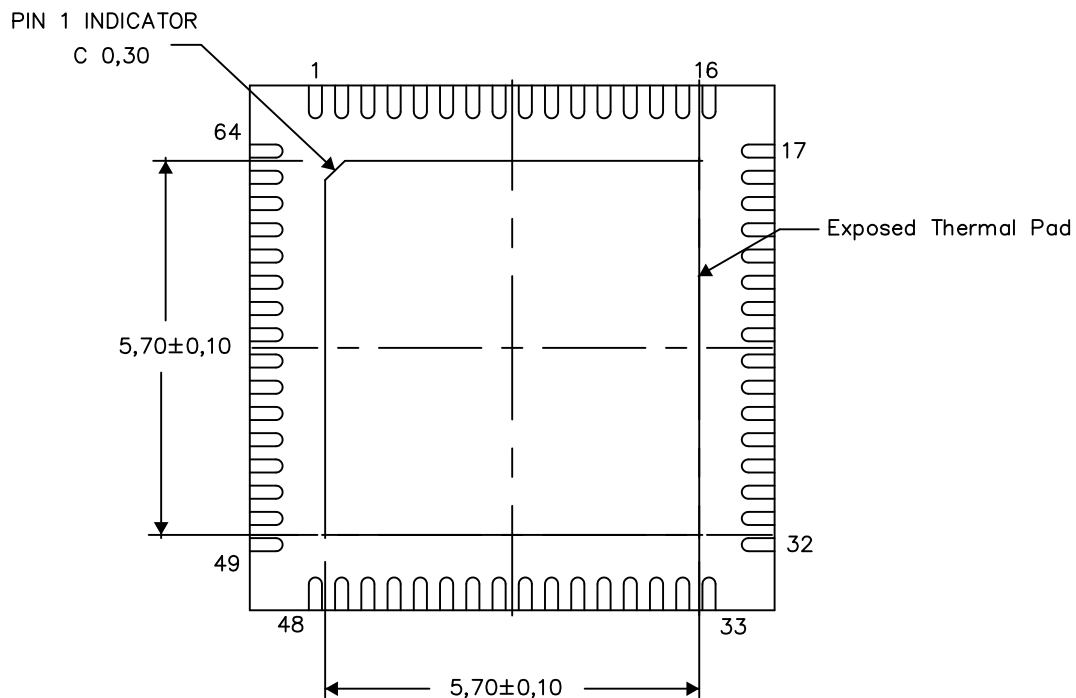
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

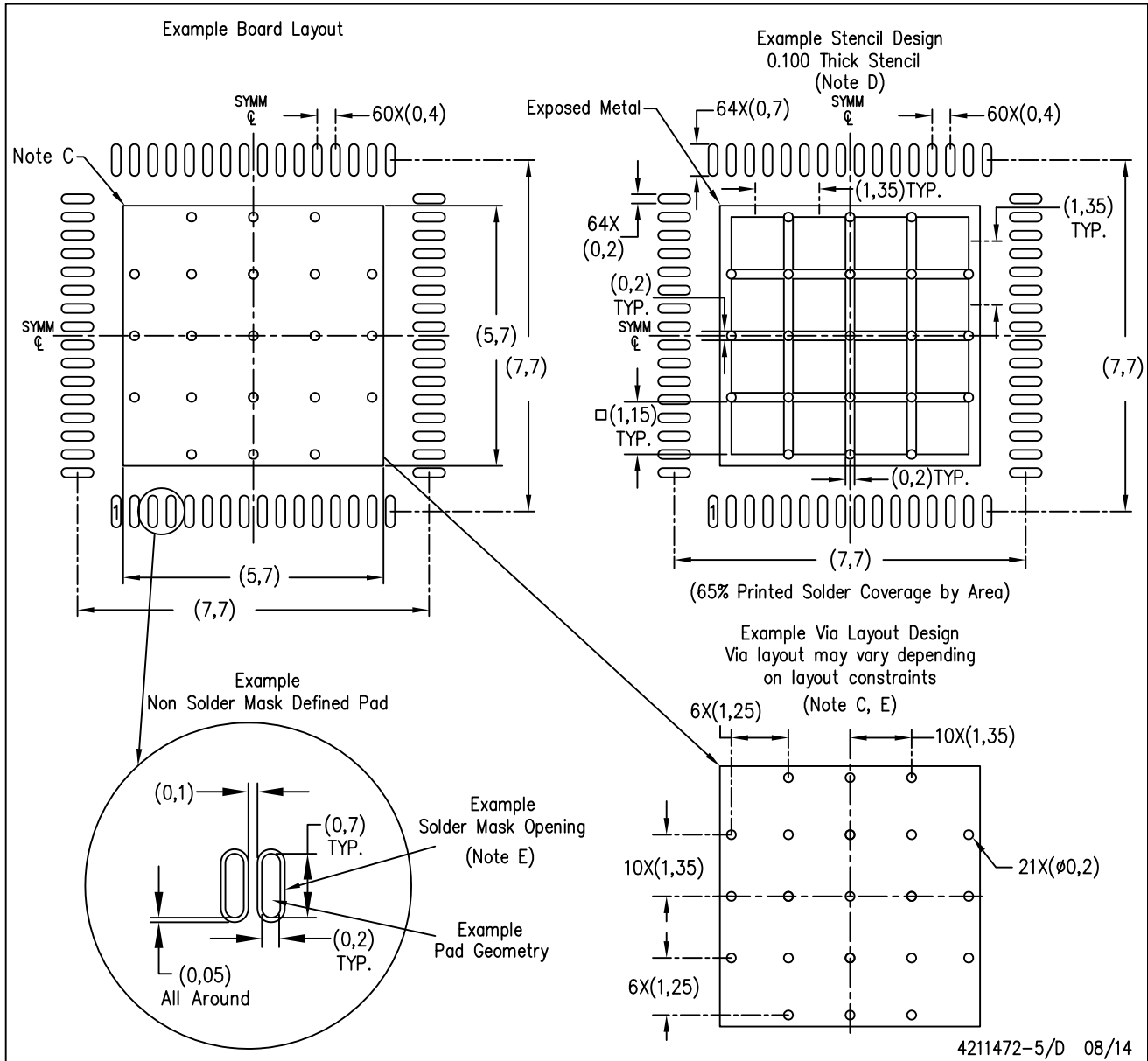
Exposed Thermal Pad Dimensions

4208001-5/H 08/14

NOTE: A. All linear dimensions are in millimeters

RSK (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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