Ultralow-Noise, High-PSRR, Fast, RF, 1-A LOW-DROPOUT LINEAR REGULATORS

Check for Samples: TPS796xx-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3A**
- **1-A Low-Dropout Regulator With Enable**
- **Available in Fixed and Adjustable (1.2 V to 5.5 V) Versions**
- **High PSRR (53 dB at 10 kHz)**
- **Ultralow-Noise (40 μV_{RMS}, TPS79630-Q1)**
- **Fast Start-Up Time (50 µs)**
- **Stable With a 1-µF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Very Low Dropout Voltage (250 mV at Full Load, TPS79630-Q1)**
- **SOT223-6 Package**

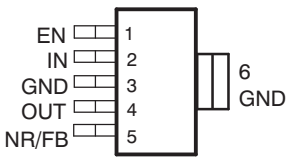
APPLICATIONS

- **RF: VCOs, Receivers, ADCs**
- **Audio**
- **Bluetooth™, Wireless LAN**

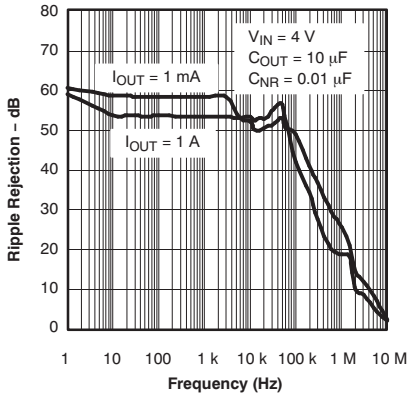
DESCRIPTION

The TPS796xx-Q1 family of low-dropout (LDO), low-power, linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in a small-outline SOT223-6 package. Each device in the family is stable with a small 1-µF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 250 mV at 1 A). Each device achieves fast start-up times (approximately 50 µs with a 0.001-µF bypass capacitor) while consuming very low quiescent current (265 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79630-Q1 exhibits approximately 40 μV_{RMS} of output voltage noise at 3-V output, with a 0.1-µF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high-PSRR, low-noise features and the fast response time.

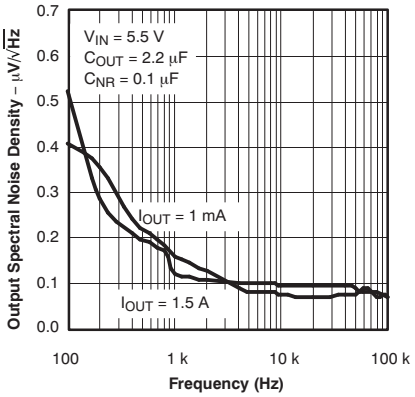
DQC PACKAGE
SOT223-6
(TOP VIEW)



TPS79630-Q1
RIPPLE REJECTION
vs
FREQUENCY



TPS79630-Q1
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	SPECIFIED TEMPERATURE RANGE, T_A	PACKAGE TYPE, PACKAGE DESIGNATOR(2)	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS79633-Q1	–40°C to +125°C	SOT223-6, DCQ	79633Q	TPS79633QDCQRQ1	Reel, 2500
TPS79630-Q1	–40°C to 125°C	SOT223-6, DCQ	PREVIEW	TPS79630QDCQRQ1	Reel, 2500
TPS79625-Q1	–40°C to 125°C	SOT223-6, DCQ	PREVIEW	TPS79625QDCQRQ1	Reel, 2500
TPS79628-Q1	–40°C to 125°C	SOT223-6, DCQ	PREVIEW	TPS79628QDCQRQ1	Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

		UNIT
V_{IN} range		–0.3 V to 6 V
V_{EN} range		–0.3 V to V_{IN} + 0.3 V
V_{OUT} range		6 V
Peak output current		Internally limited
Continuous total power dissipation		See *Thermal Information* table
ESD ratings	Human Body Model (HBM) AEC-Q100 Classification Level H2	2 kV
	Charged Device Model (CDM) AEC-Q100 Classification Level C3A	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

	MIN	NOM	MAX	UNIT
Ambient temperature, T_A	–40°		125	°C

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS796xx-Q1 DCQ 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	70.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	70	°C/W
θ_{JB}	Junction-to-board thermal resistance	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W°
ψ_{JB}	Junction-to-board characterization parameter	30.1	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range (T_A = –40°C to 125°C), $V_{EN} = V_{IN,}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1 mA, C_{OUT} = 10 µF, and C_{NR} = 0.01 µF, unless otherwise noted. Typical values are at +25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} Input voltage(1)					2.7		5.5	V
I_{OUT} Continuous output current					0		1	A
Output voltage	Accuracy	Fixed V_{OUT} < 5 V	0 µA ≤ I_{OUT} ≤ 1 A, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–2.0		+2.0	%
Output voltage line regulation ($\Delta V_{OUT}\%/V_{IN}$)(1)			V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V			0.05	0.12	%/V
Load regulation ($\Delta V_{OUT}\%/\Delta I_{OUT}$)			0 µA ≤ I_{OUT} ≤ 1 A			5		mV
Dropout voltage(2) (V_{IN} = $V_{OUT\ (nom)}$ – 0.1 V)		TPS79628-Q1	I_{OUT} = 1 A			270	365	mV
		TPS79630-Q1	I_{OUT} = 1 A			250	345	mV
		TPS79633-Q1	I_{OUT} = 1 A			220	325	mV
Output current limit			V_{OUT} = 0 V		2.4		4.2	A
Ground pin current			0 µA ≤ I_{OUT} ≤ 1 A			265	385	µA
Shutdown current(3)			V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V			0.07	1	µA
FB pin current			V_{FB} = 1.225 V				1	µA
Power-supply ripple rejection		TPS79630-Q1	f = 100 Hz, I_{OUT} = 10 mA			59		dB
			f = 100 Hz, I_{OUT} = 1 A			54		dB
			f = 10 Hz, I_{OUT} = 1 A			53		dB
			f = 100 Hz, I_{OUT} = 1 A			42		dB
Output noise voltage (TPS79630-Q1)			BW = 100 Hz to 100 kHz, I_{OUT} = 1 A	C_{NR} = 0.001 µF		54		μV_{RMS}
				C_{NR} = 0.0047 µF		46		μV_{RMS}
				C_{NR} = 0.01 µF		41		μV_{RMS}
				C_{NR} = 0.1 µF		40		μV_{RMS}
Time, start-up (TPS79630-Q1)			R_L = 3 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
				C_{NR} = 0.0047 µF		75		µs
				C_{NR} = 0.01 µF		110		µs
EN pin current			V_{EN} = 0 V		–1		1	µA
UVLO threshold			V_{CC} rising		2.25		2.65	V
UVLO hysteresis						100		mV
High-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		1.7		V_{IN}	V
Low-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		0		0.7	V

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater. TPS79650-Q1 is tested at V_{IN} = 5.5 V.
(2) V_{DO} is not measured for TPS79625-Q1 because minimum V_{IN} = 2.7 V.
(3) For adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

FUNCTIONAL BLOCK DIAGRAM

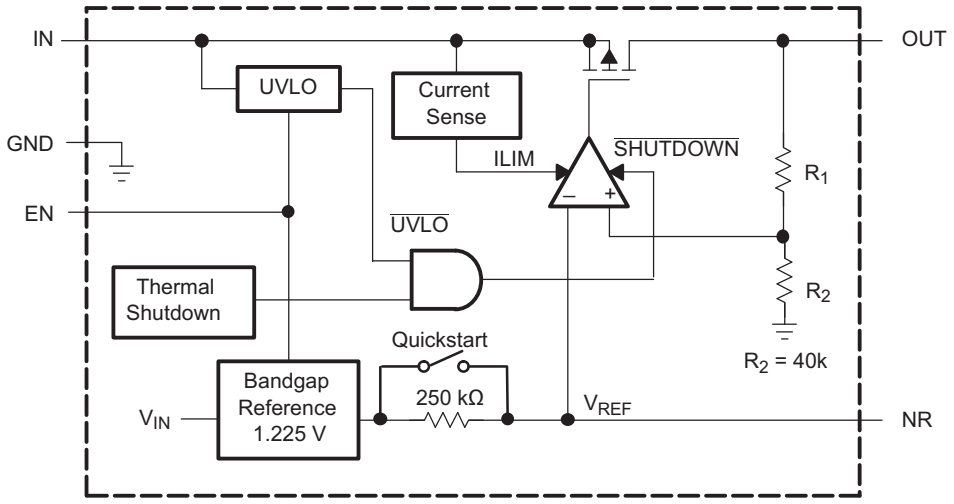


Table 1. Terminal Functions

TERMINAL		DESCRIPTION
NAME	SOT223 (DCQ)	
NR	5	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This improves power-supply rejection and reduces output noise.
FB	5	This terminal is the feedback input voltage for the adjustable device.
EN	1	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
GND	3, Tab	Regulator ground
IN	2	Unregulated input to the device.
OUT	4	Output of the regulator.

TYPICAL CHARACTERISTICS

TPS79630-Q1
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

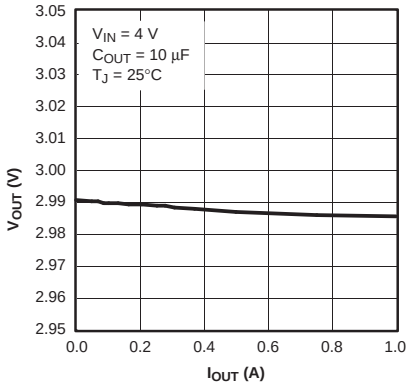


Figure 1.

TPS79628-Q1
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

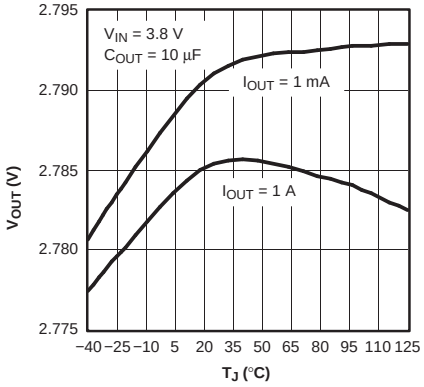


Figure 2.

TPS79628-Q1
GROUND CURRENT
vs
JUNCTION TEMPERATURE

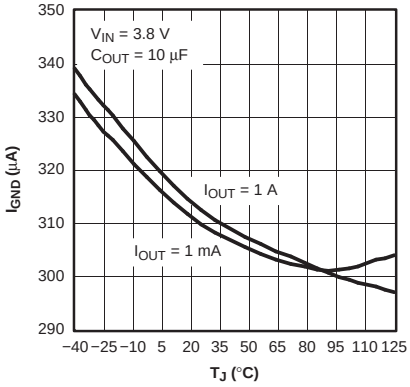


Figure 3.

TPS79630-Q1
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

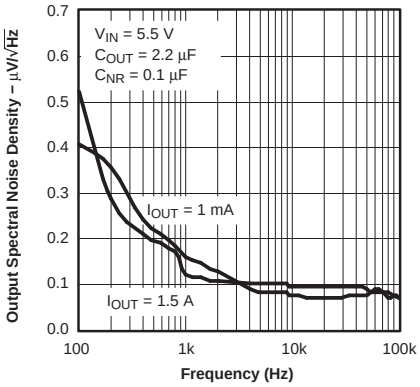


Figure 4.

TPS79630-Q1
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

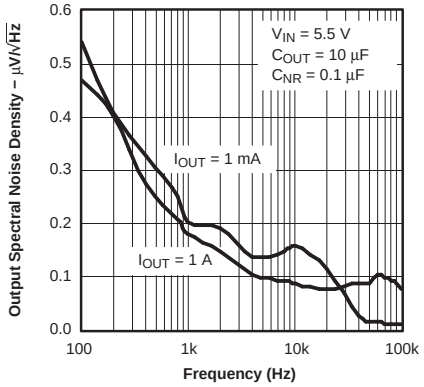


Figure 5.

TPS79630-Q1
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

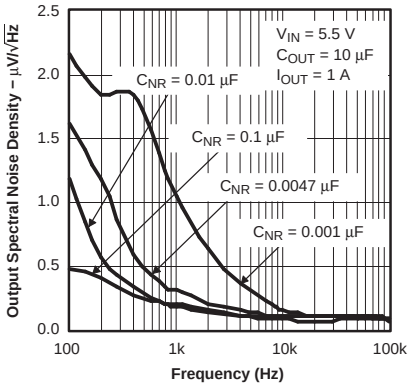


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TPS79630-Q1
ROOT MEAN SQUARED OUTPUT NOISE
vs
BYPASS CAPACITANCE

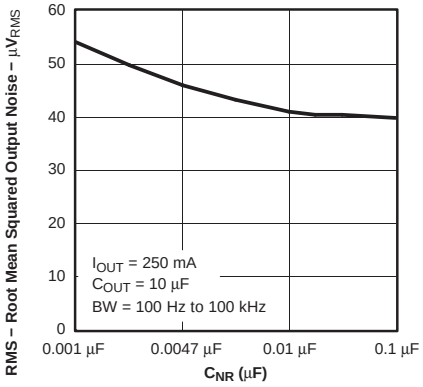


Figure 7.

TPS79628-Q1
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

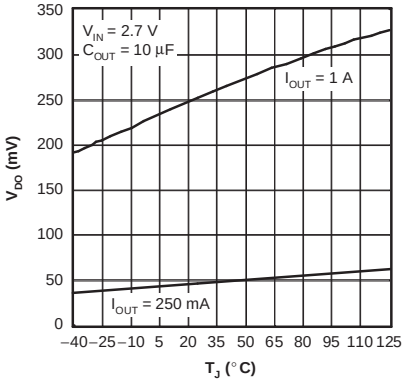


Figure 8.

TPS79630-Q1
RIPPLE REJECTION
vs
FREQUENCY

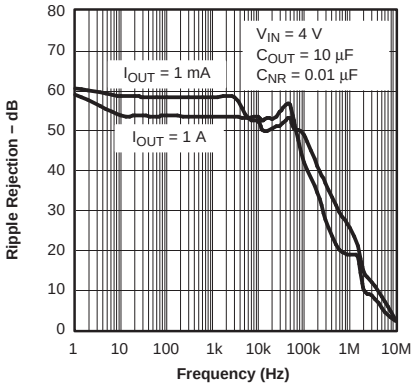


Figure 9.

TPS79630-Q1
RIPPLE REJECTION
vs
FREQUENCY

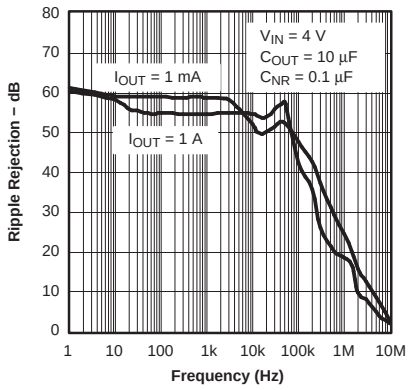


Figure 10.

TPS79630-Q1
RIPPLE REJECTION
vs
FREQUENCY

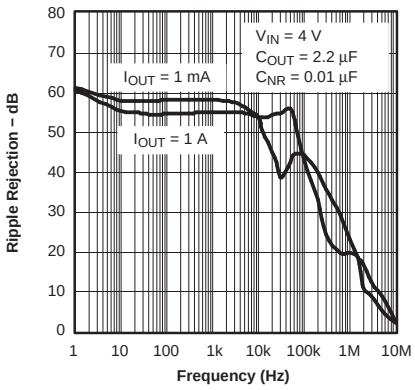


Figure 11.

START-UP TIME

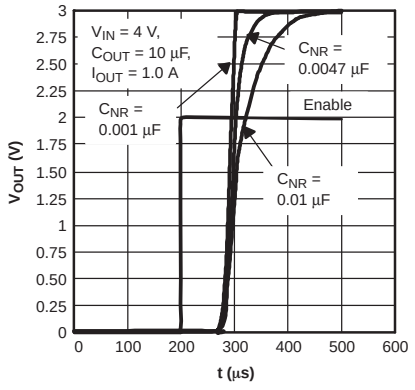


Figure 12.

TPS79618-Q1
LINE TRANSIENT RESPONSE

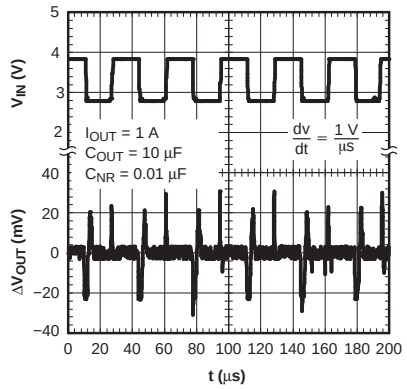


Figure 13.

TPS79630-Q1
LINE TRANSIENT RESPONSE

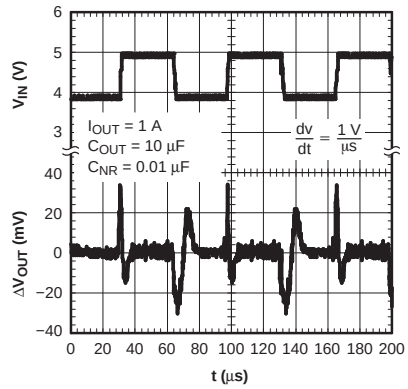


Figure 14.

TPS79628-Q1
LOAD TRANSIENT RESPONSE

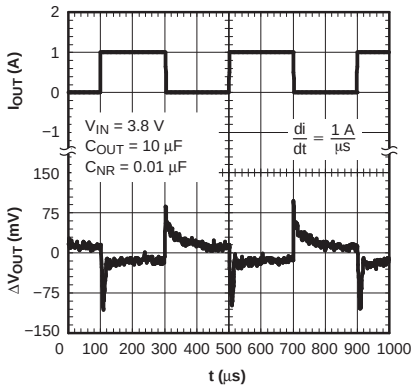


Figure 15.

TYPICAL CHARACTERISTICS (continued)

TPS79625-Q1

POWER UP/POWER DOWN

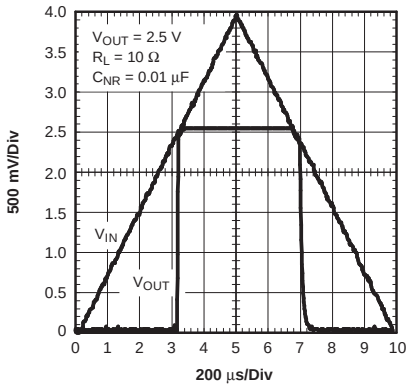


Figure 16.

TPS79630-Q1
DROPOUT VOLTAGE
vs
OUTPUT CURRENT

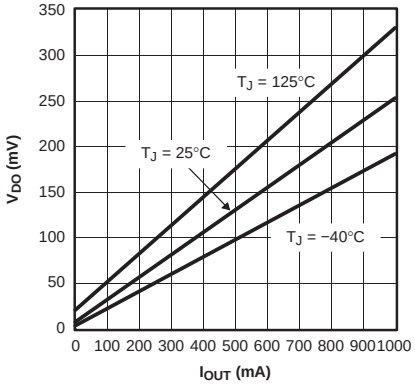


Figure 17.

TPS79630-Q1
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

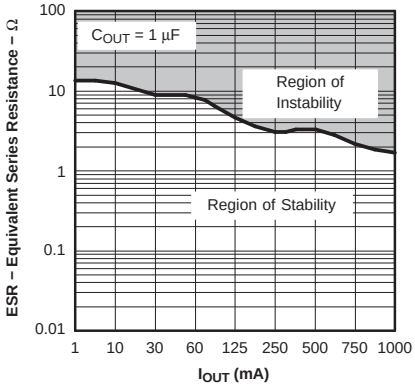


Figure 18.

TPS79630-Q1
TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

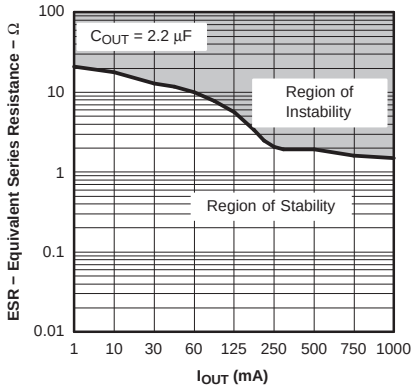


Figure 19.

TPS79630-Q1
TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

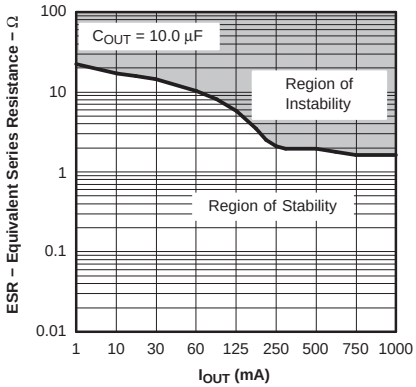


Figure 20.

APPLICATION INFORMATION

The TPS796xx-Q1 family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 µA typically), and enable input to reduce supply currents to less than 1 µA when the regulator is turned off.

A typical application circuit is shown in Figure 21.

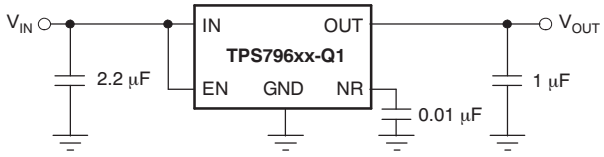


Figure 21. Typical Application Circuit

External Capacitor Requirements

Although not required, it is good analog design practice to place a 0.1-µF to 2.2-µF capacitor near the input of the regulator to counteract reactive input sources. A 2.2-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS796xx-Q1, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

As with most LDO regulators, the TPS796xx-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 µF. Any 1-µF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS796xx-Q1 has an NR pin that is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 µF in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the Functional Block Diagram.

For example, the TPS79630-Q1 exhibits 40 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 10-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

Regulator Mounting

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to the printed circuit board (PCB) copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in an application bulletin *Solder Pad Recommendations for Surface-Mount Devices*, literature number AB-132, available for download from the TI web site (www.ti.com).

Regulator Protection

The TPS796xx-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS796xx-Q1 features internal current limiting and thermal protection. During normal operation, the TPS796xx-Q1 limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately +165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately +140°C, regulator operation resumes.

THERMAL INFORMATION

POWER DISSIPATION

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 1:

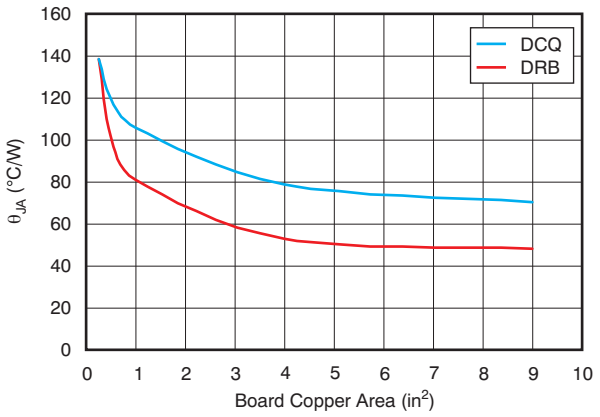
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SON (DRB) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the SOT-223 (DCQ) package, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 2:

$$R_{\theta JA} = \frac{(+125^{o}C - T_A)}{P_D} \quad (2)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 22.



Note: θ_{JA} value at board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

Figure 22. θ_{JA} vs Board Size

Figure 22 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE: When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 3). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{3}$$

Where P_D is the power dissipation shown by Equation 2, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (as Figure 24 shows).

NOTE: Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 23, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 3 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

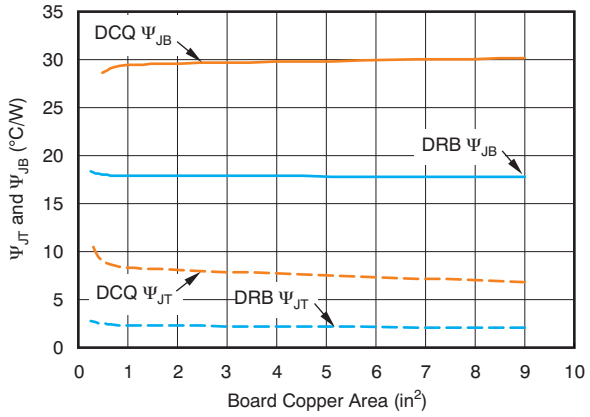
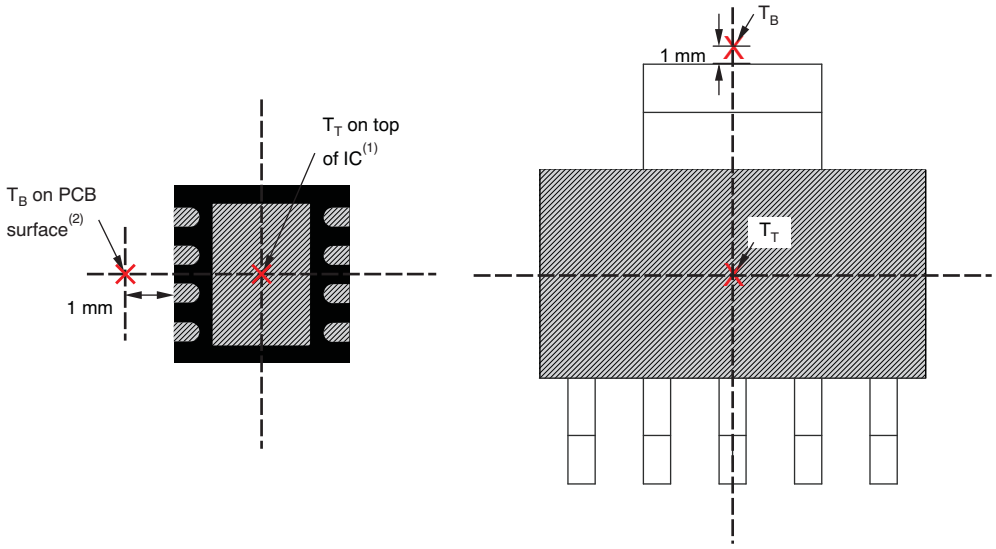


Figure 23. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.



(a) Example DRB (SON) Package Measurement **(b) Example DCQ (SOT-223) Package Measurement**

(1) T_T is measured at the center of both the X- and Y-dimensional axes.

(2) T_B is measured ***below*** the package lead on the PCB surface.

Figure 24. Measuring Points for T_T and T_B

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79633QDCQRQ1	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	79633Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

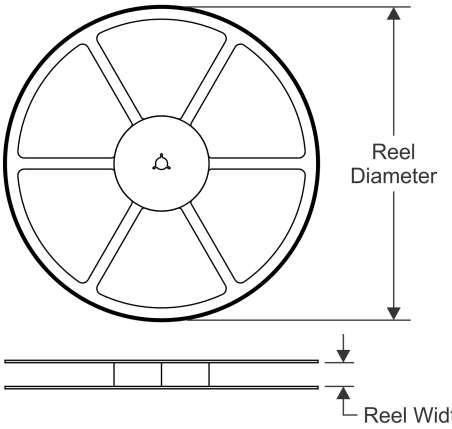
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

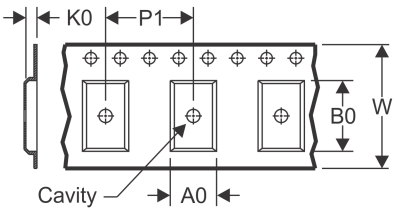
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

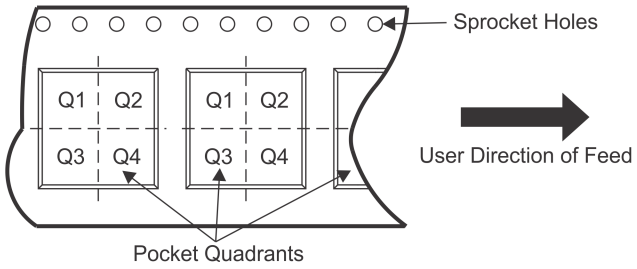


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

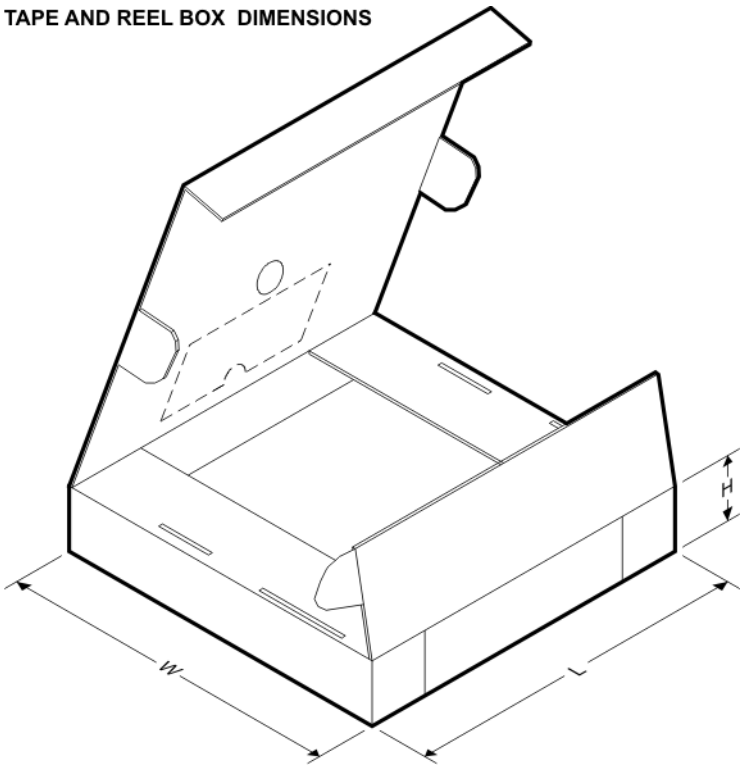
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79633QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

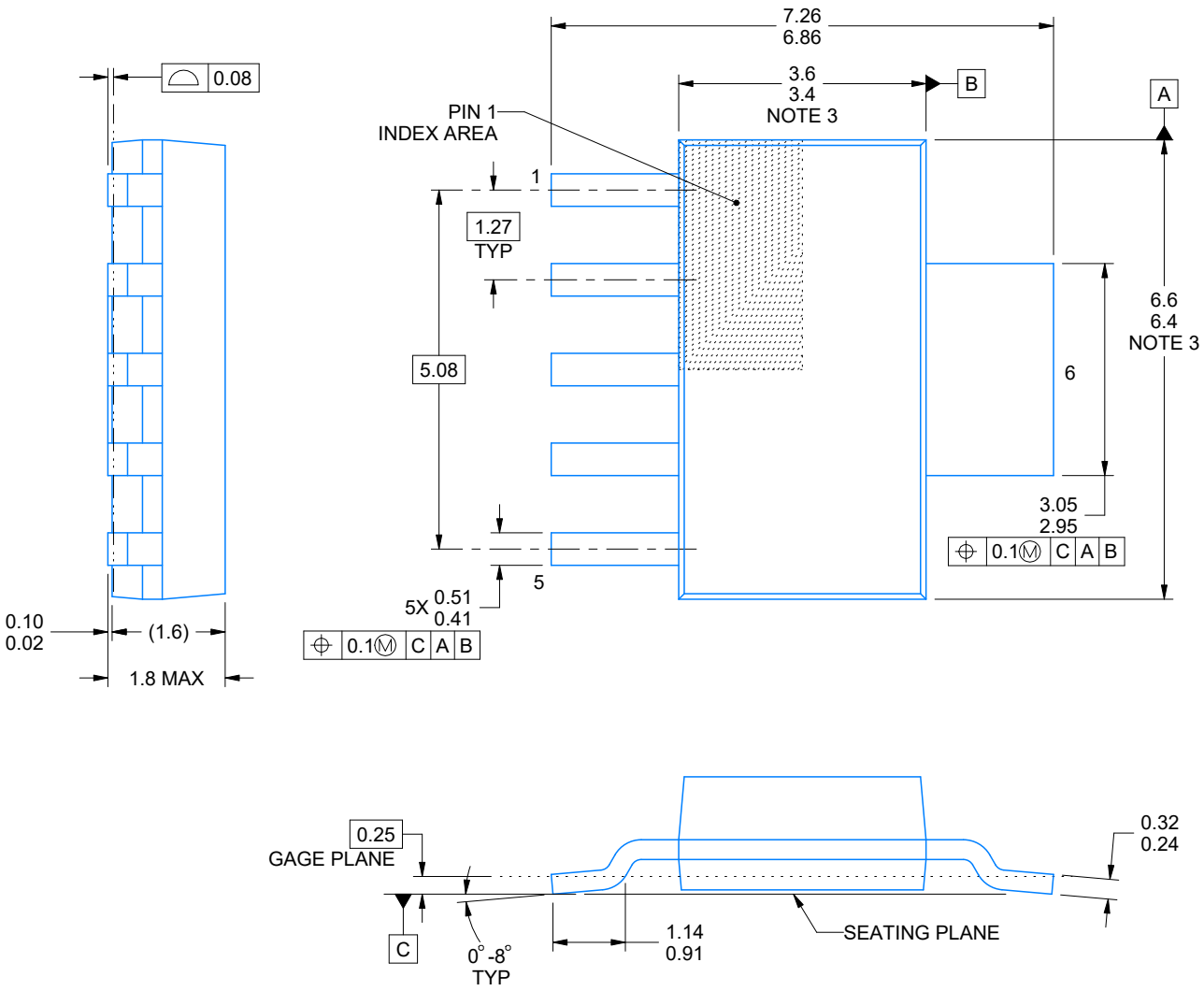
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79633QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



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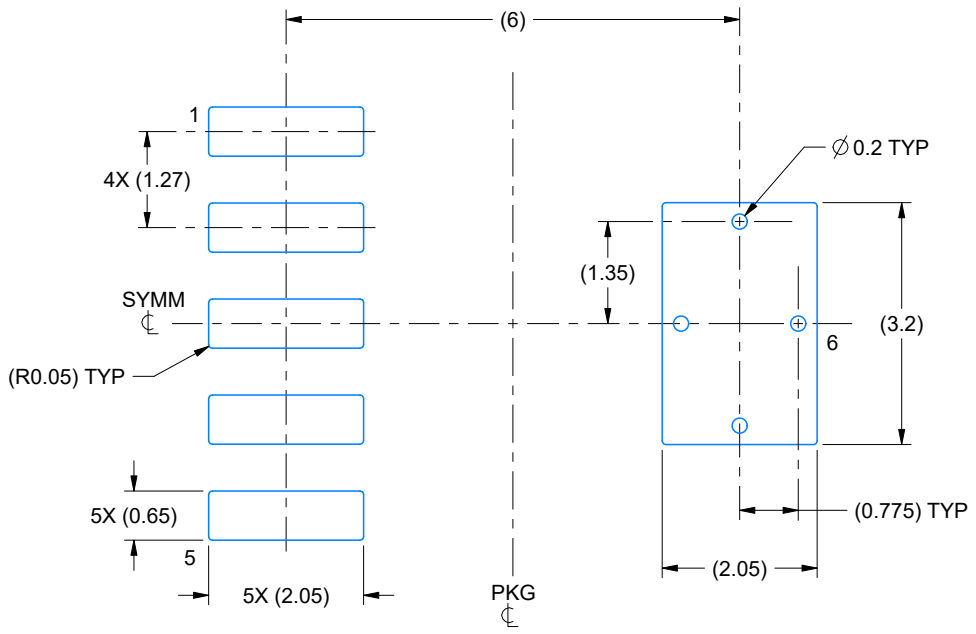
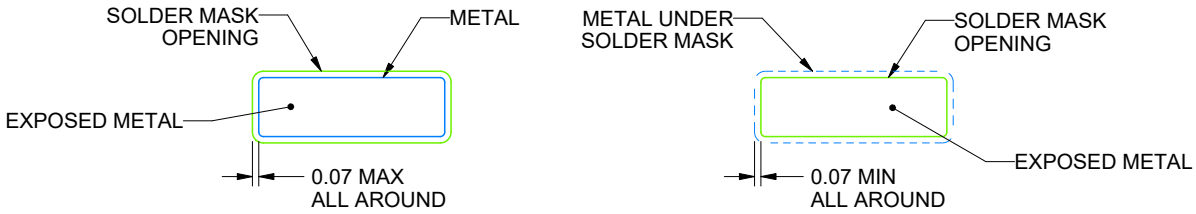
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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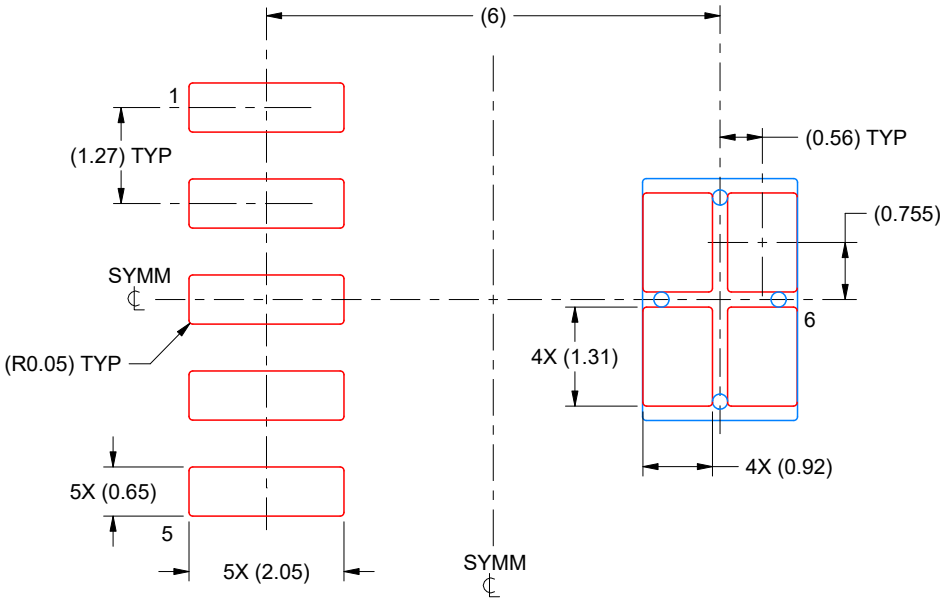
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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