TPS7B4255-Q1
Automotive, 70-mA, 40-V, Voltage-Tracking LDO With 5-mV Tracking Tolerance

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Wide input voltage range (–40 V to +40 V):
  - Absolute maximum input range: –40 V to +45 V
- Wide output voltage range: 2 V to 40 V
- Very-tight, output-tracking tolerance: 5 mV (max)
- Low dropout voltage: 500 mV (max) at 70 mA
- Reverse polarity protection
- Reverse current protection (short to battery)
- Combined reference and enable input
- Low quiescent current at light load: 35 µA
- Extreme, wide ESR range:
  - Stable with 1-µF to 200-µF ceramic output capacitor, 1-mΩ to 3-Ω ESR
- Overtemperature protection
- Output short-circuit proof to ground and supply
- Packages: 5-pin, SOT-23 DBV and DYB

2 Applications

- Powertrain pressure sensors
- Powertrain temperature sensors
- Powertrain exhaust sensors
- Powertrain fluid concentration sensors
- Body control modules (BCM)

3 Description

The TPS7B4255-Q1 is a low-dropout (LDO) voltage-tracking regulator, with high tracking accuracy and excellent load and line transient response. The device is available in two 5-pin, SOT-23 packages (DBV and DYB). The TPS7B4255-Q1 is designed to supply off-board sensors in automotive applications such as powertrain systems. The device provides integrated protection features such as reverse polarity, output short to battery and ground, and current limit and thermal shutdown to protect against the high risk of cable failures in an off-board power system. The device is designed to maintain a 45-V (absolute maximum) input voltage to sustain the load dump transient conditions.

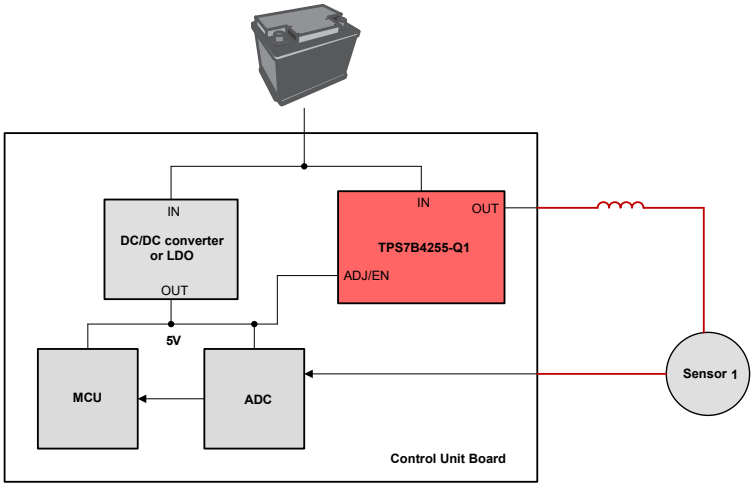
A reference voltage applied at the ADJ/EN pin effectively buffers the voltage with high accuracy for loads up to 70 mA. The high tracking accuracy provides accurate power supply to the off-board modules and enables better accuracy when measuring ratiometric sensors.

By setting the ADJ/EN input pin low, the TPS7B4255-Q1 switches to standby mode and reduces the quiescent current to the minimum value.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7B4255-Q1	SOT-23 (5), DBV	2.90 mm × 1.60 mm
	SOT-23 (5), DYB	2.93 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2022	*	Initial release.

5 Pin Configuration and Functions

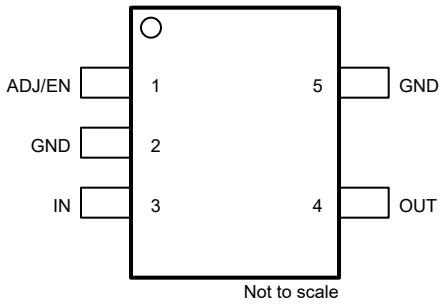

Figure 5-1. DBV Package, 5-Pin SOT-23 (Top View)

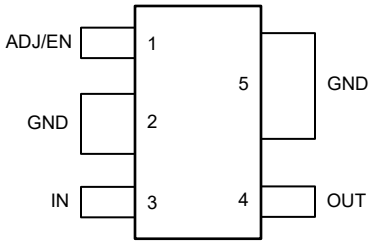

Figure 5-2. DYB Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADJ/EN	1	I	ADJ/EN PIN. Connect the reference to this pin. This pin connects to the reference voltage. A low signal below V_{IL} disables the device and a high signal above V_{IH} enables the device. Connect the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, place a capacitor close to this pin.
GND	2	G	Ground pin. This pin is internally connected to pin 5 on the DYB package.
GND	5	G	Ground pin. On the DYB package, this pin is internally connected to pin 2. On the DBV package this pin is not internally connected, but connecting this pin to GND is recommended.
IN	3	I	Input power-supply voltage pin. This pin is the device supply. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible to compensate for line influences.
OUT	4	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND; see the *Recommended Operating Conditions* table. Place the output capacitor as close to output of the device as possible.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	-40	45	V
V_{OUT}	Regulated output voltage	–5	45	V
ADJ	Adjustable Input	-0.3	45	V
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Unregulated input voltage	3		40	V
V_{OUT}	Regulated output voltage	2		40	V
I_{OUT}	Output current	0		70	mA
C_{OUT}	Output capacitor(2)	1		200	µF
ESR	Output capacitor ESR requirements	0.001		3	Ω
C_{IN}	Input capacitor(1)	0	1		µF
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance is 500 nF.
(2) Effective output capacitance of 500 nF minimum required for stability.

Thermal Information

THERMAL METRIC(1)		TPS7B4255-Q1		UNIT
		DBV (SOT-23)	DYB (SCT595)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.3	127.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.6	59.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	16.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.9	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.1	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 1 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{ADJ} = 5 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + 600 mV to 40 V, I_{OUT} = 100 µA to 70 mA	–5		5	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 600 mV to 40 V, I_{OUT} = 100 µA			0.5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	V_{IN} = V_{OUT} + 600 mV, I_{OUT} = 100 µA to 70 mA (1)			0.5	mV
I_Q	Quiescent current	V_{IN} = 3 V to 40 V, V_{ADJ} = 2 V, I_{OUT} = 0 mA, T_J = 25ºC		TBD	31	µA
		V_{IN} = 3 V to 40 V, V_{ADJ} = 2 V, I_{OUT} = 0 mA, -40ºC < T_J < 85ºC			36	
		V_{IN} = 3 V to 40 V, V_{ADJ} = 2 V, I_{OUT} = 0 mA			42	
I_{GND}	Ground current	V_{IN} = 3 V to 40 V, V_{ADJ} = 2 V, I_{OUT} = 70 mA, T_J = 25ºC			600	
		V_{IN} = 3 V to 40 V, V_{ADJ} = 2 V, I_{OUT} = 70 mA			800	
V_{DO}	Dropout voltage	I_{OUT} = 70 mA, V_{ADJ} ≥ 3.3 V, V_{IN} = V_{ADJ} (2)			500	mV
		I_{OUT} = 50 mA, V_{ADJ} ≥ 4 V, V_{IN} = V_{ADJ} (2)			355	
$I_{SHUTDOWN}$	Shutdown supply current (I_{GND})	$V_{ADJ/EN}$ = 0 V			3	µA
$I_{ADJ/EN}$	ADJ/EN pin current	$V_{ADJ/EN}$ = V_{IN} = 13.5 V			0.3	
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising, I_{OUT} = 1 mA	2.6	2.7	2.81	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling, I_{OUT} = 1 mA	2.3	2.4	2.5	
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis			300		mV
V_{IL}	Adjust and enable logic input low level				0.7	V
V_{IH}	Adjust and enable logic input high level		2			
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1 V, V_{OUT} short to 90% x V_{ADJ}	75	100	120	mA
PSRR	Power-supply ripple rejection	V_{IN} - V_{OUT} = 1 V, Frequency = 100 Hz, I_{OUT} = 70 mA		80		dB
V_n	Output noise voltage	V_{OUT} = 3.3 V, I_{OUT} = 1 mA, a 5 μV_{RMS} reference is used for this measurement		150		μV_{RMS}
I_R	Reverse current at V_{IN}	V_{IN} = 0 V, V_{OUT} = 20 V, V_{ADJ} = 5 V	-5		5	µA
I_{RN1}	Reverse current at negative V_{IN}	V_{IN} = -20 V, V_{OUT} = 20 V, V_{ADJ} = 5 V	-5		5	
I_{RN2}	Reverse current at negative V_{IN}	V_{IN} = -20 V, V_{OUT} = 0 V, V_{ADJ} = 5 V	-5		5	
T_J	Junction temperature		–40		150	°C
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			20		°C

(1) Power dissipation is limited to 2 W for device production testing purposes. The power dissipation can be higher during normal operation. Please see the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150°C.
(2) Measured when the output voltage V_{OUT} has dropped 10 mV from the typical value.

TIming Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing Characteristics						
tstartup	Startup time	Time from EN high to V_{OUT} = 95% × V_{ADJ}, V_{ADJ} = 5 V		275		µs

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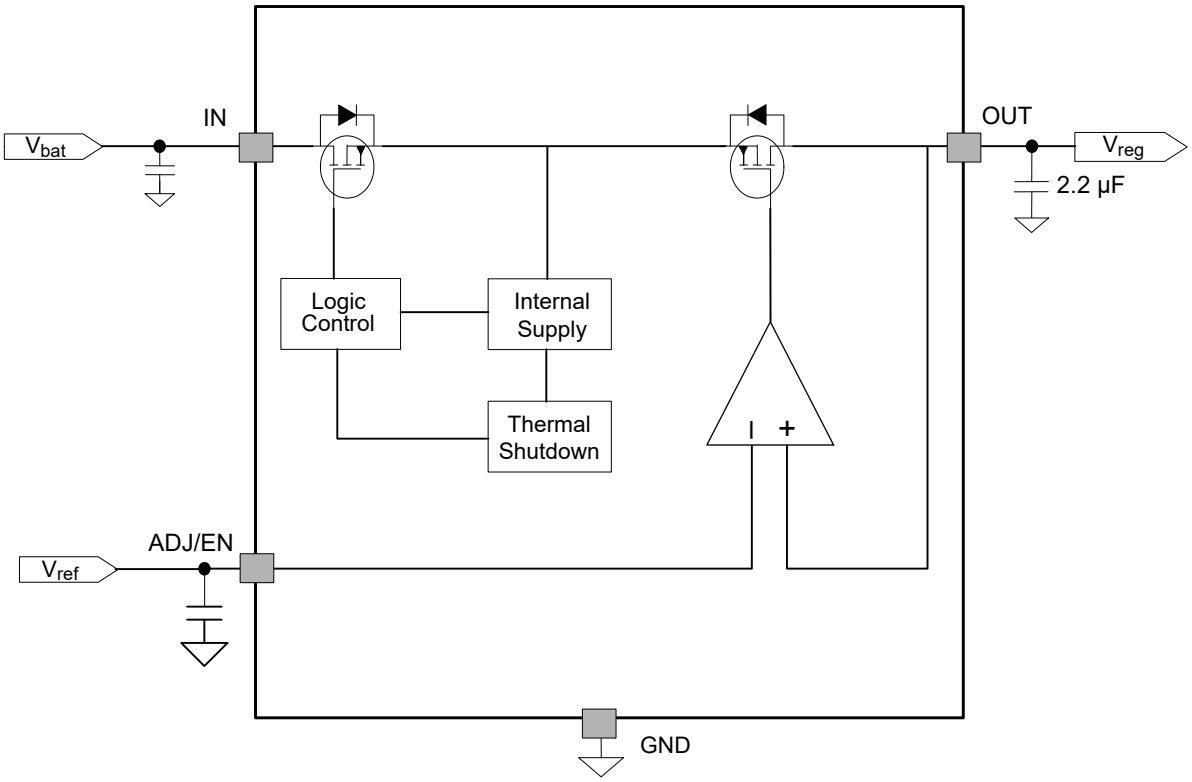
7 Detailed Description

7.1 Overview

The TPS7B4255-Q1 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering sensors off-board, multiple protection features are built into the LDO including short to battery, short to GND, and reverse current protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Regulated Output (V_{OUT})

Because this device is a tracking LDO, the output voltage is determined by the voltage provided to the ADJ pin. When the voltage at the ADJ pin exceeds the required voltage to enable the LDO, the output begins to rise to the voltage on the ADJ pin. The output rises linearly as determined by the load, the output capacitor, and the current limit. When the voltage reaches the level on the ADJ pin, the output voltage remains within a couple of millivolts from the voltage set on the ADJ pin.

7.3.2 Undervoltage Lockout

The device has an internally fixed undervoltage lockout threshold. Undervoltage lockout activates when the input voltage on V_{IN} drops below the undervoltage lockout (UVLO) level. This activation ensures the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up in the standard power-up sequence when the input voltage is above the required level.

7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle off and on. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

The internal protection circuitry of the TPS7B4255-Q1 is designed to protect against overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4255-Q1 into thermal shutdown degrades device reliability.

7.3.4 V_{OUT} Short to Battery

When the output is shorted to the battery (as shown in Figure 7-1), the TPS7B4255-Q1 survives and no damage occurs to the device. A short to the battery can also occur when the device is powered by an isolated supply, as shown in Figure 7-2, at a lower voltage. In this case, the TPS7B4255-Q1 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on V_{OUT}, which typically runs at 5 V. The continuous reverse current that flows out through V_{IN} is less than 5 µA.

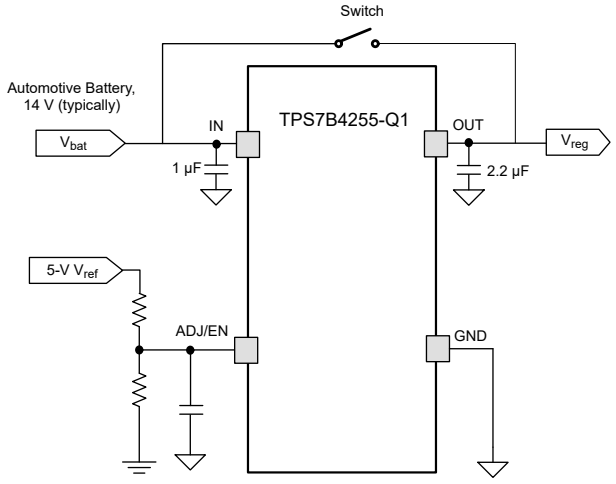


Figure 7-1. Output Voltage Short to Battery

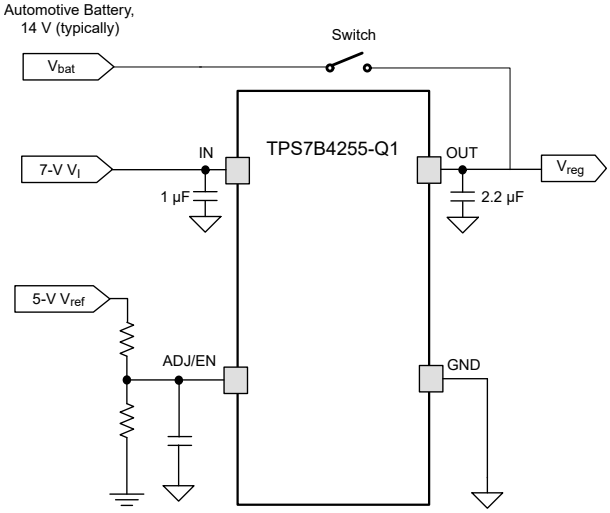


Figure 7-2. Output Voltage Higher Than the Input

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7.3.5 Tracking Regulator With an Enable Circuit

By pulling the reference voltage below 0.7 V, the device disables and enters a sleep state where the device draws 3 µA (max) from the power supply. In a real application, the reference voltage is generally sourced from another LDO voltage rail. A scenario where the device must be disabled without a shutdown of the reference voltage can occur; the device can be configured as shown in Figure 7-3 in this case. The TPS7B84-Q1 is a 150-mA LDO with ultra-low quiescent current that is used as a reference voltage to the TPS7B4255-Q1 and also as a power supply to the ADC. In a configuration as shown in Figure 7-3, the operational status of the device is controlled by a microcontroller (MCU) input or output.

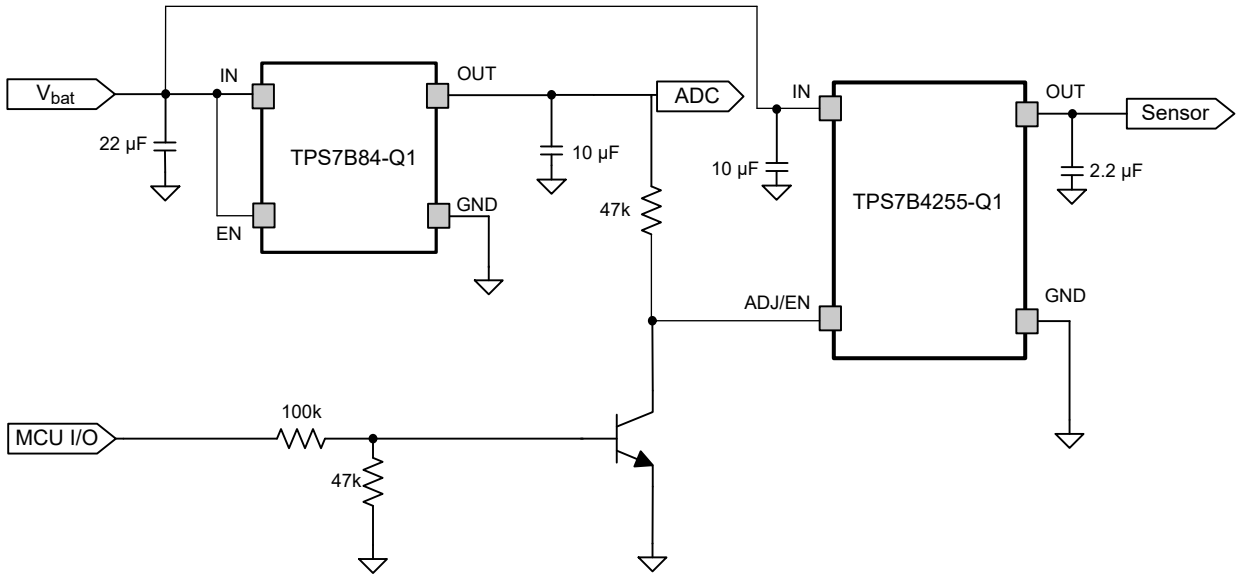

Figure 7-3. Tracking an LDO With an Enable Circuit

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} < 4 V

The device operates with input voltages above 3 V to ensure proper operation. The device turns on when V_{IN} is greater than $V_{UVLO(RISING)}$ and V_{ADJ} is greater than V_{IH}, and operates correctly as long as the input voltage stays above 3 V. For voltages below 3 V and above $V_{UVLO(FALLING)}$, the LDO continues to operate but certain circuits may not have the proper headroom to operate within specification. When the input voltage drops below $V_{UVLO(FALLING)}$ the device shuts off again.

7.4.2 Operation With ADJ/EN Control

The ADJ pin operates as both the reference and EN pin to the LDO. When the input voltage is greater than $V_{UVLO(RISING)}$ and V_{ADJ} is greater than V_{IH}, the LDO is enabled and functional. When in this mode, the LDO tracks the voltage at the ADJ pin because this pin functions as the reference to the control loop in the error amplifier. When V_{IN} is greater than $V_{UVLO(RISING)}$ and V_{ADJ} is lower than V_{IL}, the LDO is disabled and is in a lower power mode.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

8.1.1 Input and Output Capacitor Selection

The TPS7B4255-Q1 requires an output capacitor of 1 µF or larger (500 nF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 3 Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

8.1.3 Reverse Current

The TPS7B4255-Q1 incorporates reverse current protection that prevents damage from a reverse polarity (that is, when V_{OUT} is higher than V_{IN}). During a reverse polarity event where the V_{IN} and V_{OUT} absolute maximum ratings are not violated and $V_{OUT} – V_{IN}$ is less than 40 V, less than 5 µA flows out of V_{IN}.

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8.2 Typical Application

Figure 8-1 shows a typical application circuit for the TPS7B4255-Q1.

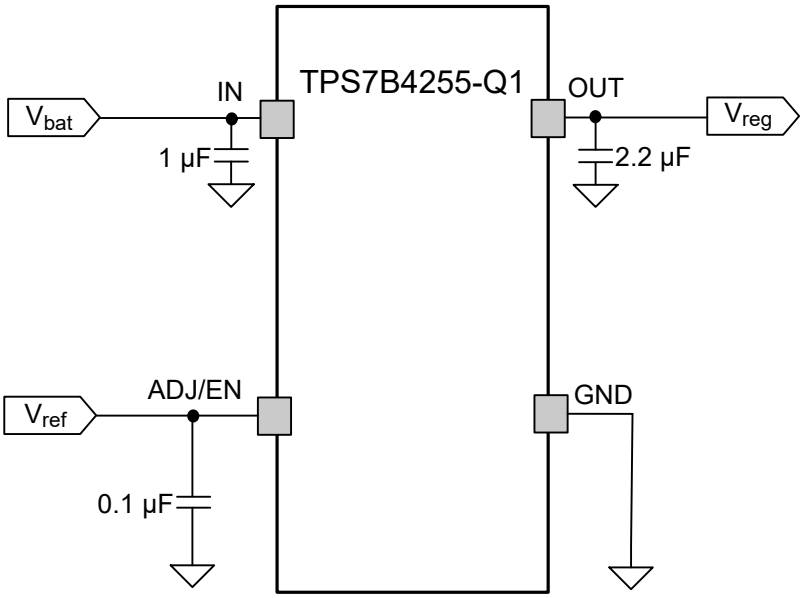

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	3 V to 40 V
ADJ reference voltage	2 V to 20 V
Output voltage	2 V to 20 V
Output current rating	70 mA
Output capacitor range	1 µF to 200 µF
Output capacitor ESR range	1 mΩ to 3 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

An input capacitor, C_{IN}, is recommended to help filter line influences. Connect the capacitors close to the device pins.

The output capacitor for the TPS7B4255-Q1 is required for stability. Without the output capacitor, the regulator oscillates. The actual size and type of the output capacitor can vary based on the application load and temperature range. The effective series resistance (ESR) of the capacitor is also a factor in the device stability. The worst case is determined at the minimum ambient temperature and maximum load expected. To ensure stability of the TPS7B4255-Q1, the device requires an output capacitor between 1 µF and 200 µF with an ESR range between 0.001 Ω and 3 Ω, which covers most types of capacitor ESR variation under the recommend operating conditions. As a result, the output capacitor selection is flexible.

The capacitor must also be rated for all ambient temperatures expected in the system. To maintain regulator stability down to –40°C, use a capacitor rated at that temperature.

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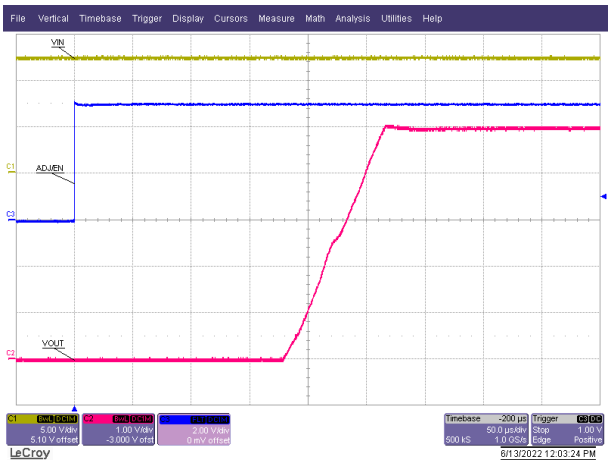
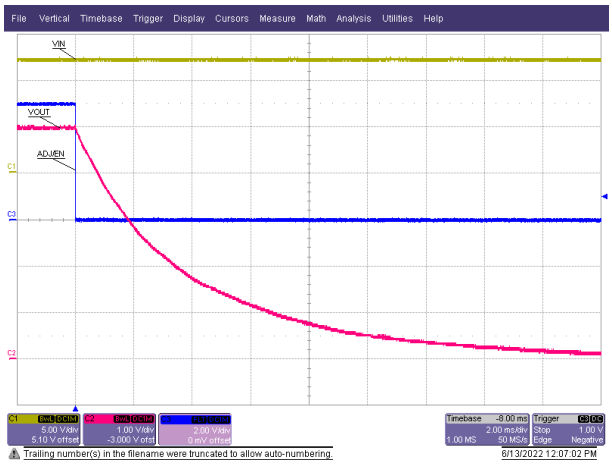
8.2.3 Application Curves



V_I = 12 V, V_{ADJ} = 5 V, C_{OUT} = 1 µF, R_{LOAD} = 4.7 kΩ

Figure 8-2. Power Up



V_I = 12 V, V_{ADJ} = 5 V, C_{OUT} = 1 µF, R_{LOAD} = 4.7 kΩ

Figure 8-3. Power Down

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. If the input supply is located more than a few inches from the TPS7B4255-Q1, add an electrolytic capacitor with a value of 10 µF and a ceramic bypass capacitor at the input.

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8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. TI also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

8.4.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4255-Q1 are available at the end of this document and at www.ti.com.

8.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7B4255-Q1 evaluation board, available at www.ti.com.

8.4.1.3 Power Dissipation and Thermal Considerations

Equation 2 calculates the device power dissipation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (2)$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- I_Q = Quiescent current

Because I_Q is much less than I_{OUT}, the term $I_Q \times V_{IN}$ in Equation 2 can be ignored.

Calculate the junction temperature (T_J) with Equation 3 for a device under operation at a given ambient air temperature (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

where:

- $R_{\theta JA}$ = Junction-to-junction-ambient air thermal impedance

Equation 4 calculates a rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (4)$$

The maximum ambient air temperature (T_{AM}) at which the device can operate can be calculated with Equation 5 for a given maximum junction temperature (T_{JM}).

$$T_{AM} = T_{JM} - (R_{\theta JA} \times P_D) \quad (5)$$

8.4.2 Layout Examples

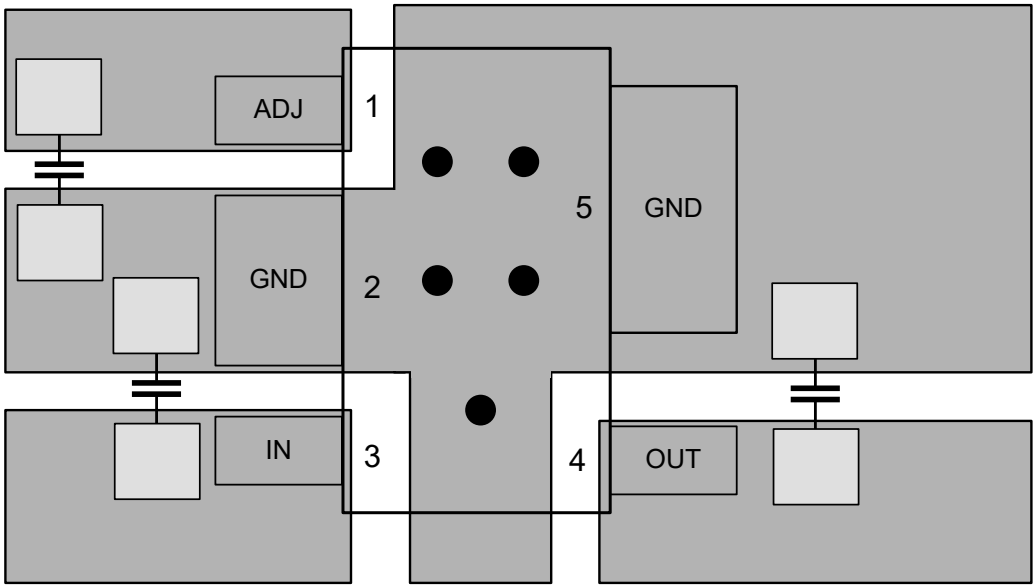


Figure 8-4. DYB Package Layout Example

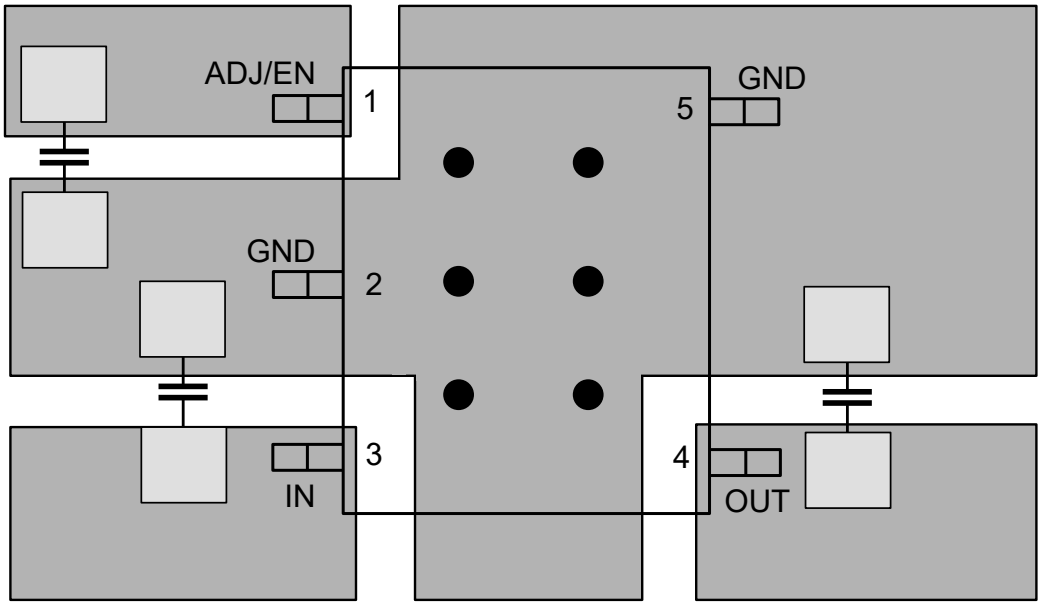


Figure 8-5. DBV Package Layout Example

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

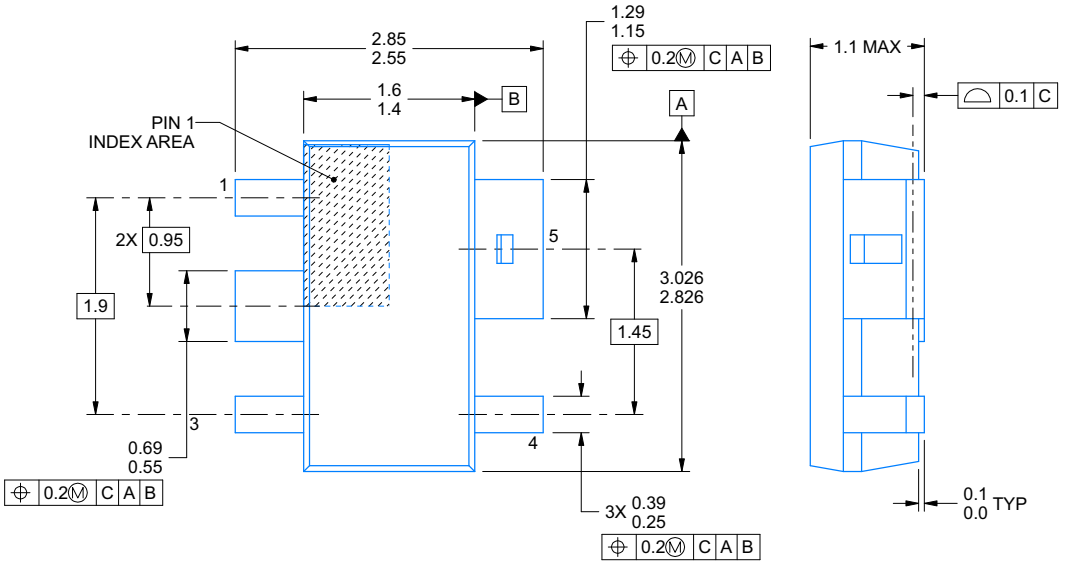
10.1 Mechanical Data

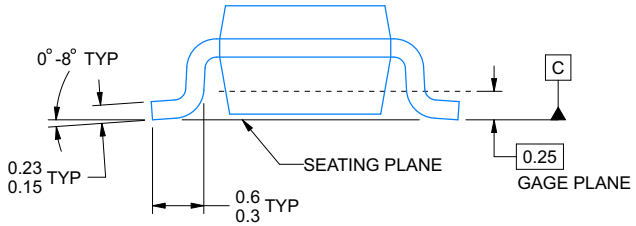
PACKAGE OUTLINE

DYB0005A

SOT - 1.1 max height

SOT





4226199/A 09/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No JEDEC reference as of August 2020.

ADVANCE INFORMATION

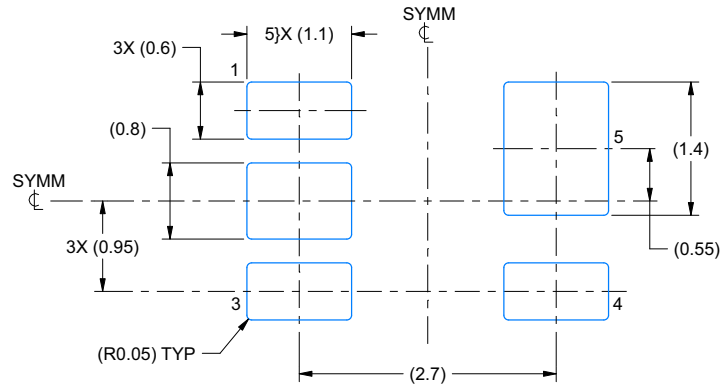
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

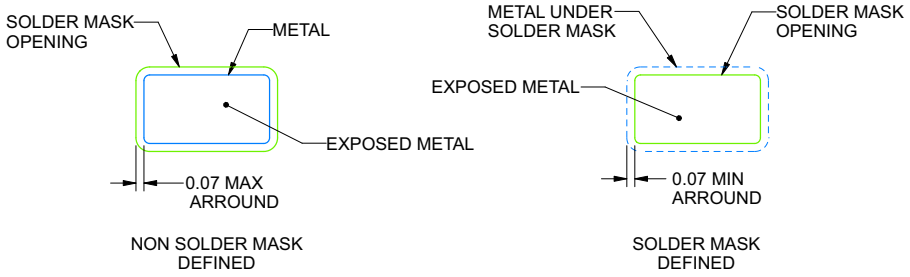
DYB0005A

SOT - 1.1 max height

SOT



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

4226199/A 09/2020

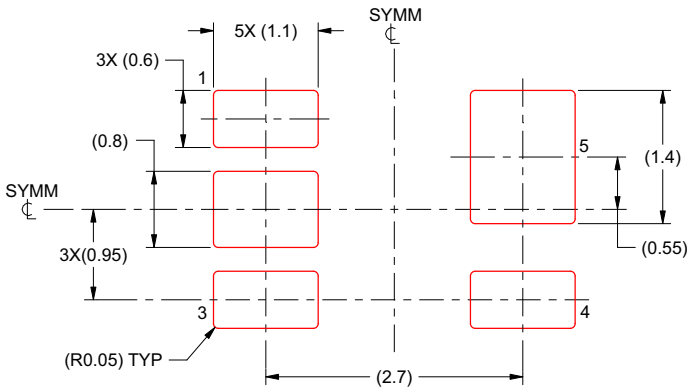
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYB0005A — **SOT - 1.1 max height**

SOT



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4226199/A 09/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7B4255QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7B4255QDYBRQ1	ACTIVE	SOT-23	DYB	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

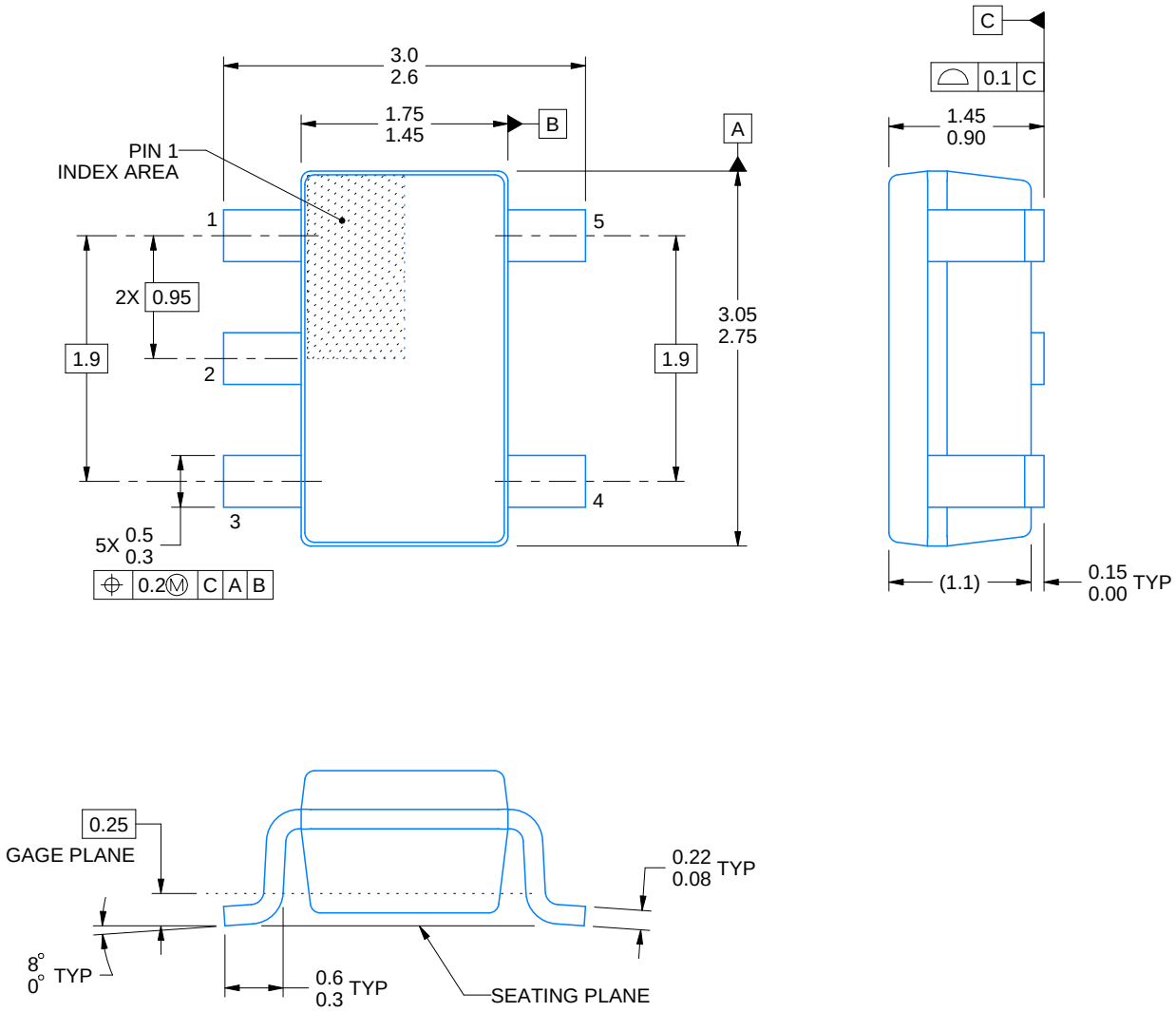
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

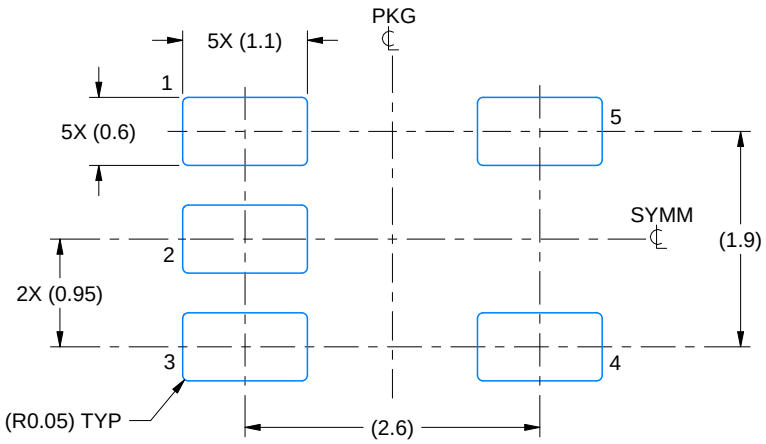
SMALL OUTLINE TRANSISTOR



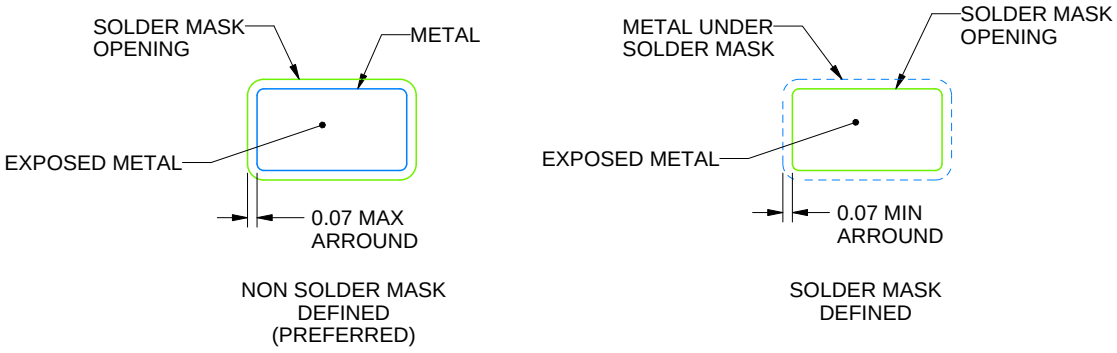
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

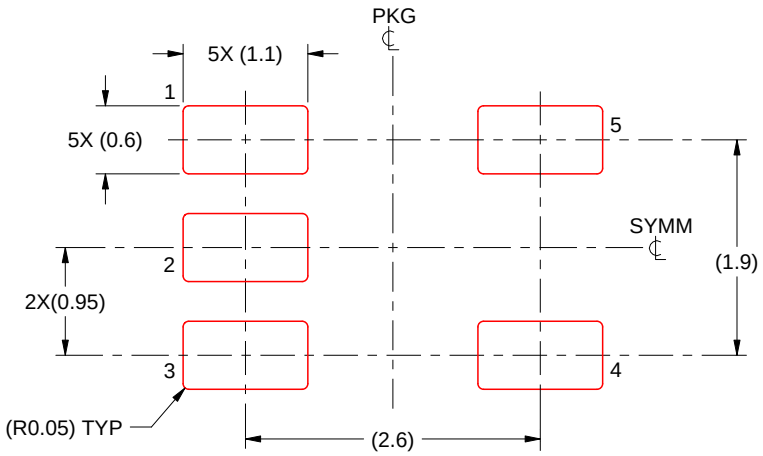


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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