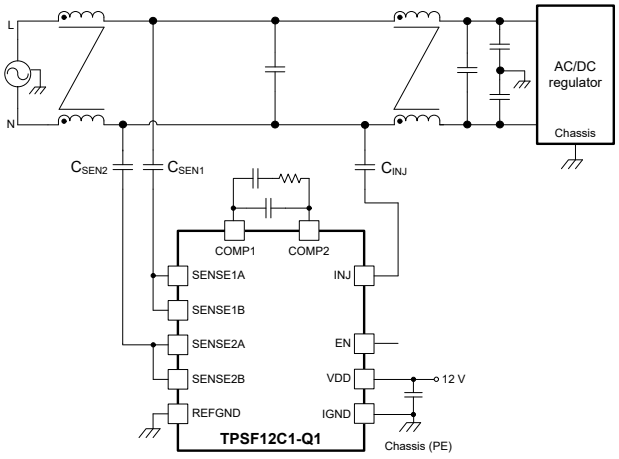
# TPSF12C1-Q1 Standalone Active EMI Filter for Common-mode Noise Mitigation in Single-Phase AC Automotive Power Systems

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Voltage-sense, current-inject active EMI filter
  - Optimized for CISPR 25 Class 5 automotive EMI requirements
  - Low impedance for common-mode emissions
  - 50%+ reduction in choke size, weight and cost
  - Peak inject current of ±80 mA (typical)
- Wide supply voltage range of 8 V to 16 V
- –40°C to 150°C junction temperature range
- Simple configuration for single-phase AC systems
  - Integrated sensing filter and summing network
  - Low leakage current at line frequency
  - Simplified compensation network
- Inherent protection features for robust design
  - Withstands 5-kV surge (IEC 61000-4-5) with minimal external component count
  - Enable pin for remote ON and OFF control
  - VDD voltage UVLO protection with hysteresis
  - Thermal shutdown protection with hysteresis
- 4.2-mm × 2-mm SOT-23 14-pin (DYY) package

## 2 Applications

- On-board charger and isolated DC/DC for EVs
- Isolated DC/DC for servers, AC/DC for telecom
- Inverters and HVAC motor control




**Simplified Schematic**

## 3 Description

The TPSF12C1-Q1 is an active filter IC designed to reduce common-mode (CM) electromagnetic interference (EMI) in single-phase AC power systems.

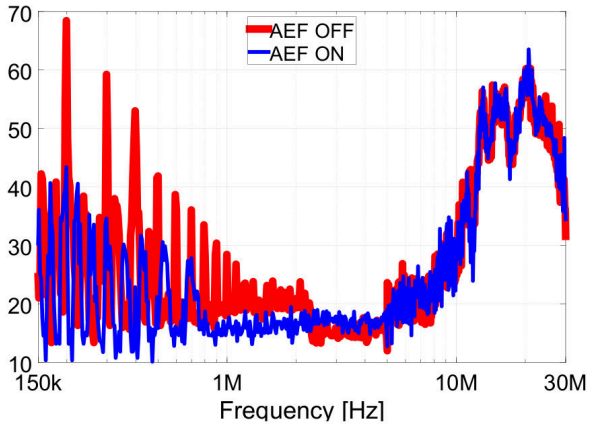
The active EMI filter (AEF) configured with voltage sense and current inject (VSCI) uses a capacitive multiplier circuit to emulate the Y-capacitors in a conventional passive filter design. The device senses the high-frequency noise on each power line using a set of sense capacitors and injects noise-canceling currents back into the power lines using an injection capacitor. The effective active capacitance is set by the circuit gain and the injection capacitance. The AEF sensing and injection impedances use relatively low capacitance values with small component footprints. The device includes integrated filtering, compensation and protection circuitry, and an enable input.

The TPSF12C1-Q1 provides a very low impedance path for CM noise in the frequency range of interest for EMI measurement. Enabling up to 25 dB of CM noise reduction at the lower end of specified frequency ranges (for example, 150 kHz to 3 MHz) significantly reduces the size, weight and cost of the CM filter implementation.

**Package Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| TPSF12C1-Q1 | DYY (SOT-23-THIN, 14) | 4.20 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**EMI Mitigation Result**

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## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| November 2022 | * | Advance Information initial release |

## 5 Device Comparison Table

| DEVICE | ORDERABLE PART NUMBER | PHASES | GRADE | JUNCTION TEMPERATURE RANGE |
|---|---|---|---|---|
| TPSF12C1-Q1 | TPSF12C1QDYYRQ1 | 1 | Automotive | –40°C to 150°C |
| TPSF12C3-Q1 | TPSF12C3QDYYRQ1 | 3 | Automotive | –40°C to 150°C |
| TPSF12C1 | TPSF12C1DYYR | 1 | Commercial | –40°C to 150°C |
| TPSF12C3 | TPSF12C3DYYR | 3 | Commerical | –40°C to 150°C |

## 6 Pin Configuration and Functions

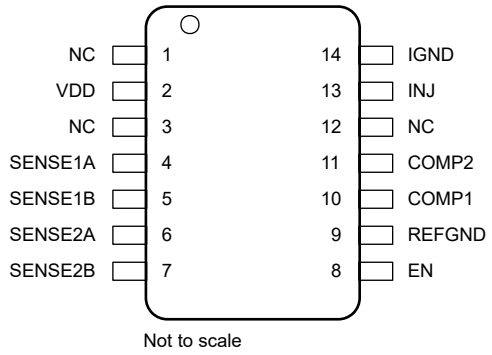


**Figure 6-1. 14-Pin SOT-23-THIN DYY Package (Top View)**

**Table 6-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1, 3, 12 | NC | – | No internal connection. Tie to the GND plane on the PCB. |
| 2 | VDD | P | Power supply for IC. Bypass to IGND with a 1-µF X7R ceramic capacitor. |
| 4 | SENSE1A | I | Sense input (power line or neutral) |
| 5 | SENSE1B | I | Sense input (power line or neutral) |
| 6 | SENSE2A | I | Sense input (power line or neutral) |
| 7 | SENSE2B | I | Sense input (power line or neutral) |
| 8 | EN | I | Enable signal to activate noise cancellation |
| 9 | REFGND | G | Reference ground (Kelvin connected to IGND) |
| 10 | COMP1 | I | Connection 1 for external compensation circuit |
| 11 | COMP2 | I | Connection 2 for external compensation circuit |
| 13 | INJ | O | Injection signal output |
| 14 | IGND | G | Injection ground |

(1) P = Power, G = Ground, I = Input, O = Output

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# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage | VDD to IGND and REFGND | –0.3 | 18 | V |
| Pin voltage | SENSE1A, SENSE1B, SENSE2A, SENSE2B to REFGND | –5.5 | 5.5 | V |
| Pin voltage | COMP1 to IGND and REFGND | –0.3 | 5.5 | V |
| Pin voltage | COMP2 to IGND and REFGND | –0.3 | 15 | V |
| Pin voltage | INJ to IGND | –0.3 | $V_{VDD}$ + 0.3 | V |
| Pin voltage | EN to IGND and REFGND | –0.3 | 18 | V |
| Pin voltage | IGND to REFGND | –0.3 | 0.3 | V |
| Sink current | INJ | | 150 | mA |
| Source current | INJ | | 150 | mA |
| $T_J$ | Operating junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2 | | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B | Corner pins (1, 7, 8, and 14) | ±750 | |
| | | | Other pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VDD}$ | VDD voltage range | | 8 | 12 | 16 | V |
| $V_{INJ}$ | Output voltage range | | 2 | | $V_{VDD}$ – 2 | V |
| $V_{SENSE}$ | Sense voltage range | | –5 | | 5 | V |
| $V_{EN}$ | Pin voltage | | 0 | | 16 | V |
| $I_{INJ}$ | Output current range | Source and sink magnitude | | | 80 | mA |
| $T_A$ | Operating ambient temperature | | –40 | | 105 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | DYY (SOT-23-THIN) 14 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 110 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 35 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 35 | °C/W |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

## 7.5 Electrical Characteristics

Limits apply over the junction temperature ($T_J$) range of –40°C to 150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{VDD}$ = 12 V(1).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | VDD quiescent current | SENSE1A, SENSE1B, SENSE2A, and SENSE2B grounded, $V_{EN}$ = 5 V, 8 V < $V_{VDD}$ < 16 V | 6.25 | 12.5 | 23.5 | mA |
| $I_{SD}$ | VDD shutdown supply current | $V_{EN}$ = 0 V | | 50 | | µA |
| **SUPPLY VOLTAGE UVLO** | | | | | | |
| $VDD_{UVLO(R)}$ | UVLO rising threshold | $V_{VDD}$ rising | 7.5 | 7.7 | 7.95 | V |
| $VDD_{UVLO(F)}$ | UVLO falling threshold | $V_{VDD}$ falling | 6.4 | 6.7 | 7.0 | V |
| $VDD_{UVLO(H)}$ | UVLO hysteresis | | | 0.96 | | V |
| **ENABLE** | | | | | | |
| $V_{EN\_H}$ | EN voltage high | | 2.2 | | | V |
| $V_{EN\_L}$ | EN voltage low | | | | 0.8 | V |
| $R_{EN}$ | EN pin pull-up resistance to VDD | $V_{EN}$ = 0 V | | 900 | | kΩ |
| $I_{EN(LKG)}$ | EN input leakage current | $V_{EN}$ = 12 V | | 850 | | nA |
| **INPUT FILTER NETWORK** | | | | | | |
| $A_{CM}$ | Gain from shorted power lines through single sense cap, $C_{SEN}$, to COMP1 pin vs. REFGND | $C_{SEN}$ = 2 µF, 60 Hz | | –42 | | dB |
| | | $C_{SEN}$ = 2 µF, 50 kHz | | –4 | | |
| | | $C_{SEN}$ = 2 µF, 500 kHz(2) | | –1.5 | | |
| | | $C_{SEN}$ = 2 µF, 1 MHz(2) | | –1 | | |
| $A_{DM}$ | Gain from differential signal applied to SENSE lines to COMP1 pin vs. REFGND | SENSE1A shorted to SENSE1B, SENSE2A shorted to SENSE2B, $C_{SEN1}$ = $C_{SEN2}$ = 1 µF, 60 Hz | | –78 | | dB |
| | | SENSE1A shorted to SENSE1B, SENSE2A shorted to SENSE2B, $C_{SEN1}$ = $C_{SEN2}$ = 1 µF, 1 kHz | | –59 | | |
| | | SENSE1A shorted to SENSE1B, SENSE2A shorted to SENSE2B, $C_{SEN1}$ = $C_{SEN2}$ = 1 µF, 500 kHz(2) | | –35 | | |
| | | SENSE1A shorted to SENSE1B, SENSE2A shorted to SENSE2B, $C_{SEN1}$ = $C_{SEN2}$ = 1 µF, 1 MHz(2) | | –36 | | |
| | | SENSE1A shorted to SENSE1B, SENSE2A shorted to SENSE2B, $C_{SEN1}$ = $C_{SEN2}$ = 1 µF, 10 MHz(2) | | –35 | | |

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## 7.5 Electrical Characteristics (continued)

Limits apply over the junction temperature ($T_J$) range of –40°C to 150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{VDD}$ = 12 V(1).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AMPLIFIER** | | | | | | |
| $A_{DC}$ | DC gain | | 53 | 58 | 62 | dB |
| $F_{BW}$ | Unity gain bandwidth | | | 113 | | MHz |
| $F_{BW}$ | 40 dB bandwidth | | | 1 | | MHz |
| $V_{OFST}$ | COMP1 offset voltage | | | 2 | | V |
| $V_{INJ\_MAX}$ | Maximum output voltage for linear operation | 10% drop in gain | $V_{VDD}$ – 2 | | | V |
| $V_{INJ\_MIN}$ | Minimum output voltage for linear operation | 10% drop in gain | | | 2 | V |
| $I_{INJ\_MAX\_OP}$ | INJ current at linearity limits | $V_{INJ}$ = $V_{VDD}$ – 2 V | 80 | | | mA |
| | | $V_{INJ}$ = $V_{IGND}$ + 2 V | | | –80 | mA |
| **PSRR** | | | | | | |
| $PSRR_{10}$ | | 8 V < $V_{VDD}$ < 16 V, See recommended feedback network, 10 kHz | | 0 | | dB |
| $PSRR_{100}$ | | 8 V < $V_{VDD}$ < 16 V, See recommended feedback network, 100 kHz | | 6 | | |
| **STARTUP** | | | | | | |
| $t_W$ | Startup delay | Period from VDD = EN applied until output valid | | 43 | | ms |
| $t_{SU}$ | EN high to valid output | | | 12 | | ms |
| $t_{SD}$ | EN low to stop output signal | | | 55 | | µs |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J\text{-}SHD}$ | Thermal shutdown threshold(2) | Temperature rising | | 175 | | °C |
| $T_{J\text{-}HYS}$ | Thermal shutdown hysteresis(2) | | | 20 | | °C |

(1) MIN and MAX limits are 100% production tested at 25ºC unless otherwise specified. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Parameter specified by design, statistical analysis and production testing of correlated parameters.

## 7.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to $T_J$ = 25°C and $V_{VDD}$ = 12 V only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of $T_J$ = –40°C to 150°C. These specifications are not ensured by production testing.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_{SUPPLY}$ | Input supply current with INJ loaded | | | 15 | | mA |

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# 8 Detailed Description

## 8.1 Overview

The TPSF12C1-Q1 is an active electromagnetic interference (EMI) filter controller that is designed to reduce common-mode (CM) conducted emissions in off-line power converter systems. The device senses the high-frequency noise on each power line using a set of Y-rated capacitors, $C_{SEN1}$ and $C_{SEN2}$, then injects noise-canceling currents back into the power lines using a Y-rated capacitor $C_{INJ}$ along with damping circuitry that ensures stability. The device includes integrated filtering, compensation and protection circuitry.

The TPSF12C1-Q1 provides a very low impedance path for CM noise in the frequency range of interest for EMI measurement. This feature can achieve approximately 15 to 25 dB of CM noise reduction over the frequency range of interest, for example, 150 kHz to 3 MHz, helping to reduce the size of common-mode chokes.

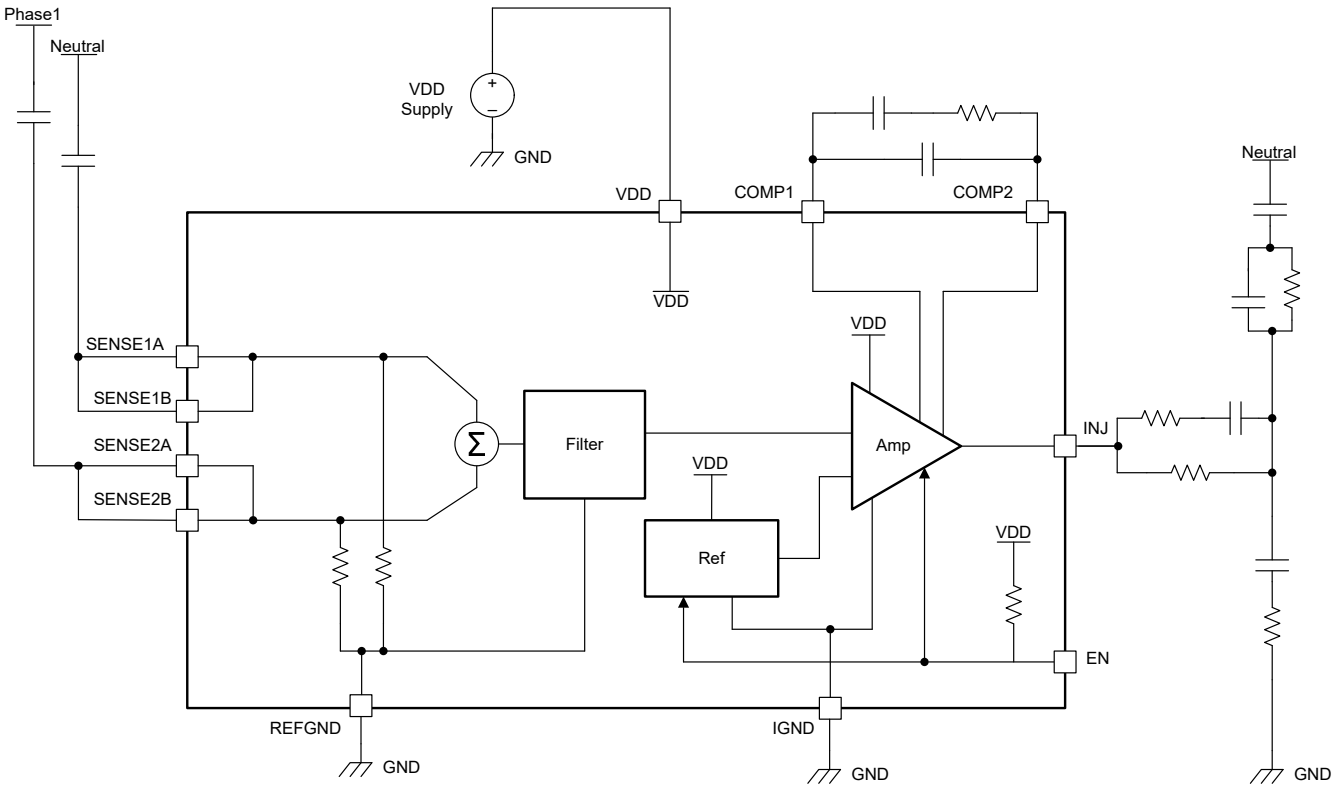
The TPSF12C1-Q1 operates over a supply voltage range of 8 V to 16 V and can withstand 18 V. The device features include:

- Internal circuitry that simplifies compensation and design
- Built-in supply voltage UVLO to ensure proper operation
- Built-in thermal shutdown protection
- An EN input that allows power saving when the system is idling

The active EMI feature significantly reduces EMI filtering cost, size, and weight, while helping to meet CISPR 25 Class 5 EMI limits for conducted and radiated emissions.

Leveraging a pin arrangement designed for simple layout that requires relatively few external components, the TPSF12C1-Q1 is specified for maximum ambient and junction temperatures of 105°C and 150°C, respectively.

## 8.2 Functional Block Diagram

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## 8.3 Feature Description

### 8.3.1 Integrated Line Filter

The TPSF12C1-Q1 has a built-in input line filter. Because the entire filter is integrated in the device, matching is better than what can be achieved using discrete components. This filter not only removes virtually all input at line frequency, it also sums the signals from the sense inputs to create a signal that represents the common-mode noise signature without line-frequency components.

### 8.3.2 Compensation

The TPSF12C1-Q1 contains partial internal compensation that, when combined with two capacitors and a resistor between COMP1 and COMP2, forms a lead-lag network. This internal network allows fewer external components to be used.

### 8.3.3 Enable

The TPSF12C1-Q1 has an enable input, EN, that allows the device to be shut down, drastically reducing power consumption during intervals when EMI mitigation is not required. The typical quiescent current consumption is 12.5 mA and 50 µA when the device is enabled and disabled, respectively. Because many designs do not use this feature, a 900-kΩ pull up resistor connects internally between VDD and EN, allowing the EN pin to be left open.

In addition, INJ is pulled low when the device is disabled to reduce the parasitic resistance in series with $C_{INJ}$.

### 8.3.4 Supply Voltage UVLO Protection

To ensure that the TPSF12C1-Q1 operates safely while VDD is powered on and off as well as during brownout conditions, this device has a built-in UVLO protection to provide predictable behavior while VDD is below its operating voltage. UVLO releases when the VDD voltage exceeds 7.95 V, allowing normal operation. UVLO engages if the VDD voltage falls below approximately 6.6 V. There is approximately 1 V of UVLO hysteresis.

### 8.3.5 Thermal Shutdown Protection

The TPSF12C1-Q1 provides built-in overtemperature protection that shuts down the device if the junction temperature exceeds approximately 175°C. After junction temperature drops by approximately 20°C, the device restarts. This process is repeated until the ambient temperature or power dissipation is reduced.

## 8.4 Device Functional Modes

### 8.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSF12C1-Q1. When the EN voltage is below approximately 0.8 V, the device is in shutdown mode. Most internal circuitry is shutdown. The quiescent current in shutdown mode drops to 50 µA (typical). The TPSF12C1-Q1 also employs VDD internal undervoltage protection. If the VDD voltage is below its UV threshold, the IC remains off. The INJ output pulls to ground while in shutdown mode.

### 8.4.2 Active Mode

The TPSF12C1-Q1 is in active mode when $V_{VDD}$ is above its UVLO threshold, EN is high, and there is no overtemperature fault. The simplest way to enable operation is to connect EN to VDD, which allows startup when the applied supply voltage exceeds the UVLO threshold voltage. In this mode, the device amplifies signals on COMP2 and outputs the amplified signal on the INJ pin.

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# 9 Applications and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The TPSF12C1-Q1 common-mode AEF IC helps to improve the CM EMI signature of single-phase power systems. The device provides a very low impedance path for CM noise in the frequency range of interest for EMI measurement and helps to meet prescribed limits for EMI standards, such as:

- CISPR 11, EN 55011 – Industrial, Scientific and Medical (ISM) applications
- CISPR 25, EN 55025 – Automotive applications
- CISPR 32, EN 55032 – Multimedia applications

To expedite and streamline the process of designing of a TPSF12C1-Q1-based solution, a comprehensive TPSF12C1-Q1 quickstart calculator is available by download to assist the system designer with component selection for a given application.

## 9.2 Typical Applications

For the circuit schematic, bill of materials, PCB layout files, and test results of a TPSF12C1-Q1-powered implementation, see the TPSF12C1-Q1 EVM.

### 9.2.1 Design 1 – AEF Circuit for High-Density On-Board Charger (OBC) in Electric Vehicles (EVs)

Figure 9-1 shows a schematic diagram of a 6.6-kW high-density OBC with conventional two-stage passive EMI filter. The CM chokes and Y-capacitors provide CM filtering, whereas the leakage inductance of the CM chokes and the X-capacitors provide DM filtering. Similar to TI reference design TIDM-02013, the circuit uses a two-phase totem-pole (TTPL) power-factor correction (PFC) front-end followed by a full-bridge CLLLC topology with active synchronous rectification.

The TTPL PFC stage runs at a fixed switching frequency of 120 kHz. The CLLLC isolated DC/DC stage runs at a variable frequency from 200 kHz to 800 kHz (500-kHz nominal) and provides galvanic isolation in addition to battery voltage and current regulation. Even though the use of LMG3522-Q1 GaN switches enables an open-frame power density of 3.8 kW/L, the conventional passive EMI filter occupies over 20% of the total solution size.

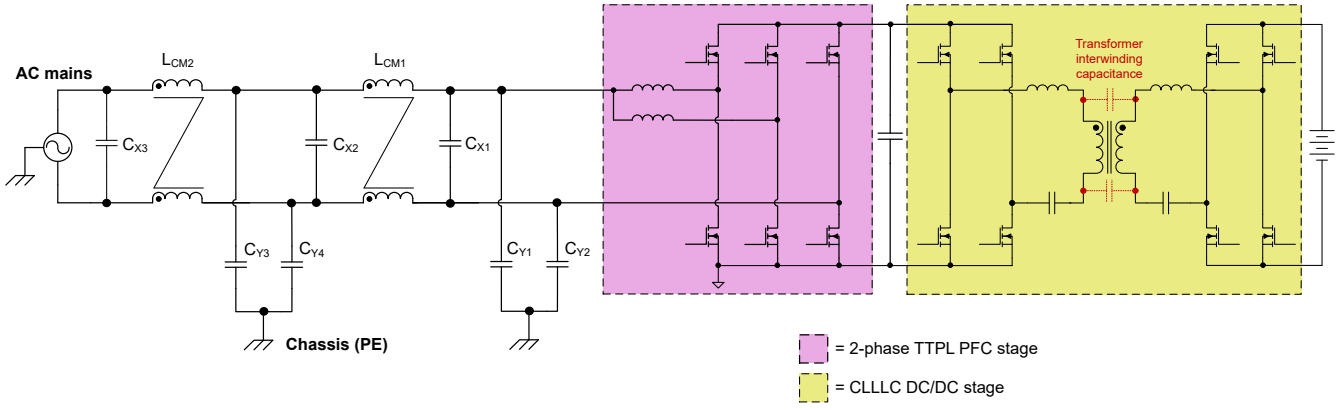


**Figure 9-1. Circuit Schematic of an OBC With a Conventional Two-Stage EMI Filter**

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Note that the DC/DC stage in particular increases the CM EMI signature based on the high dv/dt of the GaN switches, the transformer interwinding capacitance as well as the various switch-node parasitic capacitances to chassis ground.

This application example replaces the two Y-capacitors, designated as $C_{Y3}$ and $C_{Y4}$ in Figure 9-1, with a single-phase AEF circuit using the TPSF12C1-Q1. See Figure 9-2. The AEF circuit provides capacitive multiplication, which reduces the inductance value and thus the size, weight, and cost of the CM chokes, now designated as $L_{CM1\text{-}AEF}$ and $L_{CM2\text{-}AEF}$. The total capacitance of the sense and inject capacitors is kept less than or equal to that of the replaced Y-capacitors, which results in the the total line-frequency leakage curernt remaining effectively unchanged or reduced.

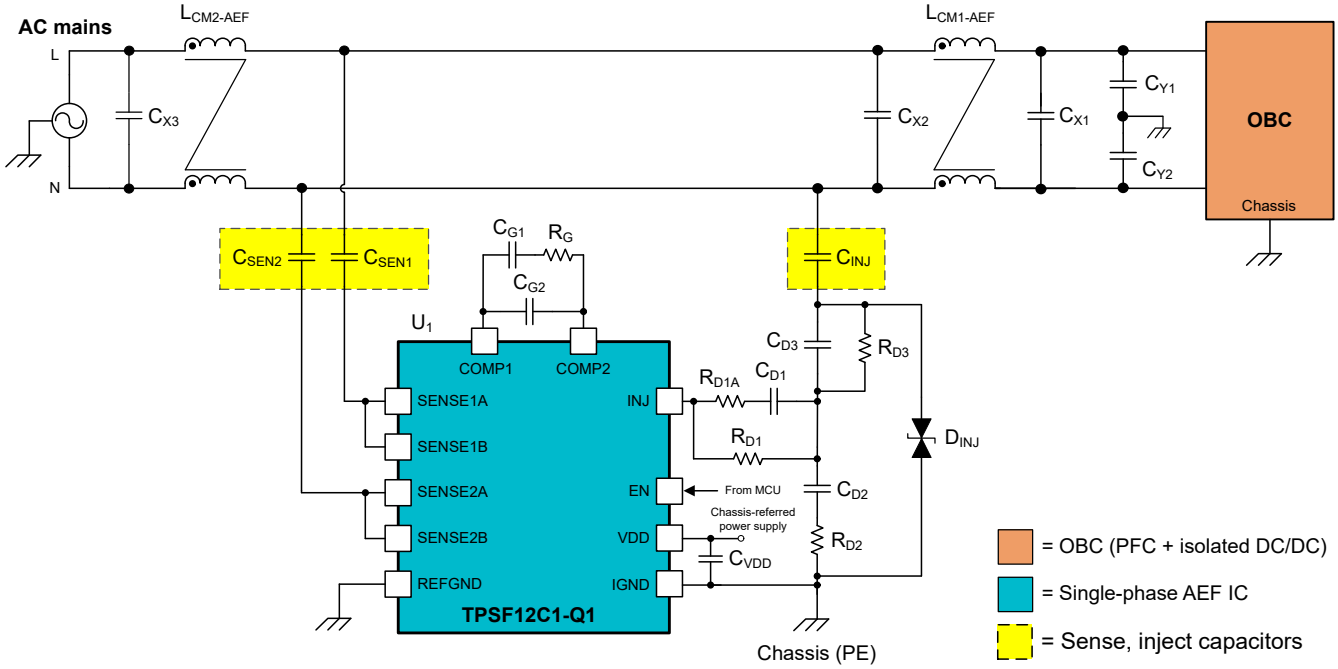


**Figure 9-2. Circuit Schematic of an OBC With AEF Circuit Connected**

### *9.2.1.1 Design Requirements*

Table 9-1 shows the intended operating parameters for this application example.

**Table 9-1. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| AC input voltage range | 85 V to 265 V RMS |
| AC input line frequency | 47 Hz to 63 Hz |
| Input RMS current (maximum) | 32 A |
| DC output voltage range | 250 V to 450 V |
| Rated output power | 6.6 kW |
| Output current (maximum) | 20 A |
| AC/DC stage switching frequency (fixed) | 120 kHz |
| DC/DC stage switching frequency (variable) | 200 kHz to 800 kHz |

#### 9.2.1.2 Detailed Design Procedure

Table 9-2 gives the selected component values, which are the same as those used in the TPSF12C1-Q1 EVM. This design uses a TVS diode placed at the low-voltage side of the inject capacitor for clamping during input surge conditions.

**Table 9-2. AEF Circuit Components for Application Circuit 1**

| REFERENCE DESIGNATOR | QTY | SPECIFICATION | MANUFACTURER(1) | PART NUMBER |
|---|---|---|---|---|
| $C_{SEN1}$, $C_{SEN2}$ | 2 | Capacitor, ceramic, 680 pF, 300 VAC, Y2 | MuRata | DE2B3SA681KN3AX02F |
| $C_{INJ}$ | 1 | Capacitor, ceramic, 4.7 nF, 300 VAC, Y2 | MuRata | DE2E3SA472MA3BX02F |
| $C_{D1}$ | 1 | Capacitor, ceramic, 4.7 nF, 50 V, 0603 | Various | – |
| $C_{D2}$ | 1 | Capacitor, ceramic, 22 nF, 50 V, 0603 | Various | – |
| $C_{D3}$ | 1 | Capacitor, ceramic, 4.7 nF, 50 V, 0603 | Various | – |
| $C_{G1}$ | 1 | Capacitor, ceramic, 10 nF, 50 V, 0603 | Various | – |
| $C_{G2}$ | 1 | Capacitor, ceramic, 10 pF, 50 V, 0603 | Various | – |
| $C_{VDD}$ | 1 | Capacitor, ceramic, 1 µF, 25 V, X7R, 0603 | Various | – |
| $D_{INJ}$ | 1 | TVS diode, bidirectional, 24 V, SOD-323 | Eaton | STS321240B301 |
| $R_{D1}$ | 1 | Resistor, 1 kΩ, 0.1 W, 0603 | Various | – |
| $R_{D1A}$ | 1 | Resistor, 50 Ω, 0.1 W, 0603 | Various | – |
| $R_{D2}$ | 1 | Resistor, 200 Ω, 0.1 W, 0603 | Various | – |
| $R_{D3}$ | 1 | Resistor, 698 Ω, 0.1 W, 0603 | Various | – |
| $R_G$ | 1 | Resistor, 1.5 kΩ, 0.1 W, 0603 | Various | – |
| $U_1$ | 1 | TPSF12C1-Q1 common-mode AEF IC for single-phase power systems | Texas Instruments | TPSF12C1QDYYRQ1 |

(1) See the *Third-Party Products Disclaimer*.

More generally, the TPSF12C1-Q1 AEF IC is designed to operate with a wide range of passive filter components and system parameters.

##### 9.2.1.2.1 Sense Capacitors

The sense pins of the TPSF12C1-Q1 feed into a second-order high-pass filter and signal combiner within the IC, which rejects the line-frequency and DM components of the power line voltages, extracting the high-frequency CM component. These sense pins operate in pairs: SENSE1A and SENSE2A connect to SENSE1B and SENSE2B, respectively.

The sense pins externally interface to the power lines using two Y-rated capacitors, designated as $C_{SEN1}$ and $C_{SEN2}$ in Figure 9-2. Choose Y2-rated sense capacitors of 680 pF, 300 VAC in this application to establish voltages at the SENSE pins of 3-V peak-to-peak when operating at maximum line voltage.

##### 9.2.1.2.2 Inject Capacitor

The INJ node interfaces to a power line using a Y-rated capacitor, designated as $C_{INJ}$ in Figure 9-2. Choose a Y2-rated inject capacitor of 4.7 nF, 300 VAC in this design to accommodate an AC swing with at least a 2-V margin of headroom from the positive and negative supply rails.

The INJ pin biases at half the VDD supply voltage. Assuming a 12-V supply rail and allowing 2 V of upper and lower headroom, this implies that a swing of ±4 V is available around the DC operating point.

##### 9.2.1.2.3 Compensation Network

The CM noise signal derived from the internal sensing filter and summation network of the TPSF12C1-Q1 is internally inverted and amplified by a gain stage. The components between the COMP1 and COMP2 pins of the IC, designated as as $R_G$, $C_{G1}$ and $C_{G2}$ in Figure 9-2, set the gain characteristic.

More specifically, resistor $R_G$ establishes a high midband AEF gain at frequencies where EMI filtering is required. Capacitor $C_{G1}$ increases the impedance of that branch at low frequencies, which sets a lower AEF amplifer gain

ADVANCE INFORMATION

to further reject line-frequency components appearing at the INJ output. Capacitor $C_{G2}$ preserves gain at high frequencies, which extends the AEF bandwidth.

Choose a value for $R_G$ between 1 kΩ and 2 kΩ. A resistance of 1.5 kΩ is a common choice and selected in this example to set a midband gain of 50 dB. Choose capacitances for $C_{G1}$ and $C_{G2}$ of 10 nF and 10 pF, respectively, which establishes a gain rolloff below approximately 10 kHz for line-and low-frequency attenuation.

#### 9.2.1.2.4 Injection Network

The components connected between the INJ pin and inject capacitor establish a damped injection network. Damping is specifically required to manage resonance between the CM choke inductance and inject capacitance, which manifests in the AEF loop gain as a pair of complex zeros.

Figure 9-3 highlights three specific RC branches: $R_{D1}$, $R_{D1A}$ and $C_{D1}$ form one branch from the INJ pin; $R_{D2}$ and $C_{D2}$ in series connect to GND; $R_{D3}$ and $C_{D3}$ in parallel connect to the inject capacitor.

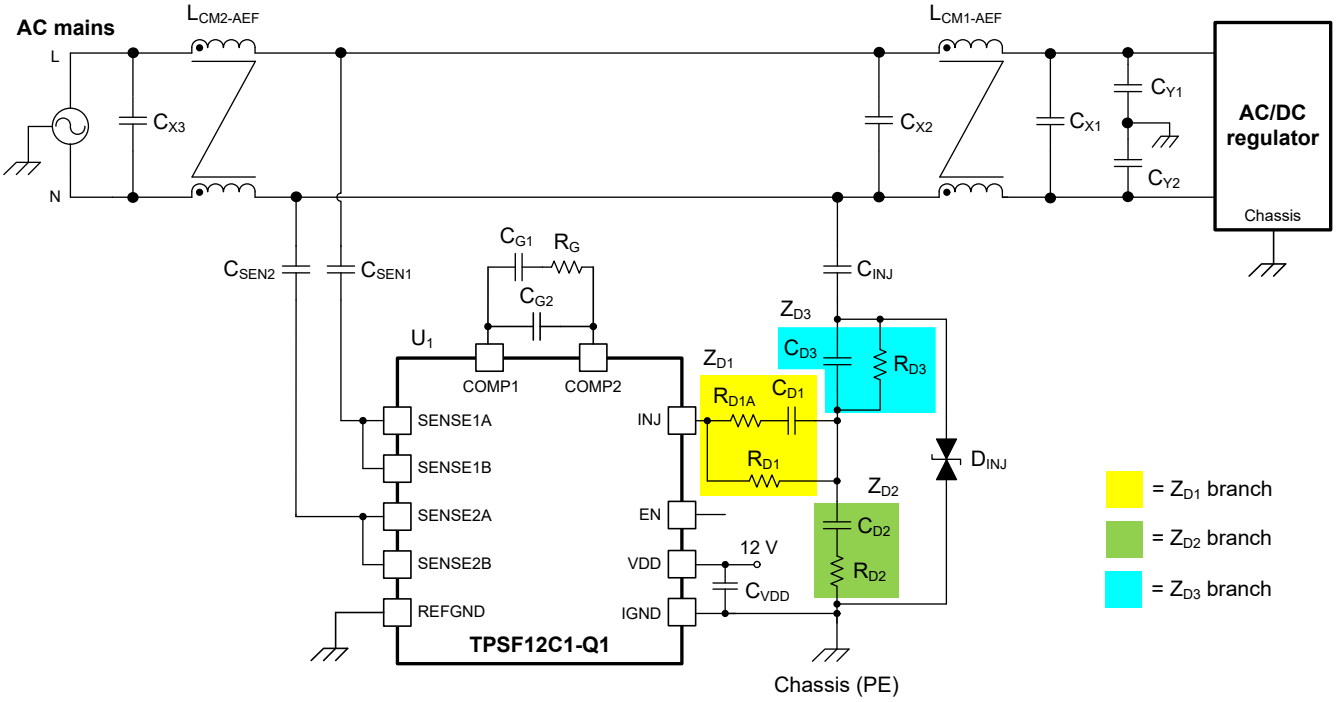


**Figure 9-3. Injection Network**

Based on the sensing and injection mechanism, the AEF circuit presents a very low impedance to CM noise. Given the three damping impedance branches highlighted in Figure 9-3, Equation 1 approximates the AEF impedance as:

$$Z_{AEF}(s) \approx \frac{Z_{INJ}(s) + Z_{D3}(s) + \left(Z_{D1}(s) \| Z_{D2}(s)\right)}{1 - G_{AEF}(s) \cdot \frac{Z_{D2}(s)}{Z_{D1}(s) + Z_{D2}(s)}} \quad (1)$$

where the term $G_{AEF}$ is the gain from the power lines to the INJ node (see the TPSF12C1-Q1 quickstart calculator for related detail).

Equation 1 shows that the impedance $Z_{INJ}$ appears in series with $Z_{D3}$ and a parallel combination of $Z_{D1}$ and $Z_{D2}$. Furthermore, the gain $G_{AEF}$ is reduced by the voltage divider ratio between $Z_{D2}$ and $Z_{D1}$. These effects combine to increase the effective impedance of the AEF and hence reduce its attenuation performance, thus illustrating a trade-off between performance and stability.

So while an injection network is needed for stability, it also adds impedance in series with inject capacitor, thus compromising EMI mitigation. As shown below, the user can minimize the impact on performance with careful and appropriate design.

Illustrated in Figure 9-4, at low frequencies in the range of 5 kHz to 50 kHz, components $R_{D1}$ and $C_{D2}$ provide compensation and $R_{D3}$ damps the effects of LC resonance. At higher frequencies (above 10 kHz), the dominant component impedance of each branch transitions to enable better attenuation performance:

- $R_{D1}$ transitions to $C_{D1}$
- $C_{D2}$ transitions to $R_{D2}$
- $R_{D3}$ transitions to $C_{D3}$

Finally, $C_{D1}$ transitions to $R_{D1A}$ if needed for phase margin of the AEF loop at high frequencies, typically above 100 kHz.

When viewed in a clockwise direction, Figure 9-4 shows these transitions in sequence as frequency increases.

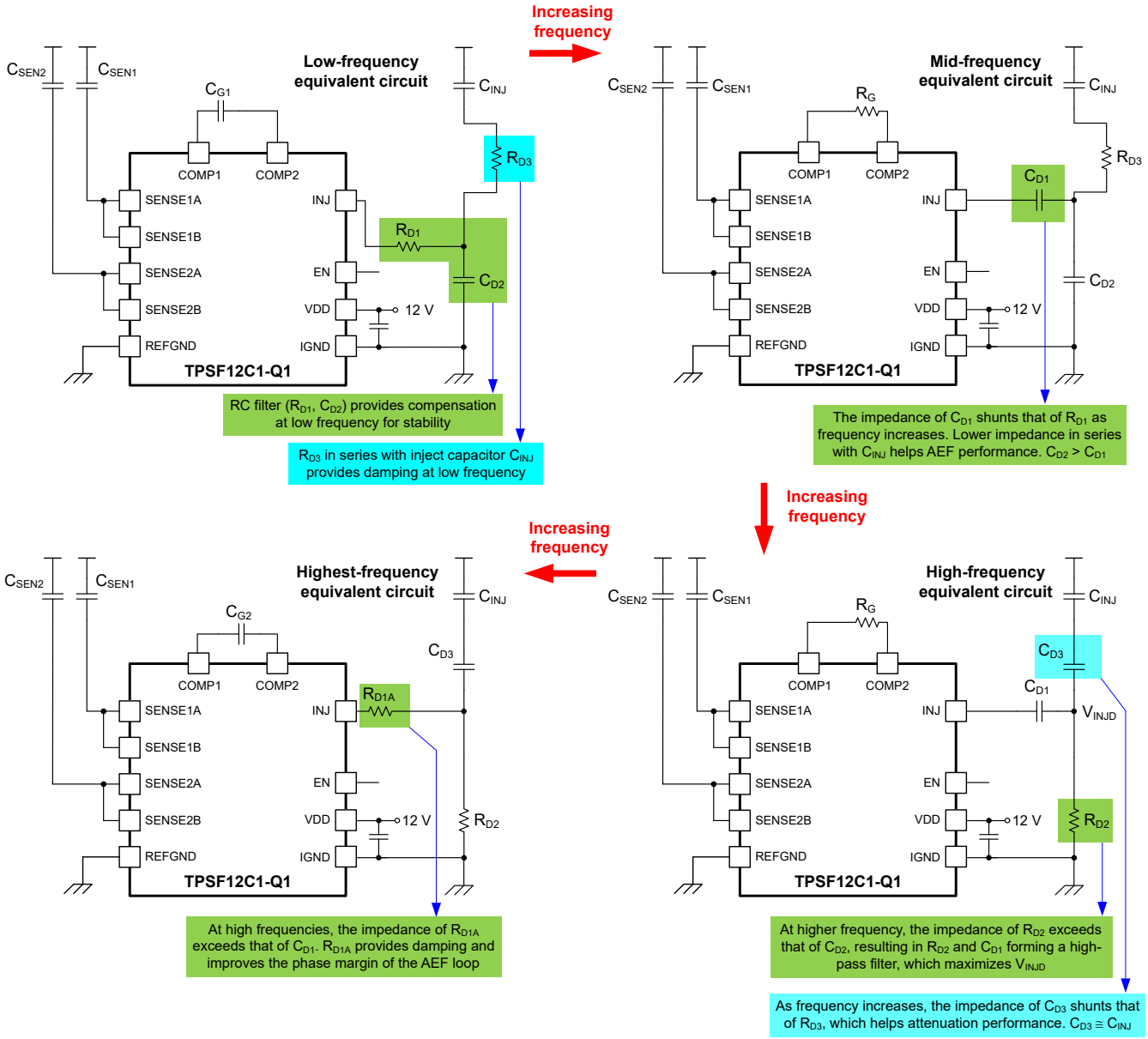


**Figure 9-4. Dominant Components of the Injection Network vs Frequency**

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Below are basic guidelines to select the component values for the injection network:

1. The undamped loop gain characteristic is likely to be unstable within the range of 5 kHz to 50 kHz, which, as mentioned previously, relates to an LC resonance between CM choke inductance and inject capacitance. Observe from circuit simulation – or by using the TPSF12C1-Q1 quickstart calculator – the frequency, $f_{LFstability}$, at which the phase crosses –180° with positive gain, indicating negative gain margin.
2. Choose a corner frequency with $R_{D1}$ and $C_{D2}$ equal to one fifth of the instability frequency:

$$\frac{1}{2\pi \cdot R_{D1} \cdot C_{D2}} = \frac{f_{LFstability}}{5} \tag{2}$$

Assigning $R_{D1}$ = 1 kΩ and assuming instablity at 35 kHz, use Equation 3 to find a value for the capacitance of $C_{D2}$:

$$C_{D2}\left[nF\right] = \frac{5000}{2\pi \cdot R_{D1}\left[k\Omega\right] \cdot f_{LFstability}\left[kHz\right]} = \frac{5000}{2\pi \cdot 1 \cdot 35} = 22nF \tag{3}$$

3. Select $C_{D1} < C_{D2}$, where a typical choice is $C_{D1} = C_{D2}/5$ = 4.7 nF.
4. Choose the resistance of $R_{D2}$ such that the $R_{D2}$, $C_{D2}$ corner frequency is equal to that of $R_{D1}$, $C_{D1}$:

$$R_{D2}\left[\Omega\right] = \frac{R_{D1}\left[\Omega\right] \cdot C_{D1}\left[nF\right]}{C_{D2}\left[nF\right]} = \frac{R_{D1}\left[\Omega\right]}{5} = \frac{1000}{5} = 200\,\Omega \tag{4}$$

5. Select the resistance of $R_{D3}$ to damp the resonance around the instability frequency, $f_{LFstability}$.
   - A typical choice for $R_{D3}$ is 500 Ω to 1 kΩ.
   - Assign $C_{D3}$ equal to $C_{INJ}$ or a suitable value such that the $R_{D3}$, $C_{D3}$ corner frequency is less than switching frequency.
   - A lower resistance for $R_{D3}$ results in more damping but at the penalty of reduced high-frequency attenuation (or forces a higher value for $C_{D3}$ to maintain the applicable corner frequency below the switching frequency).
6. Select a resistance for $R_{D1A}$ of 50 Ω to improve the phase margin of the AEF loop (if needed).

#### 9.2.1.2.5 Surge Protection

While the sense pins have internal clamp protection, the higher value of inject capacitance produces larger currents during surge events and thus requires external protection. Place a bidirectional TVS diode on the low-voltage side of the inject capacitor with standoff voltage of 24 V. Using the SOD-323 packaged device given in Table 9-2, clamping occurs at 40 V and 50 V with surge currents of 1 A and 8 A, respectively.

### *9.2.1.3 Application Curves*

Unless otherwise indicated, $V_{VDD}$ = $V_{EN}$ = 12 V.

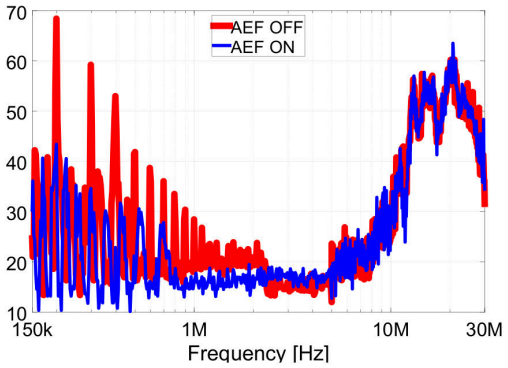


**Figure 9-5. EMI Mitigation Result with AEF On and Off (EN Tied High and Low)**

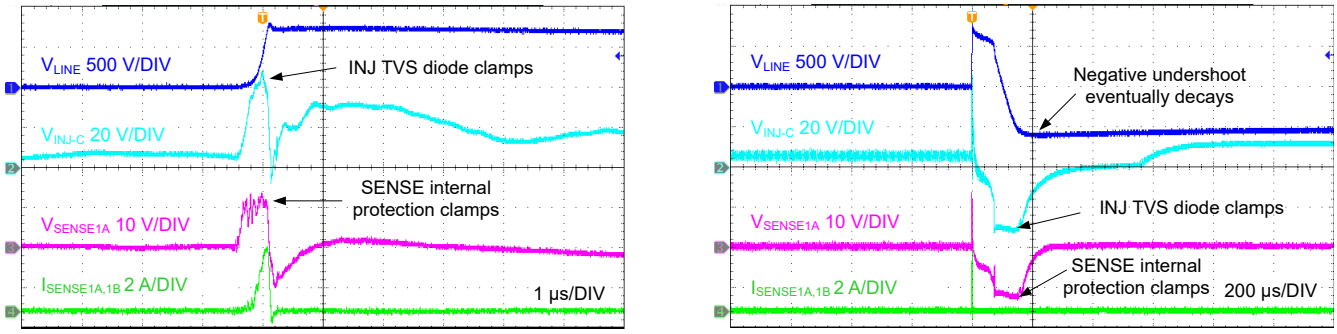


**Figure 9-6. IEC 61000-4-5 Positive Surge, 5-kV Single Strike – 1 µs/div (a), 200 µs/div (b)**

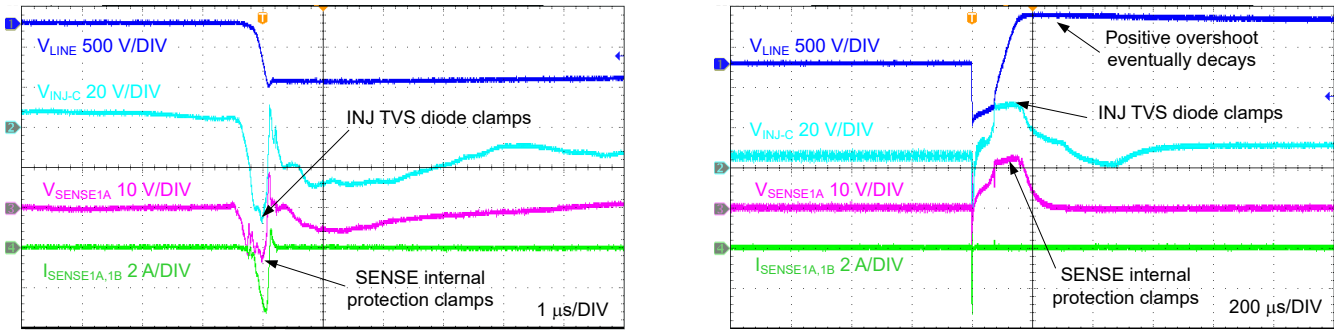


**Figure 9-7. IEC 61000-4-5 Negative Surge, 5-kV Single Strike – 1 µs/div (a), 200 µs/div (b)**

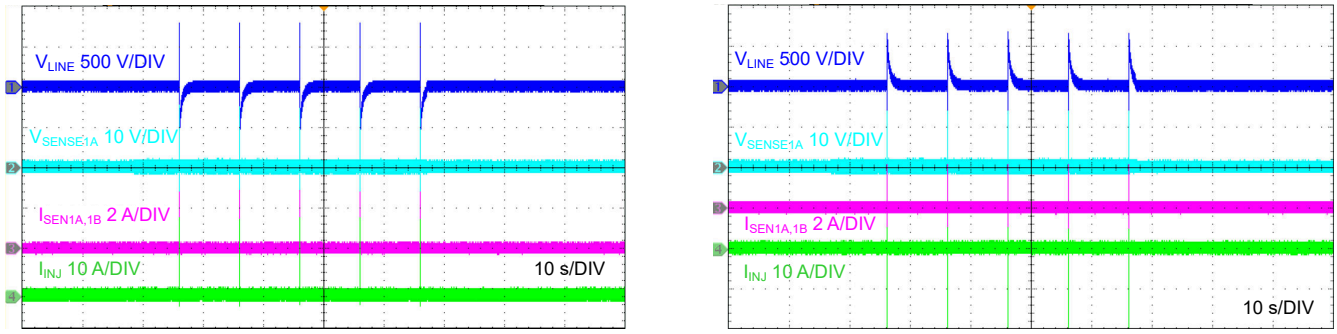


**Figure 9-8. IEC 61000-4-5 Surge, 5-kV Repetitive Strike at 10-Second Intervals – Positive (a), Negative (b)**

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## 9.3 Power Supply Recommendations

The TPSF12C1-Q1 AEF IC operates over a wide supply voltage range of 8 V to 16 V (typically 12 V) and is referenced to chassis ground of the system. The characteristics of this VDD bias supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the VDD supply must be capable of delivering the required supply current to the loaded AEF circuit.

The supply rail can already be present in the system or can be derived using a low-cost solution with an auxiliary winding from an isolated flyback regulator. Connect a 1-µF ceramic capacitor close to the VDD and IGND pins of the TPSF12C1-Q1. Ensure that the VDD ripple voltage is less than 50 mV peak-to-peak.

## 9.4 Layout

Proper PCB design and layout is important in active EMI circuits (where high regulator voltage and current slew rates exist) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the design depends to a large extent on PCB layout.

### 9.4.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimze AEF performance. Figure 9-9 and Figure 9-10 show a recommended layout for the TPSF12C1-Q1 with optimized placement and routing of the IC and small-signal components. Figure 9-11 shows an example filter board design with CM chokes, X-capacitors and Y-capacitors along with a receptacle for easy connection of an AEF daughterboard.

- *Route the sense lines S1 and S2 away from the INJ line.* Avoid coupling between sense and inject traces.
- *Place a ceramic capacitor close to the VDD and IGND pins.* Minimize the area of the loop to the VDD and IGND pins.
- *Place the compensation network copnponents close to the COMP1 and COMP2 pins.* Reduce noise sensitivity of the feedback compensation network path by placing the $R_G$-$C_{G1}$-$C_{G2}$ network close to the COMP pins. COMP2 is the inverting input to the AEF anplifier and represents a high-impedance node sensitive to noise.
- *Provide enough PCB area for proper heatsinking.* Use sufficient copper area to acheive a low thermal impedance. Provide adequate heatsinking for the TPSF12C1-Q1 to keep the junction temperature below 150°C. A top-side ground plane is an important heat-dissipating area. Use several heat-sinking vias to connect IGND (pin 14) and REFGND (pin 9) to the PCB ground plane.

### 9.4.2 Layout Example

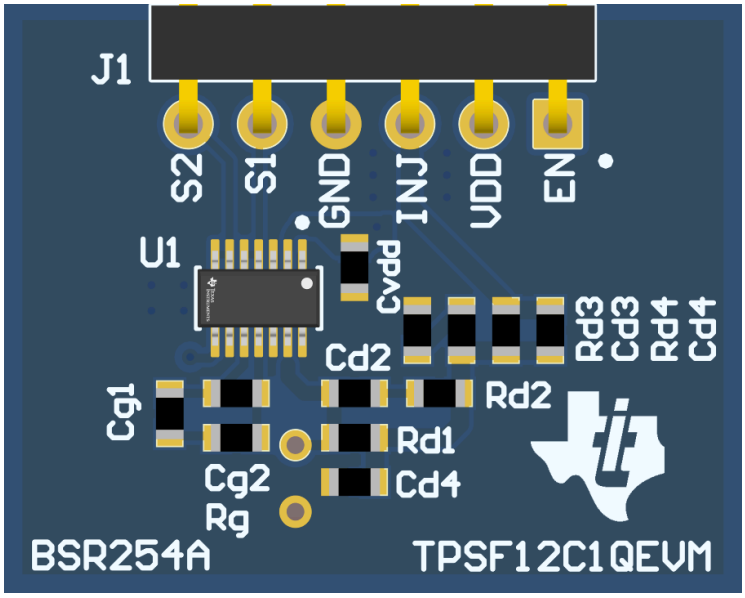


**Figure 9-9. Typical Layout**

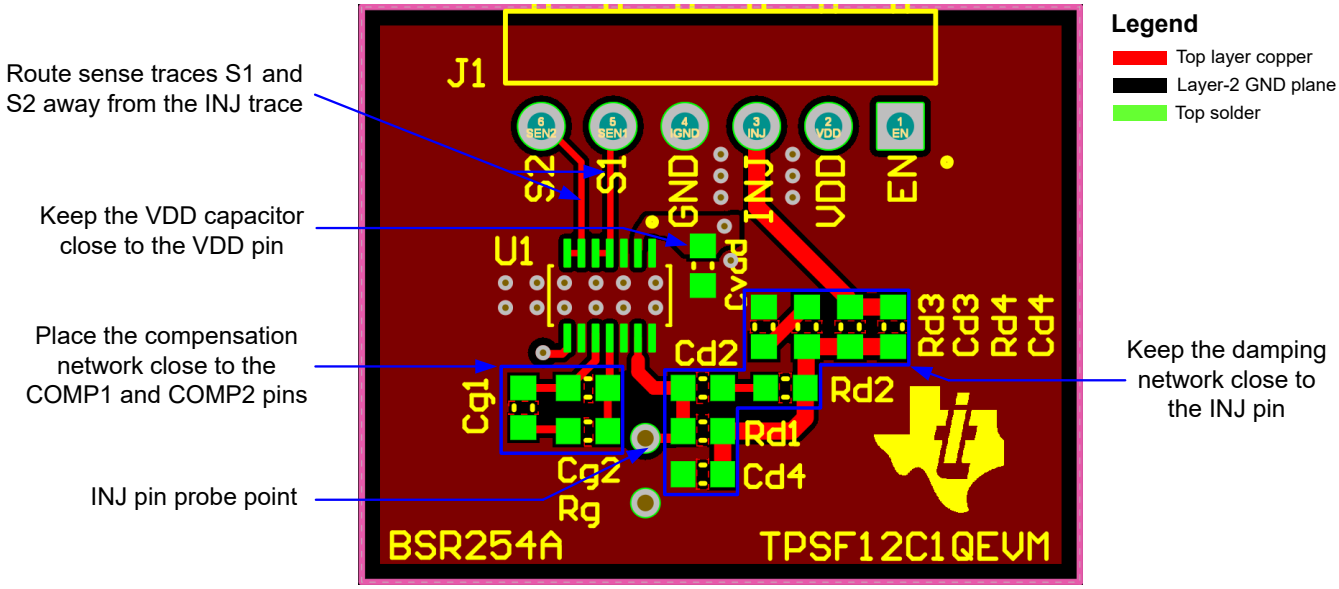


**Figure 9-10. Typical Top-Layer Design**

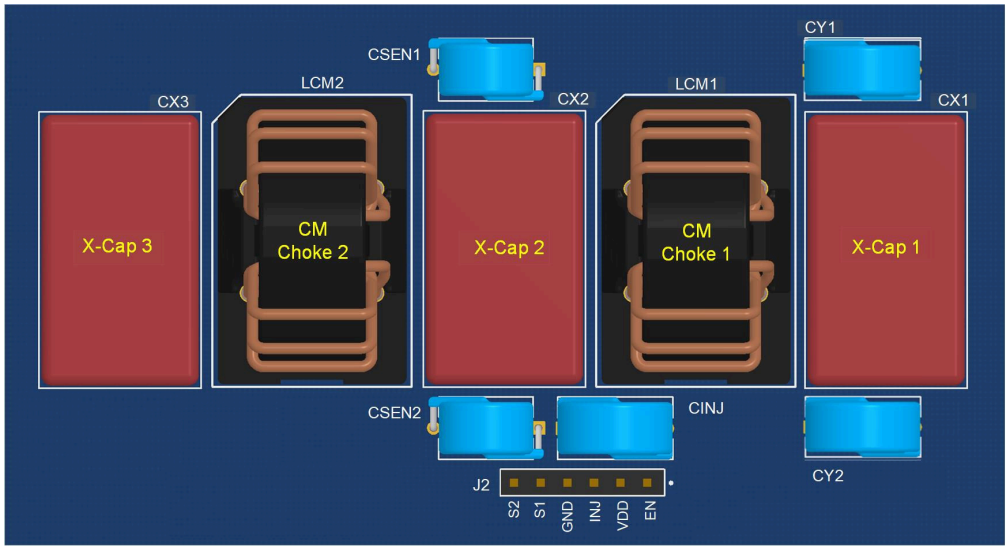


**Figure 9-11. Typical Filter Board Design**

ADVANCE INFORMATION

# 10 Device and Documentation Support

## 10.1 Device Support

### 10.1.1 Third-Party Products Disclaimer

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### 10.1.2 Development Support

All AEF devices from the family shown in Table 10-1 are rated for an ambient temperature up to 105°C and are functional safety capable.

**Table 10-1. Common-mode AEF IC Family**

| DEVICE | ORDERABLE PART NUMBER | PHASES | GRADE | JUNCTION TEMPERATURE RANGE |
|---|---|---|---|---|
| TPSF12C1-Q1 | TPSF12C1QDYYRQ1 | 1 | Automotive | –40°C to 150°C |
| TPSF12C3-Q1 | TPSF12C3QDYYRQ1 | 3 | Automotive | –40°C to 150°C |
| TPSF12C1 | TPSF12C1DYYR | 1 | Commercial | –40°C to 150°C |
| TPSF12C3 | TPSF12C3DYYR | 3 | Commerical | –40°C to 150°C |

For development support see the following:

- TPSF12C1-Q1 *Quickstart calculator*
- TPSF12C1-Q1 EVM *Altium layout source files*
- TPSF12C1-Q1 PSPICE for TI and SIMPLIS *simulation models*
- For TI's reference design library, visit *TI Reference Design library*
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*
- TI Reference Designs:
  - *Automotive wide $V_{IN}$ front-end reference design for digital cockpit processing units*
- Technical Articles:
  - Texas Instruments, *How to reduce EMI and shrink power-supply size with an integrated active EMI filter*
  - Texas Instruments, *How device-level features and package options can help minimize EMI In automotive designs*
  - Texas Instruments, *How to use slew rate for EMI control*
- White Papers:
  - Texas Instruments, *Valuing Wide $V_{IN}$, Low-EMI Synchronous Buck Circuits for Cost-Effective, Demanding Applications*
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
- To view a related device of this product, see the TPSF12C3-Q1 three-phase active EMI filter for common-mode EMI mitigation

## 10.2 Documentation Support

### 10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* ADJ article
- Texas Instruments, *Designing High Performance, Low-EMI, Automotive Power Supplies* application report
- Texas Instruments, *EMI Filter Components And Their Nonidealities For Automotive DC/DC Regulators* technical brief

### 10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.5 Trademarks

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### 10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

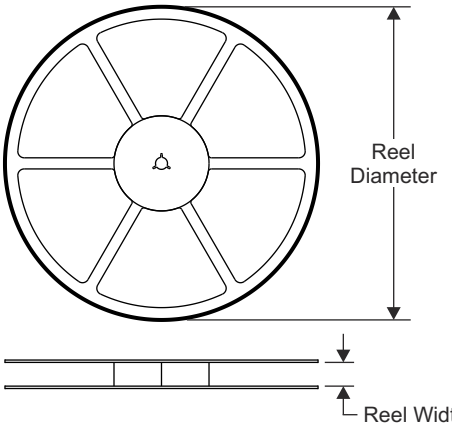
## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

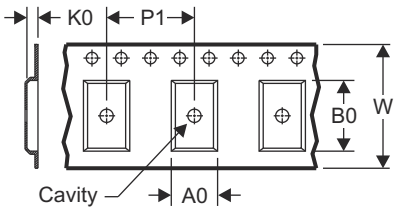
ADVANCE INFORMATION

## 11.1 Tape and Reel Information

**REEL DIMENSIONS**

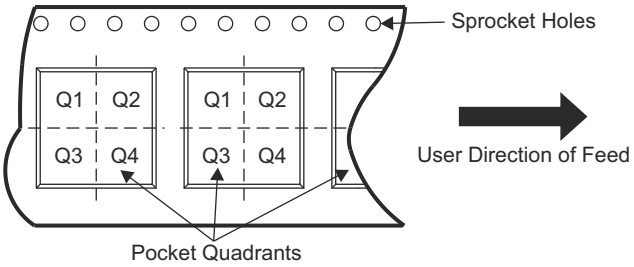



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

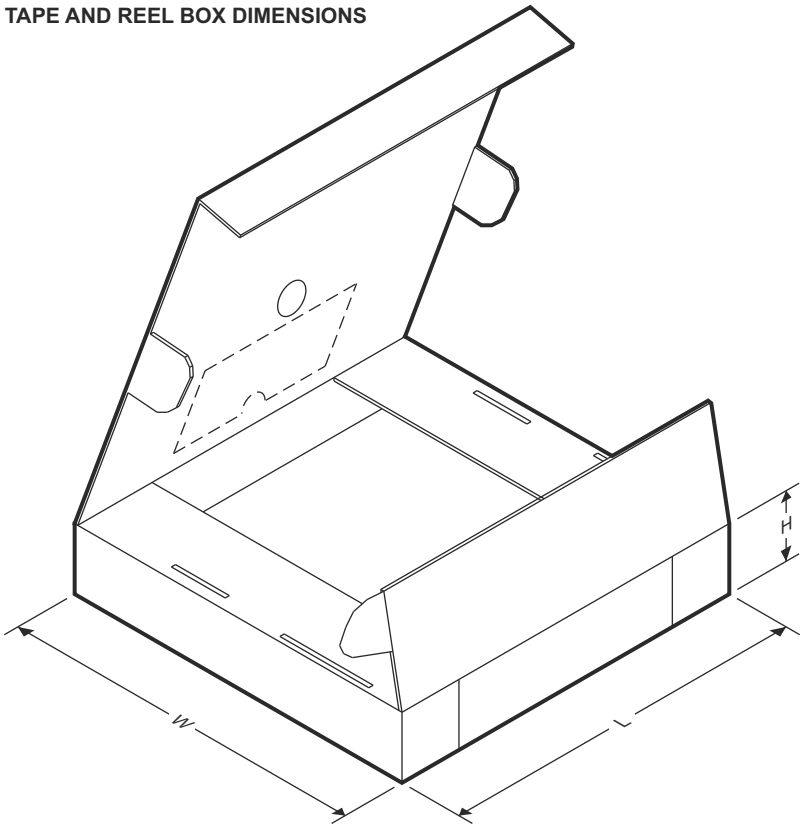
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPSF12C1QDYYRQ1 | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |

ADVANCE INFORMATION

**TAPE AND REEL BOX DIMENSIONS**




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPSF12C1QDYYRQ1 | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |

ADVANCE INFORMATION

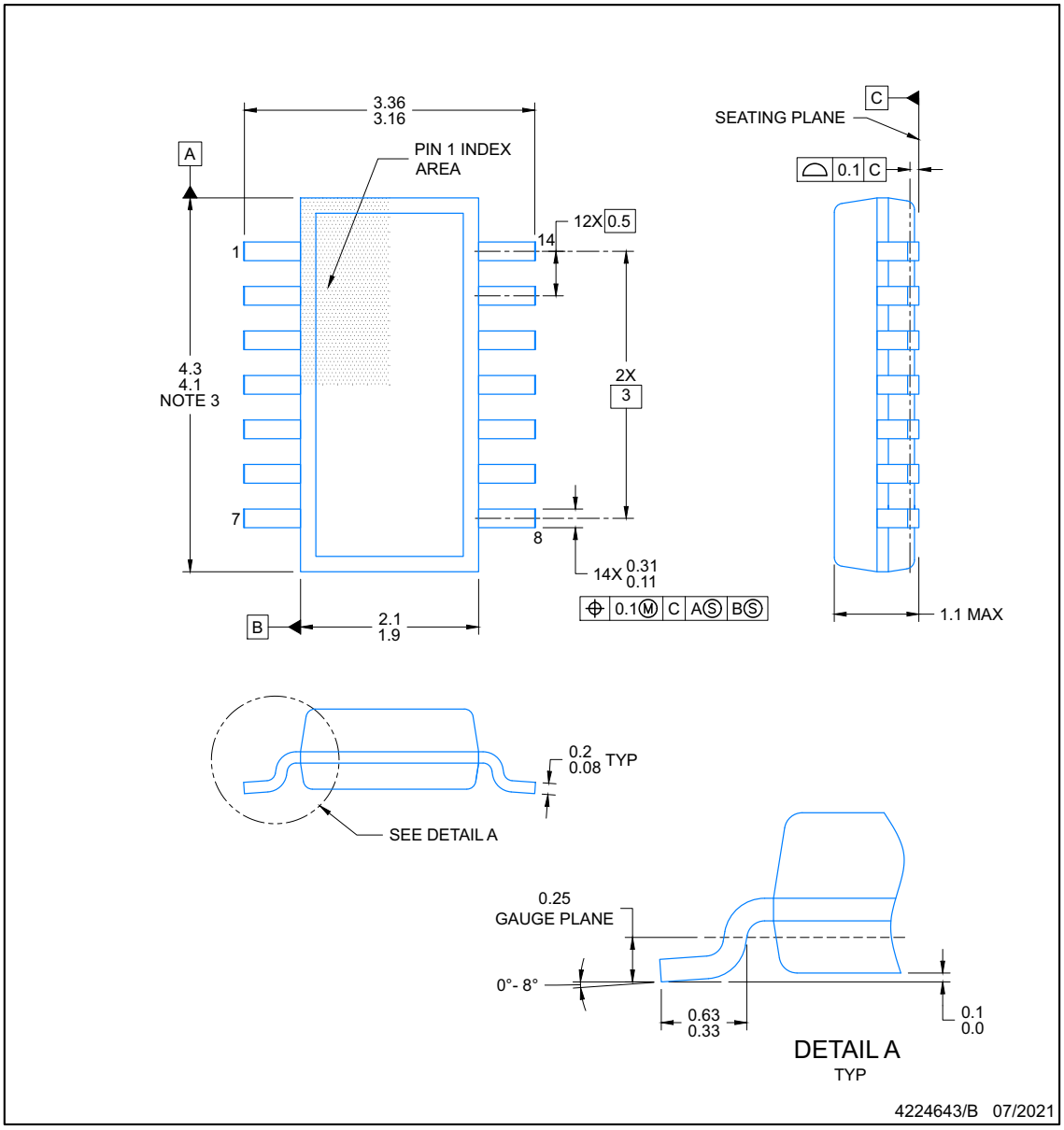
ADVANCE INFORMATION

# PACKAGE OUTLINE

## DYY0014A

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE




NOTES:

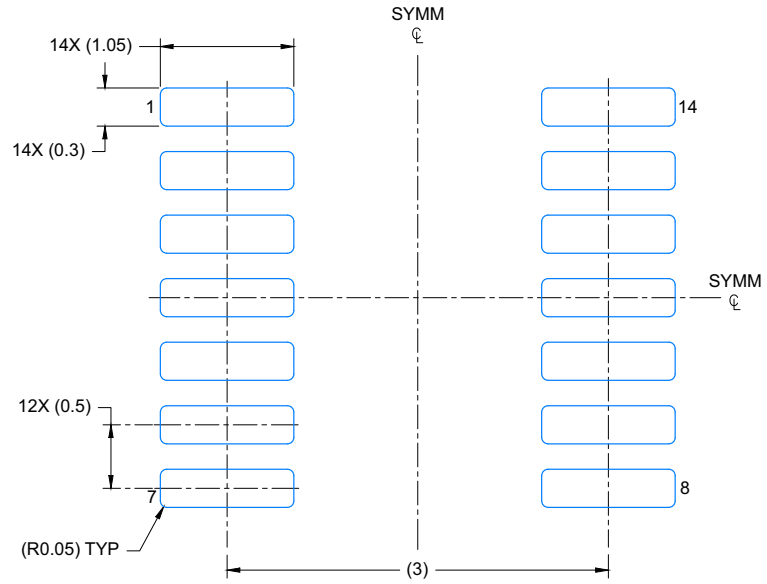
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

# EXAMPLE BOARD LAYOUT

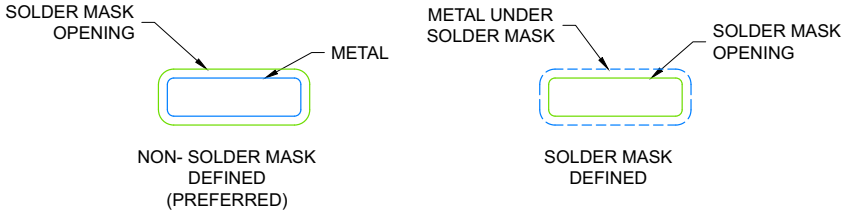
## DYY0014A

### SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

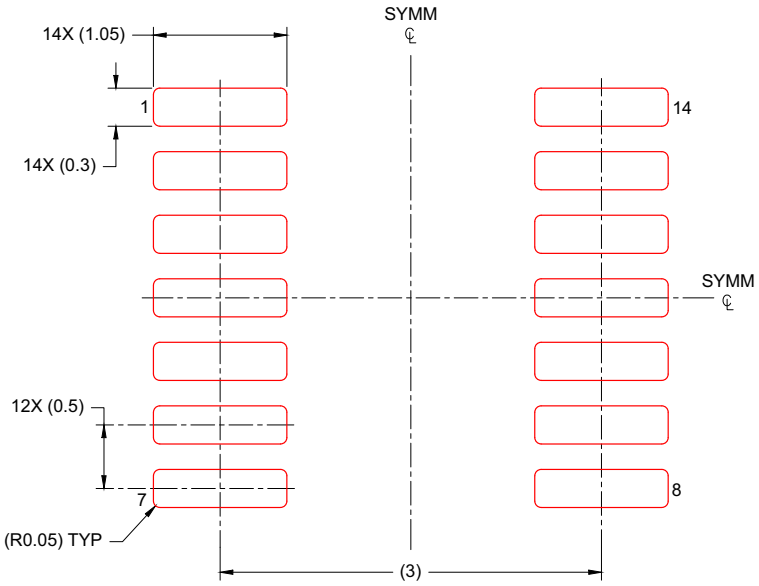
ADVANCE INFORMATION

ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

**DYY0014A** — **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P12C1QDYYRQ1 | ACTIVE | SOT-23-THIN | DYY | 14 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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