TRS3232E 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ±15-kV IEC ESD Protection In Small Package

1 Features

- ESD protection for RS-232 bus pins
  - ±15 kV (HBM)
  - ±8 kV (IEC61000-4-2, Contact discharge)
  - ±15 kV (IEC61000-4-2, Air-gap discharge)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU V.28 standards
- Operates with 3-V to 5.5-V V_{CC} supply
  - Interoperable with RS-232 down to 2.7-V V_{CC}
- Operates up to 250 kbps
- Two drivers and two receivers
- Low supply current: 300 µA (typical)
- External capacitors: 4 × 0.1 µF
- Accepts 5-V logic input with 3.3-V supply
- Available in near chip-scale package (QFN-16, 3 mm x 3 mm), 85% smaller than SOIC-16
- Pin compatible to alternative high-speed devices (1 Mbps)
  - SN65C3232E (–40°C to +85°C)
  - SN75C3232E (0°C to 70°C)

2 Applications

- Industrial PCs
- Wired networking
- Data center and enterprise computing
- Battery-powered systems
- Notebooks
- Palmtop PCs
- Hand-held equipment

3 Description

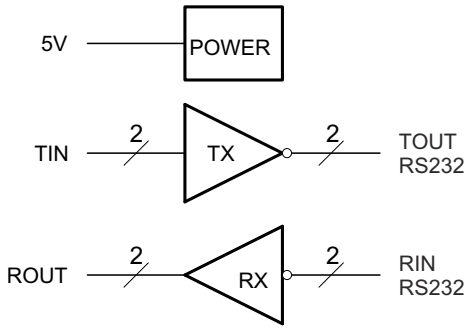
The TRS3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND).

The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbps and a maximum of 30-V/µs driver output slew rate.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRS3232E	SOIC (D) 16	9.90 mm × 3.91 mm
	SSOP (DB) 16	6.20 mm × 5.30 mm
	SOIC (DW) 16	10.30 mm × 7.50 mm
	TSSOP (PW) 16	5.00 mm × 4.40 mm
	VQFN (RGT) 16	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2021) to Revision D (June 2021)	Page
• Added *Applications*: Industrial PCs, Wired networking, and Data center and enterprise computing	1
• Changed the table note in the *ESD Ratings - IEC Specifications* to make it applicable to D, DB and PW packages.	4
• Changed the thermal paramater values for D, DB and PW packages in the *Thermal Information* table	5

Changes from Revision B (October 2017) to Revision C (June 2021)	Page
• Added RGT package to the *Device Information*	1
• Added the RGT *Pin Configuration*	3
• Added the *ESD Ratings - IEC Specifications*	4
• Added RGT to the *Thermal Information*	5
• Added RGT package to the *Switching Characteristics*	7
• Changed the capacitor value From: 1 µf To: 0.1 µf in the *Layout Diagram*	15

Changes from Revision A (July 2015) to Revision B (October 2017)	Page
• Added Feature: Interoperable with RS-232 down to 2.7-V V_{CC}	1
• Added Driver Output Voltage vs. Supply Voltage, Both Drivers Loaded	0

Changes from Revision * (April 2007) to Revision A (July 2015)	Page
• Deleted *Ordering Information* table	1
• Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

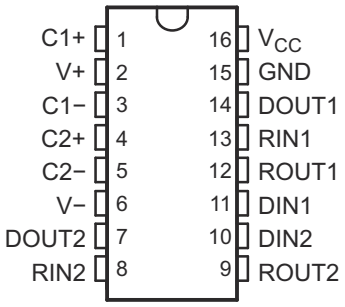


Figure 5-1. D, DW, DB or PW Package, 16-Pin SOIC, SSOP or TSSOP, Top View

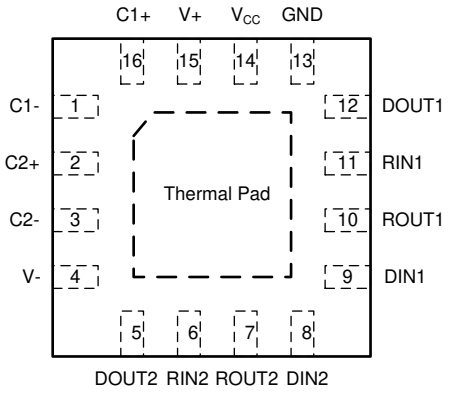


Figure 5-2. RGT package, 16 Pin VQFN, Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.	RGT		
C1+	1	16	—	Positive lead of C1 capacitor
C1–	3	1	—	Negative lead of C1 capacitor
C2+	4	2	—	Positive lead of C2 capacitor
C2–	5	3	—	Negative lead of C2 capacitor
DIN1	11	9	I	Logic data input (from UART)
DIN2	10	8	I	Logic data input (from UART)
DOUT2	7	5	O	RS232 line data output (to remote RS232 system)
DOUT1	14	12	O	RS232 line data output (to remote RS232 system)
GND	15	13	—	Ground
RIN1	13	11	I	RS232 line data input (from remote RS232 system)
RIN2	8	6	I	RS232 line data input (from remote RS232 system)
ROUT2	9	7	O	Logic data output (to UART)
ROUT1	12	10	O	Logic data output (to UART)
V+	2	15	O	Positive charge pump output for storage capacitor only
V–	6	4	O	Negative charge pump output for storage capacitor only
V_{CC}	16	14	—	Supply voltage, connect to external 3-V to 5.5-V power supply
Thermal Pad		Yes	—	Thermal pad for improving heat dissipation. Can be connected to GND or left floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
V+	Positive output supply voltage(2)		–0.3	7	V
V–	Negative output supply voltage(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage	Drivers	–0.3	6	V
		Receivers	–25	25	V
V_O	Output voltage	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	V
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except RIN1, RIN2, DOUT1 and DOUT2	±2000	V
			Pins RIN1, RIN2, DOUT1 and DOUT2	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, Contact Discharge(1)	Pins RIN1, RIN2, DOUT1, DOUT2	±8000	V
		IEC 61000-4-2, Air-Gap Discharge(1)	Pins RIN1, RIN2, DOUT1, DOUT2	±15000	

(1) For RGT, D, DB and PW packages only: Minimum of 1-µF capacitor between VCC and GND is required to meet the specified IEC 61000-4-2 rating.

6.4 Recommended Operating Conditions

See Typical Operating Circuit and Capacitor Values.(1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2		5.5	V
			V_{CC} = 5 V	2.4		5.5	
V_{IL}	Driver low-level input voltage	DIN		0		0.8	V
V_I	Receiver input voltage	RIN		–25		25	V
T_A	Operating free-air temperature		TRS3232EC	0		70	°C
			TRS3232EI	–40		85	

(1) C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.5 Thermal Information

THERMAL METRIC(1)		TRS3232E					UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	RGT (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.2	85.9	72.3	103.1	48.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	39.0	43.1	33.5	49.2	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	44.5	37.1	54.8	23.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	10.1	7.5	12.0	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	44.1	37.1	54.1	23.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	9.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.7 Electrical Characteristics — Driver

over operating free-air temperature range (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS} (3)	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V				
r_O	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values).(2)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.3		V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

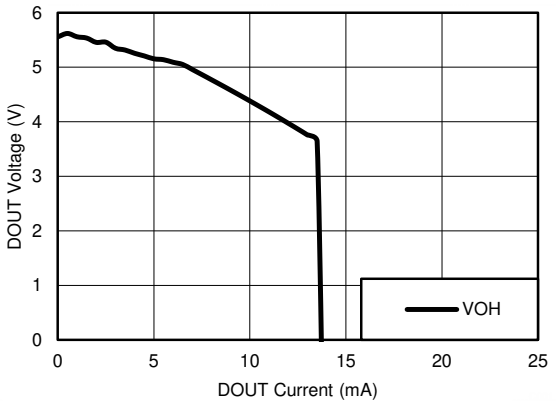
6.9 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Typical Operating Circuit and Capacitor Values)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ, C_L = 1000 pF, see Driver Slew Rate One DOUT switching,	RGT package	250	500		kbps
			D, DB, DW and PW packages	150	250		
$t_{sk(p)}$	Driver pulse skew(3)	R_L = 3 kΩ, C_L = 1000 pF, V_{CC} = 5 V Driver Pulse Skew	RGT package		50		ns
		R_L = 3 kΩ to 7 kΩ, C_L = 150 pF to 2500 pF see Driver Pulse Skew	D, DB, DW and PW packages		300		
SR(tr)	Driver slew rate, transition region (see Driver Slew Rate)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	
t_{PLH}	Receiver propagation delay time, low- to high-level output	C_L = 150 pF, see Receiver Propagation Delay Times	RGT package		90		ns
			D, DB, DW and PW packages		300		
t_{PHL}	Receiver propagation delay time, high- to low-level output	C_L = 150 pF, see Receiver Propagation Delay Times	RGT package		100		ns
			D, DB, DW and PW packages		300		
$t_{sk(p)}$	Receiver pulse skew(3)	RGT package			20		ns
		D, DB, DW and PW packages			300		

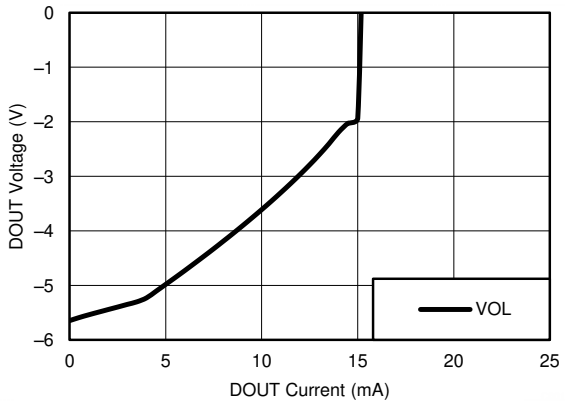
(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

Typical Characteristics



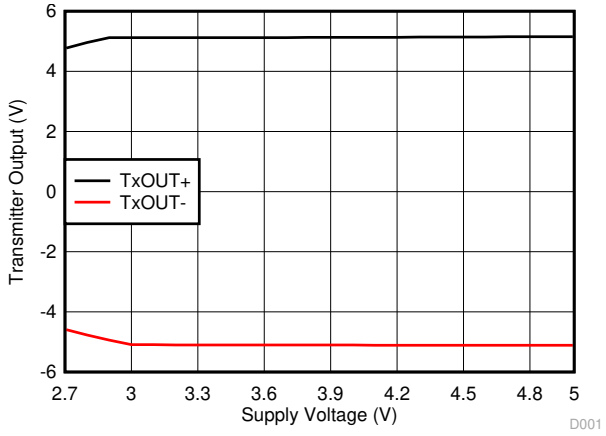
V_{CC} = 3.3 V

Figure 6-1. DOUT V_{OH} vs Load Current, Both Drivers Loaded



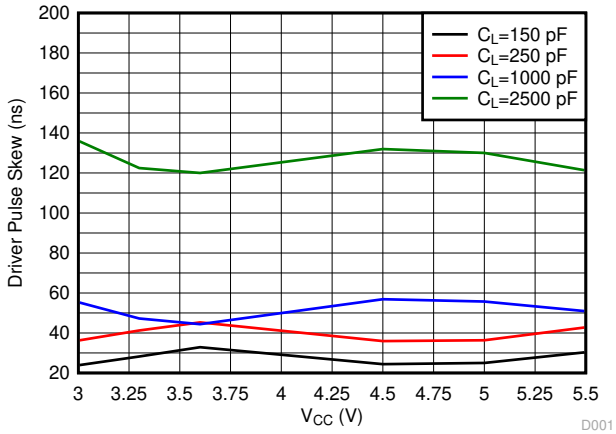
V_{CC} = 3.3 V

Figure 6-2. DOUT V_{OL} vs Load Current, Both Drivers Loaded



TX1 at 250 kbps TX2 at 15.6 kbps
Both TX loaded 3 kΩ and 1000 pF

Figure 6-3. Driver Output Voltage vs. Supply Voltage, Both Drivers Loaded



D001_tx_skew.grf

Figure 6-4. Driver Pulse Skew (RGT Package)

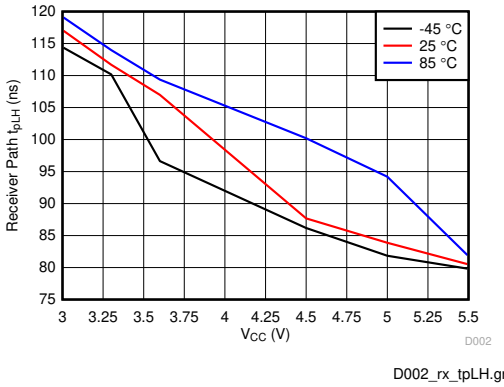


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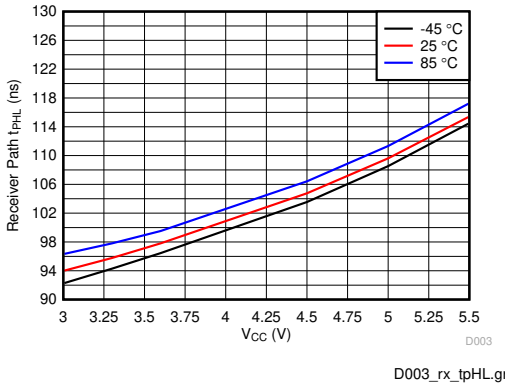
Figure 6-5. Receiver Path Low-to-High Propagation Delay (RGT Package)



D003_rx_tpHL.grf

Figure 6-6. Receiver Path High-to-Low Propagation Delay (RGT Package)

Typical Characteristics

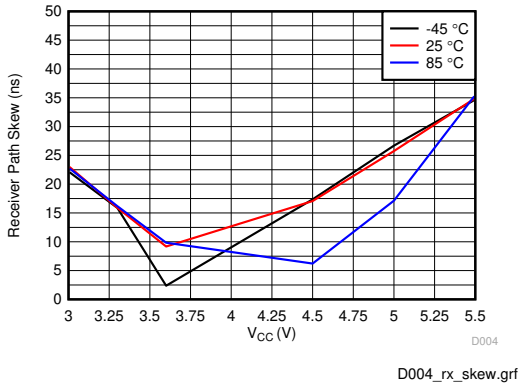
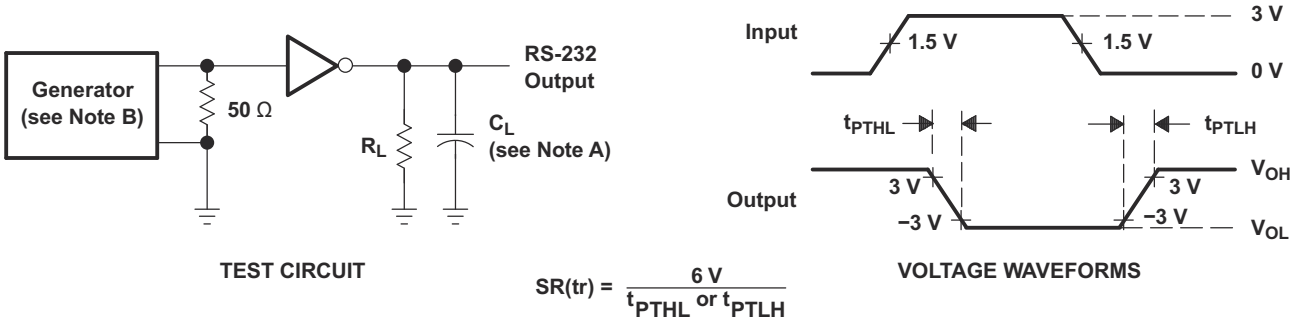


Figure 6-7. Receiver Path Skew ($|t_{pHL}-t_{pLH}|$) (RGT Package)

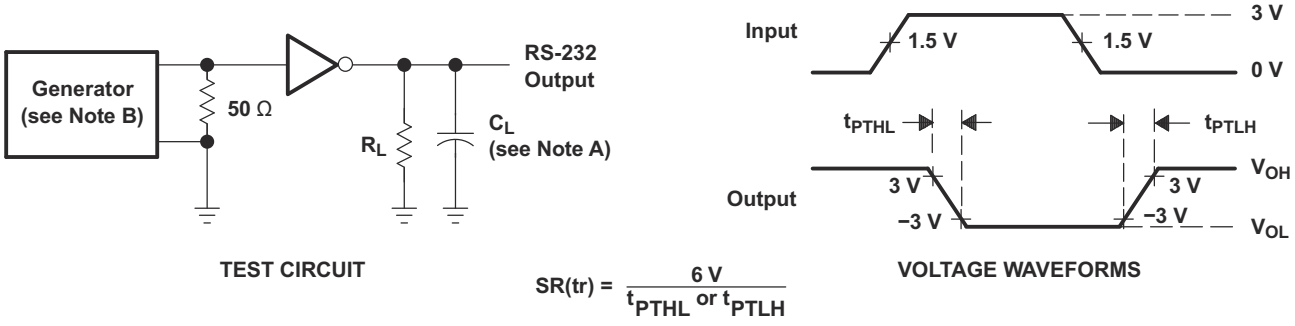
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns

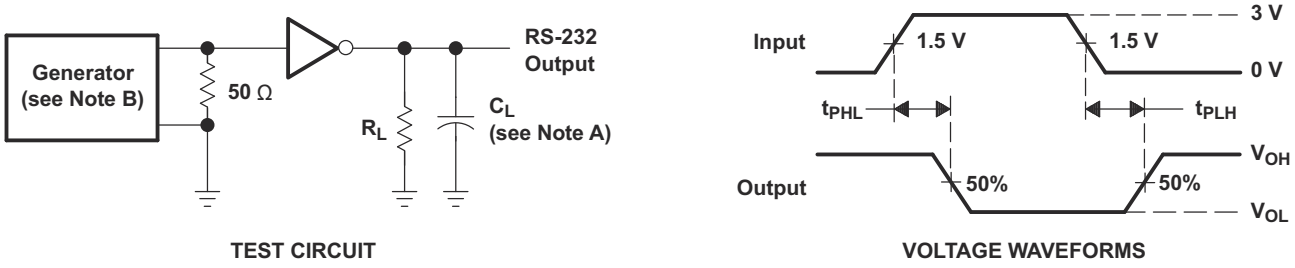
Figure 7-1. Driver Slew Rate



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns

Figure 7-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns

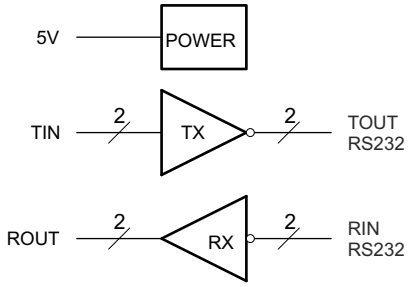
Figure 7-3. Receiver Propagation Delay Times

8 Detailed Description

8.1 Overview

The TRS3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbps and a maximum of 30-V/µs driver output slew rate. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.4 Device Functional Modes

Table 8-1 and Table 8-2 list the functional modes of the drivers and receivers of TRS3232E.

Table 8-1. Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 8-2. Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

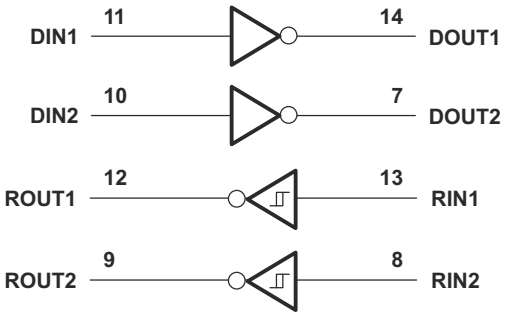


Figure 8-1. Logic Diagram

8.4.1 V_{CC} Powered by 3 V to 5.5 V

The device is in normal operation.

8.4.2 V_{CC} Unpowered, V_{CC} = 0 V

When TRS3232E is unpowered, it can be safely connected to an active remote RS232 device.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

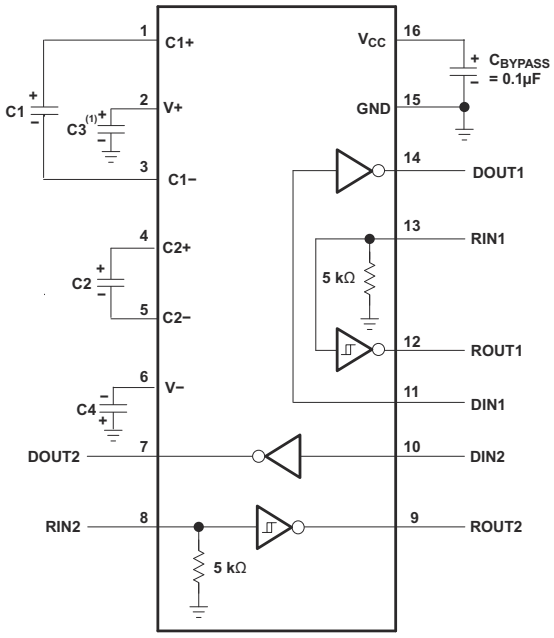
9.1 Application Information

The TRS3232E interfaces logic lines from a UART or microcontroller to the voltage and current levels needed for RS232 communication. The TIN inputs will accept 5-V logic with 3.3-V V_{CC} supply. All baud rates up to 250-kbps are supported.

It is important to use the correct capacitors for the VCC voltage. This will reduce ripple voltage on the TOUT outputs. If only one driver is needed, the unused driver input should be connected to V_{CC} or ground.

9.2 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable. For proper operation, add capacitors as shown in Table 9-1.



A. C3 can be connected to V_{CC} or GND
Resistor values shown are nominal.
Nonpolorized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 9-1. Typical Operating Circuit and Capacitor Values

Table 9-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V ± 5.5 V	0.1 µF	0.47 µF

9.2.1 Design Requirements

The recommended V_{CC} is 3.3 V or 5 V. 3 V to 5.5 V is also possible.

The maximum recommended bit rate is 250 kbps.

9.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

Figure 9-2 curves are for 3.3-V VCC and 250-kbps alternative bit data stream.

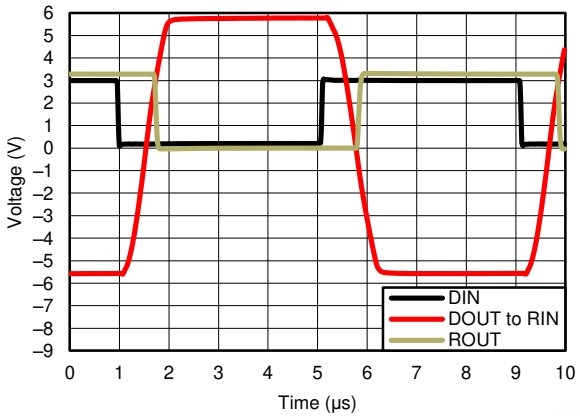


Figure 9-2. 250 kbps Driver to Receiver Loopback Timing Waveform, V_{CC}= 3.3 V

10 Power Supply Recommendations

The supply voltage, V_{CC}, should be between 3 V and 5.5 V. Select the values of the charge-pump capacitors using Table 9-1.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

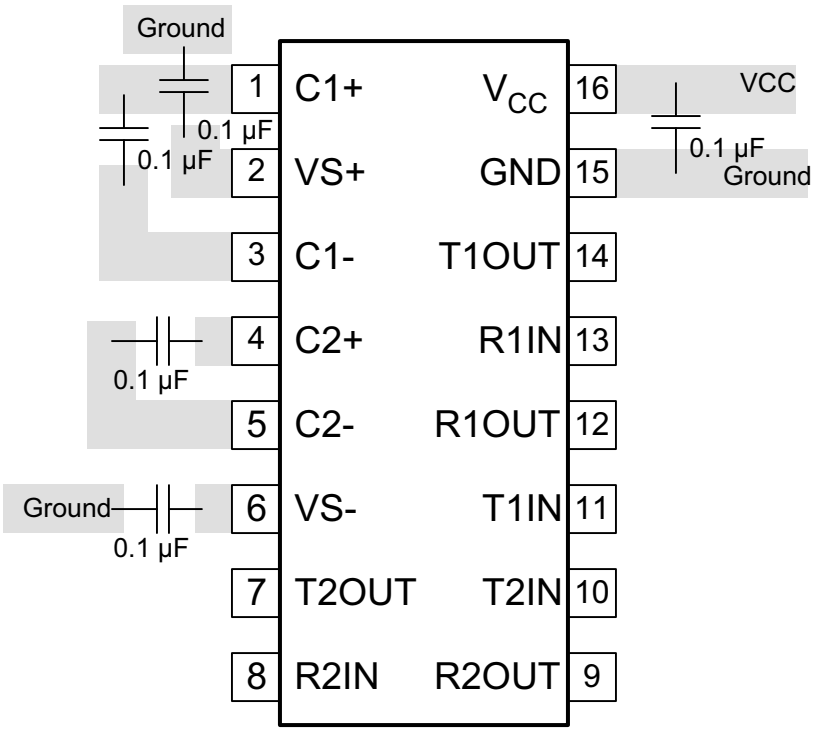


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3232ECDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC	Samples
TRS3232ECDW	NRND	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC	
TRS3232ECDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC	Samples
TRS3232ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32EC	Samples
TRS3232EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	Samples
TRS3232EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI	Samples
TRS3232EIDW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI	
TRS3232EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	Samples
TRS3232EIPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	Samples
TRS3232EIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3232	Samples
TRSF3232ECDWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRSF3232EC	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TRS3232E :

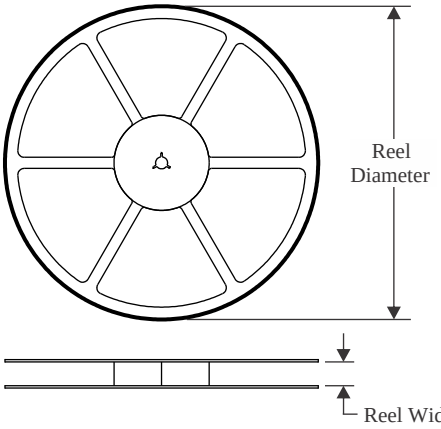
- Automotive : TRS3232E-Q1

NOTE: Qualified Version Definitions:

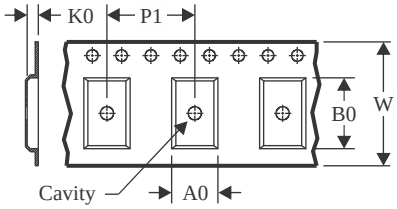
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

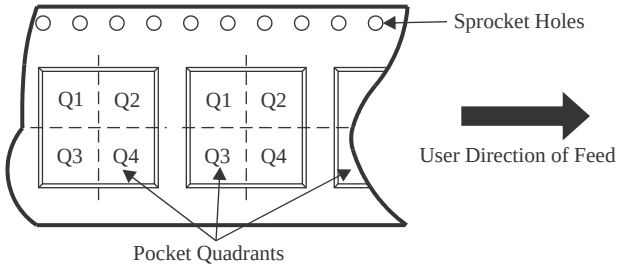


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

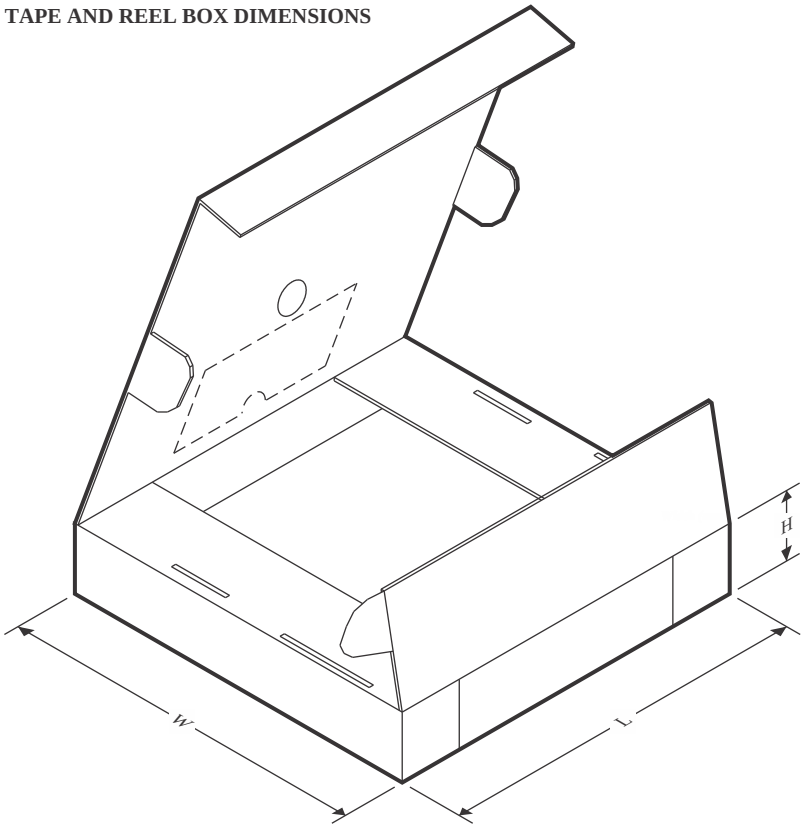
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRS3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TRSF3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

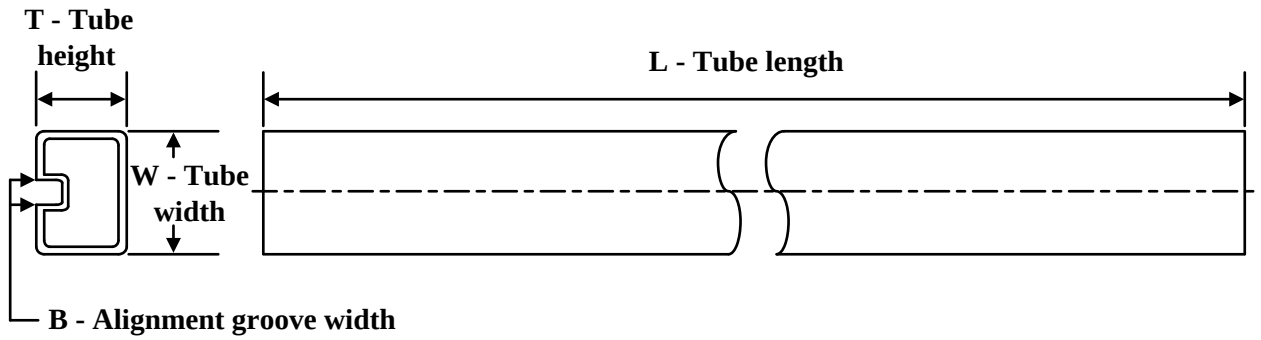
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3232ECDR	SOIC	D	16	2500	356.0	356.0	35.0
TRS3232ECDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRS3232ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRS3232ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS3232EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRS3232EIDR	SOIC	D	16	2500	356.0	356.0	35.0
TRS3232EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS3232EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRS3232EIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TRSF3232ECDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE

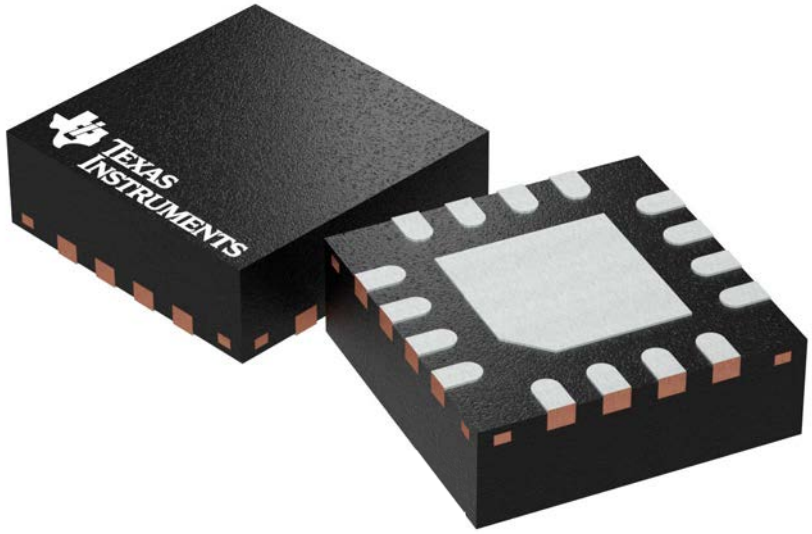


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TRS3232ECDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TRS3232EIDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



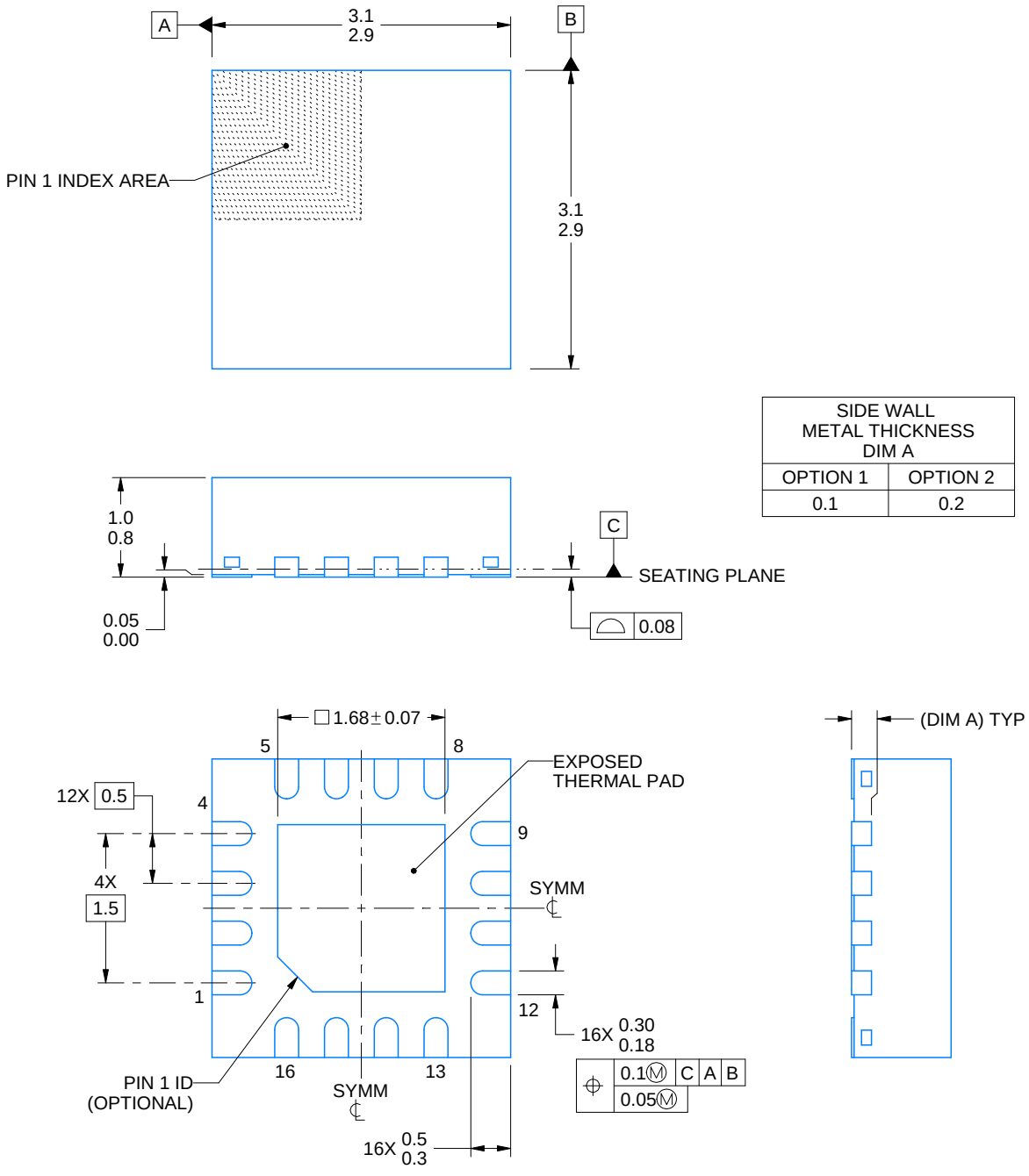
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

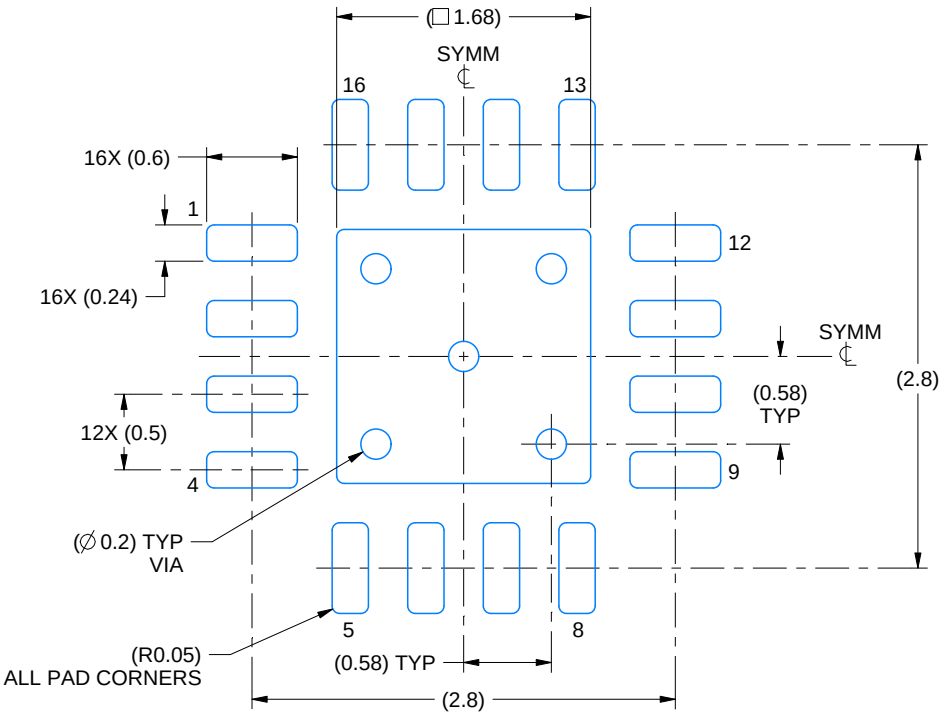
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

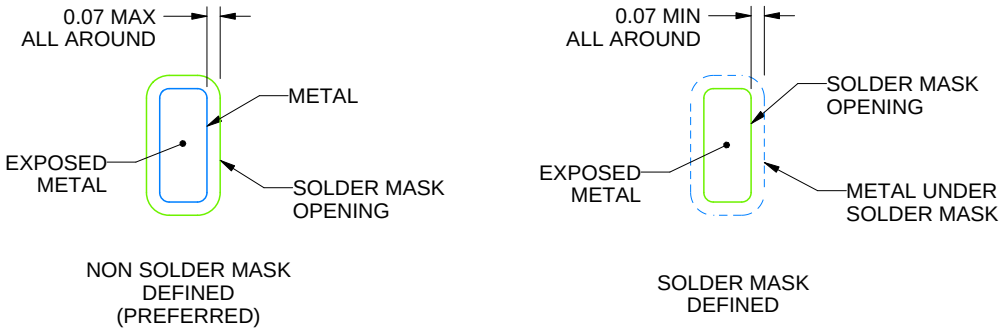


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

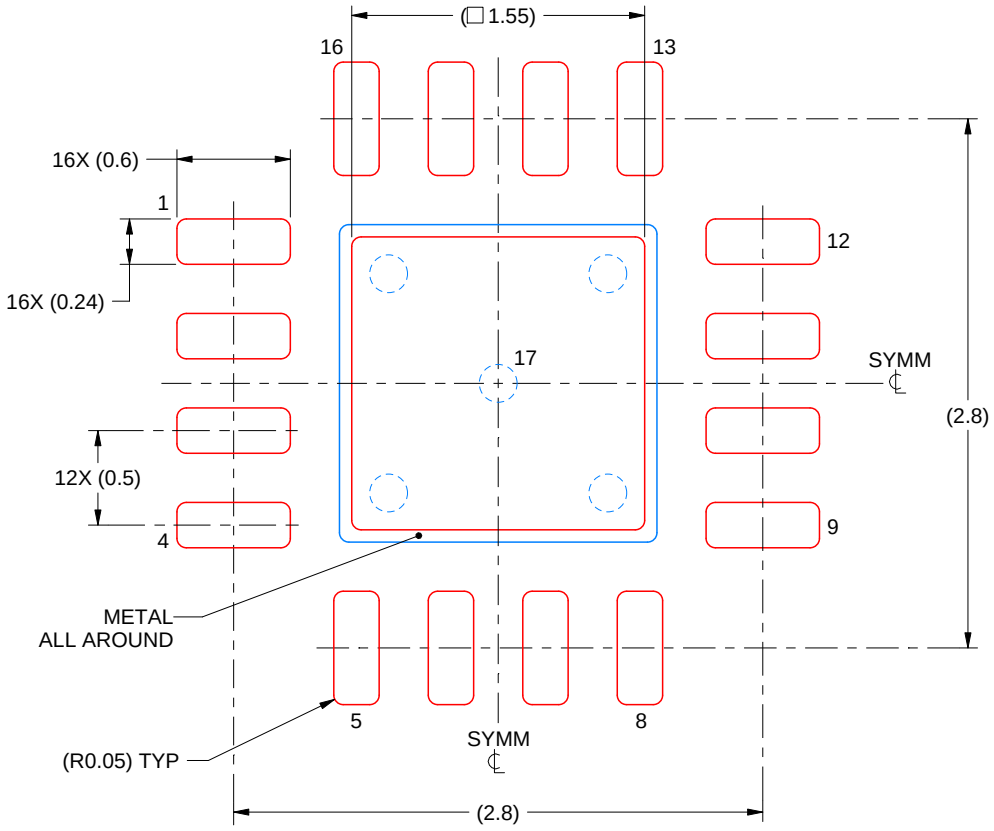


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

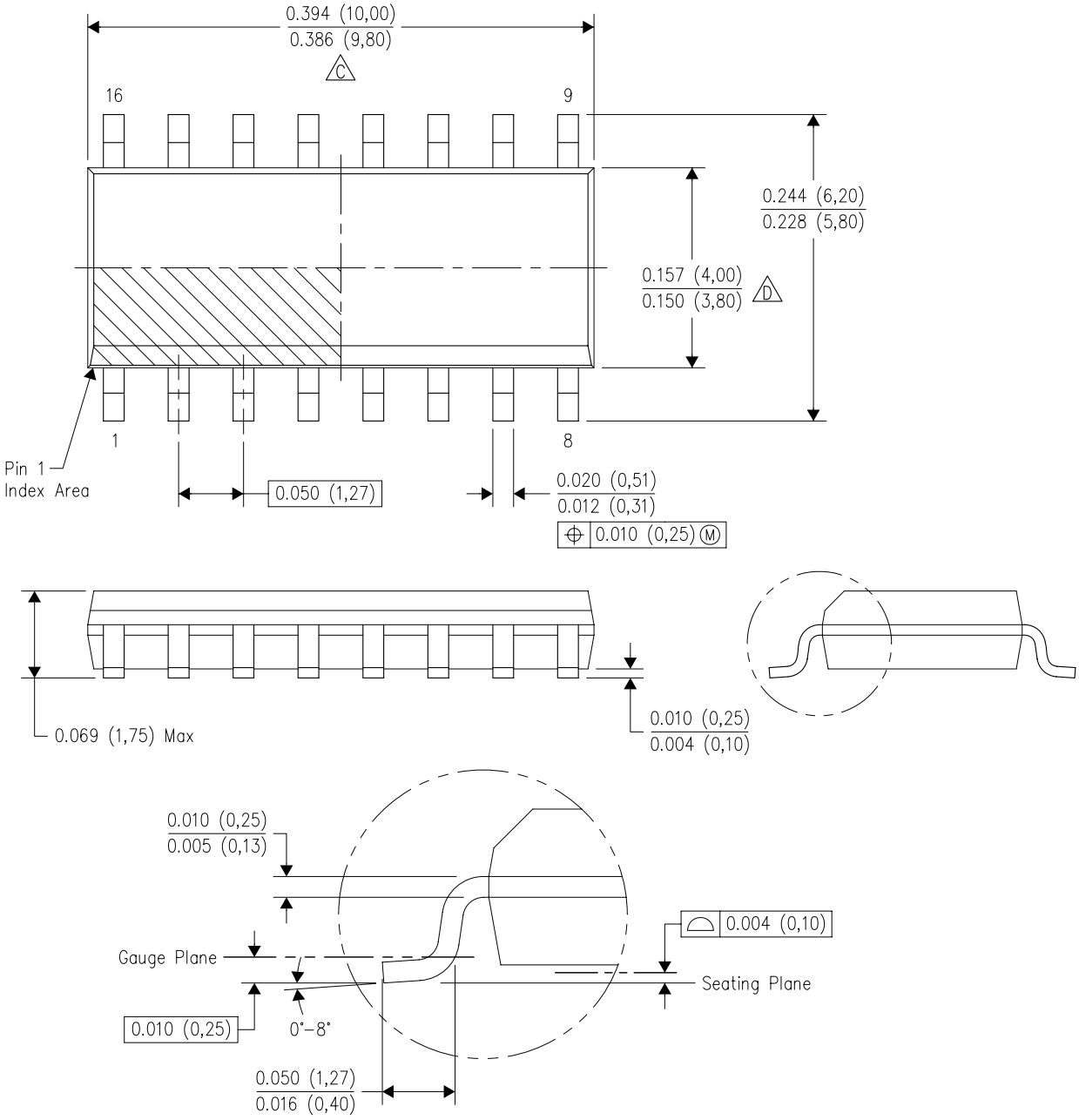
EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



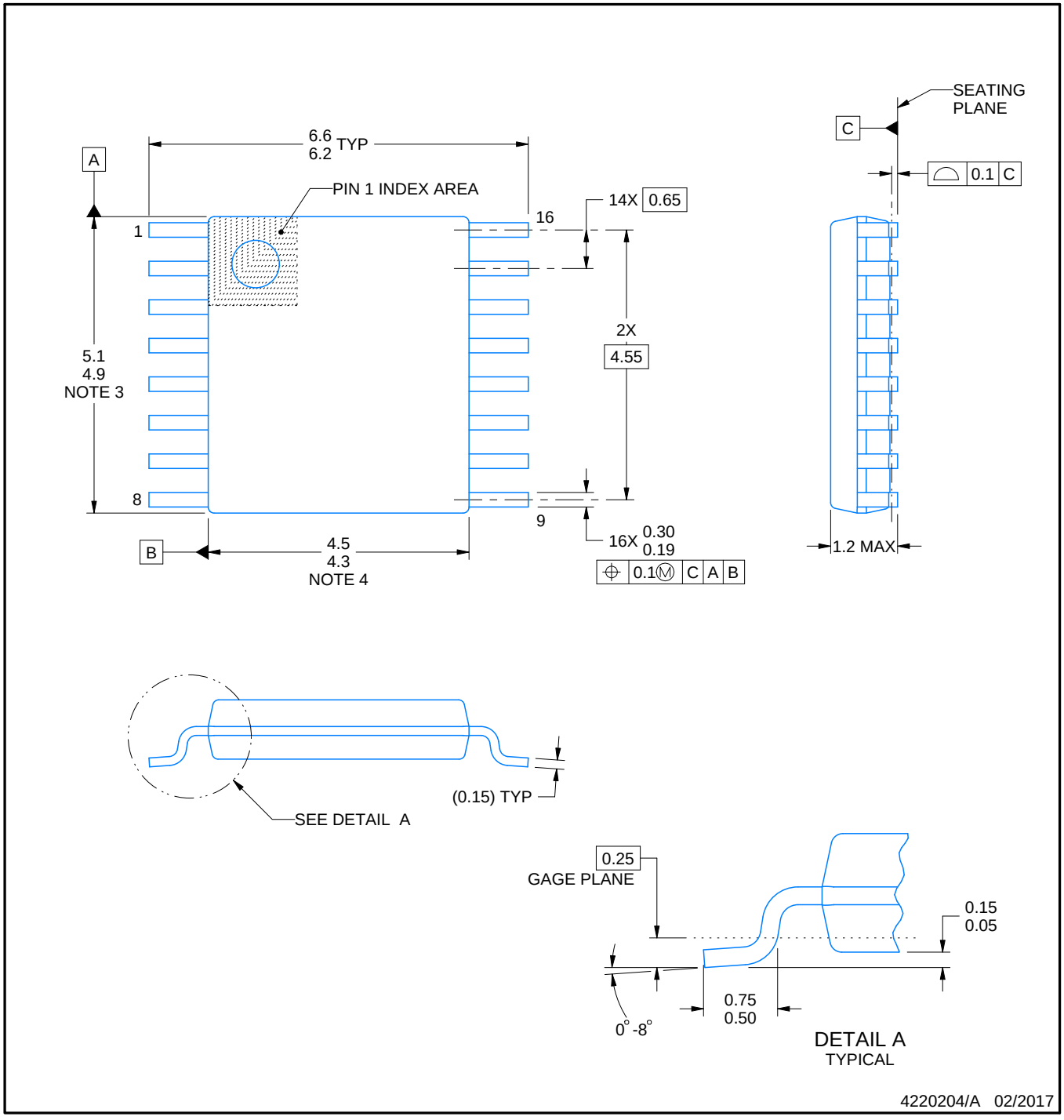
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

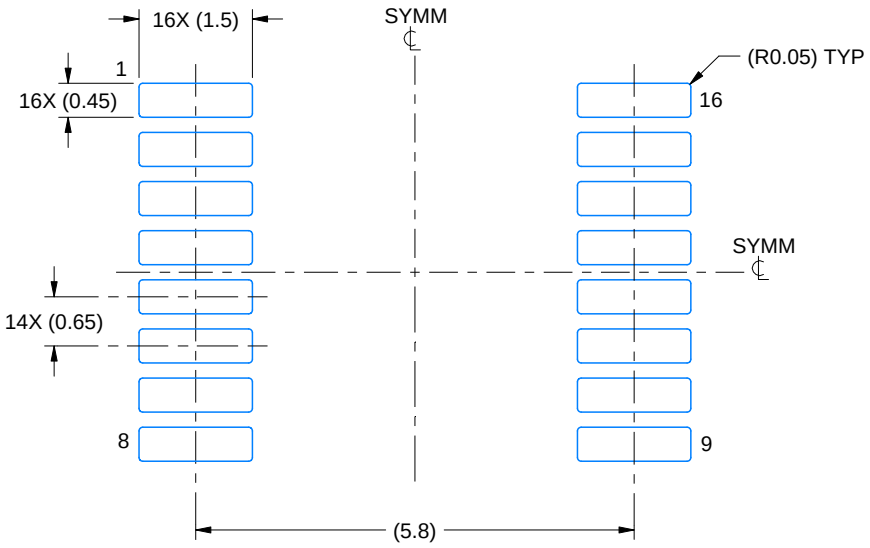
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

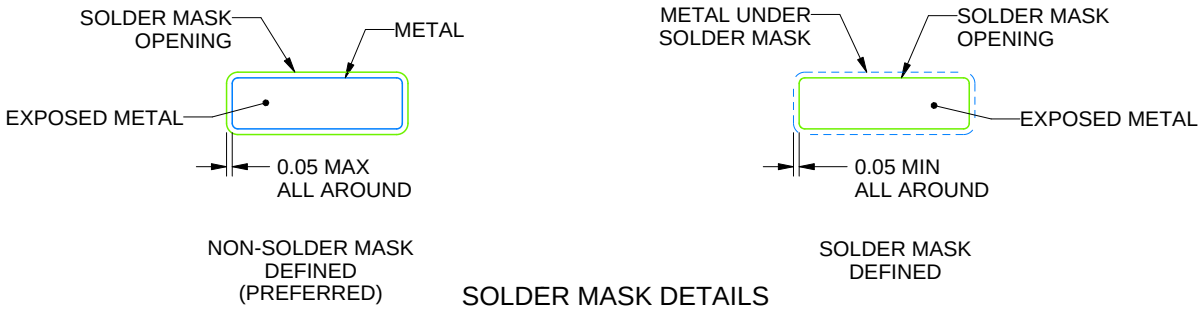


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

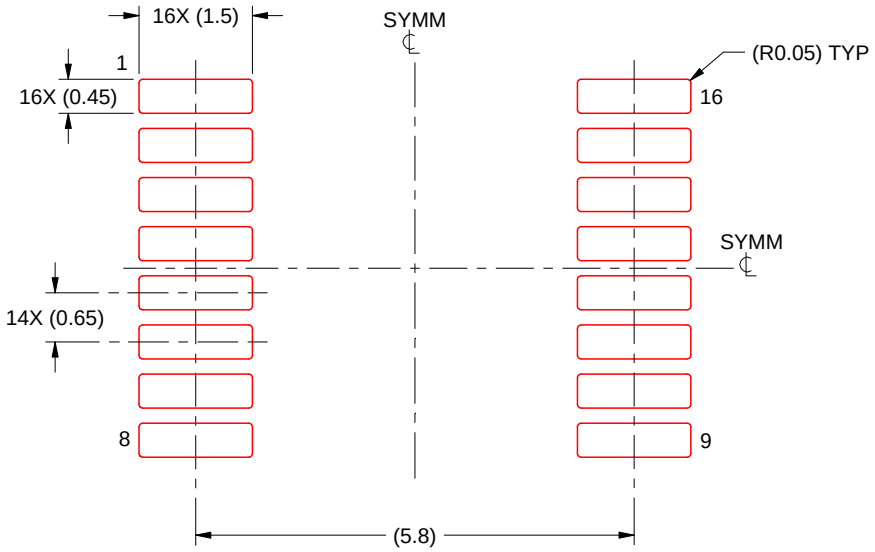


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

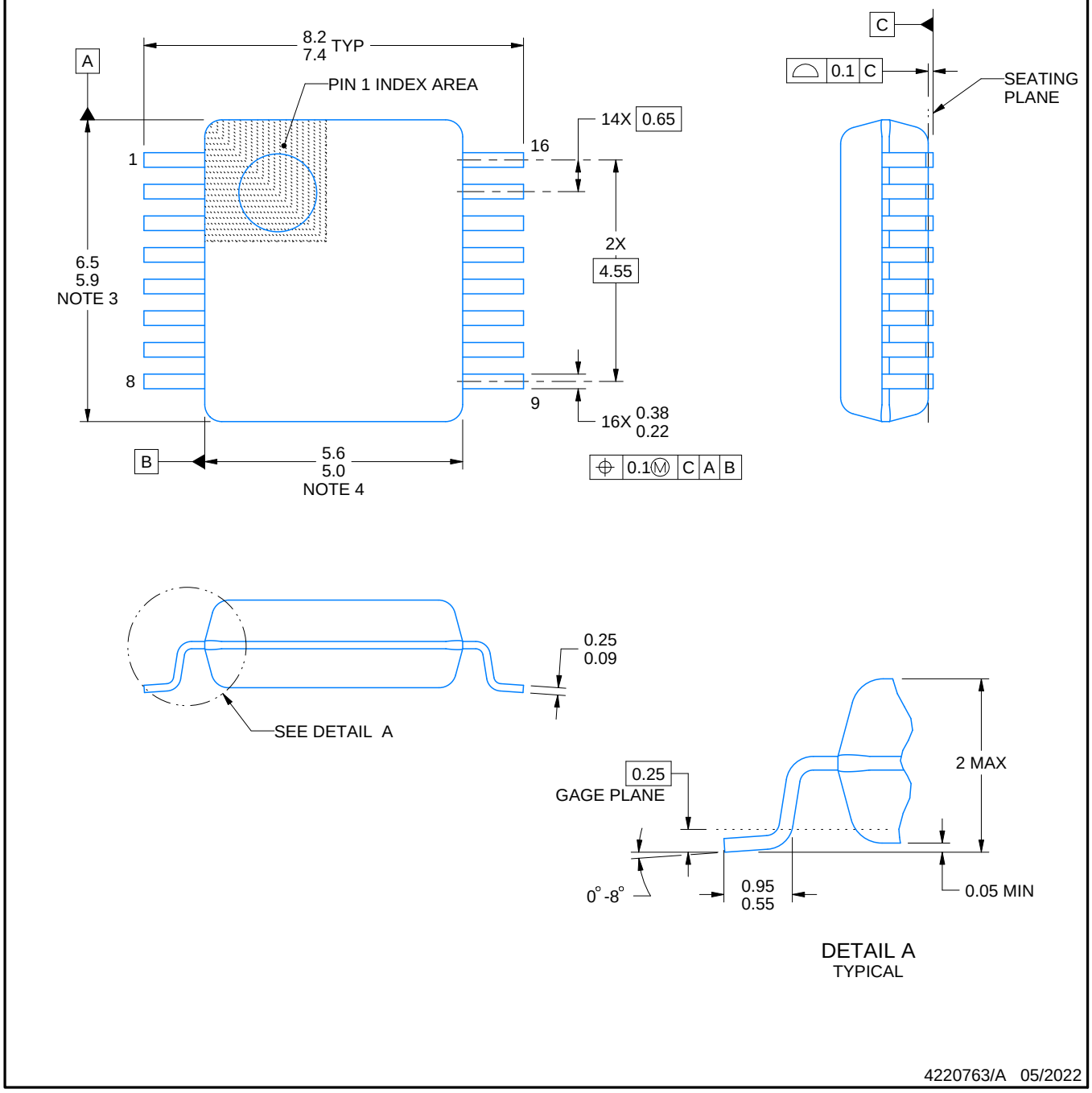
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

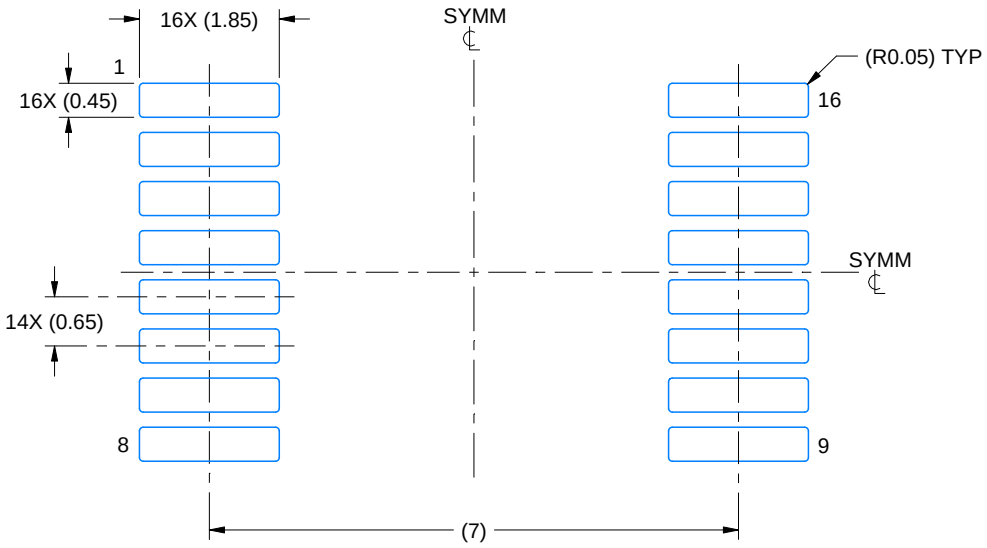
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

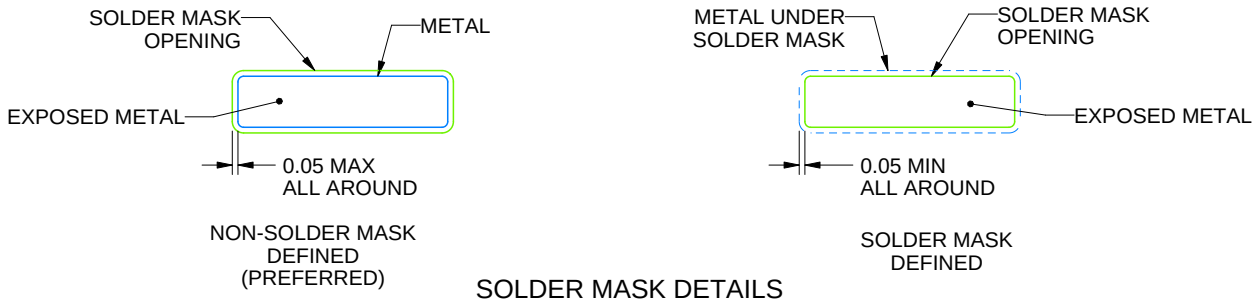


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

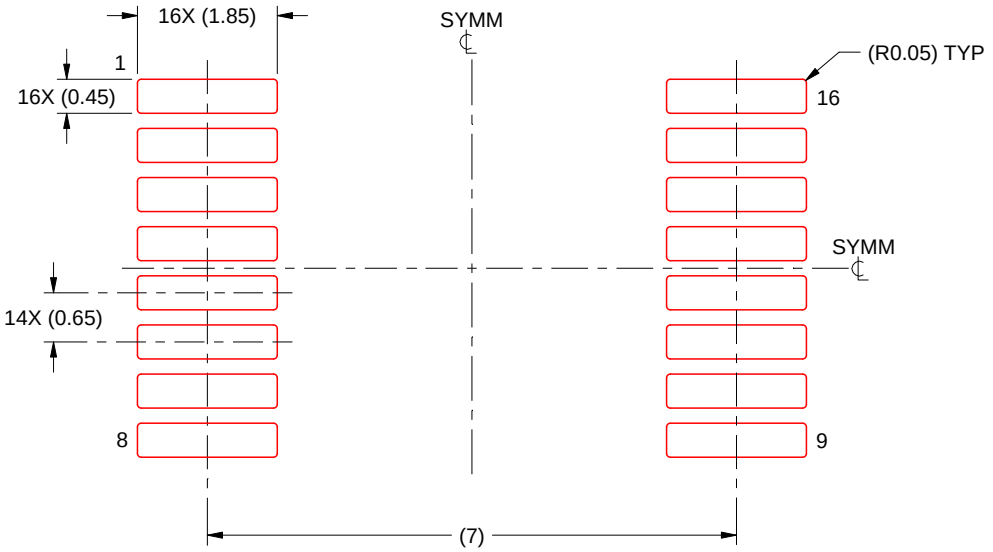


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

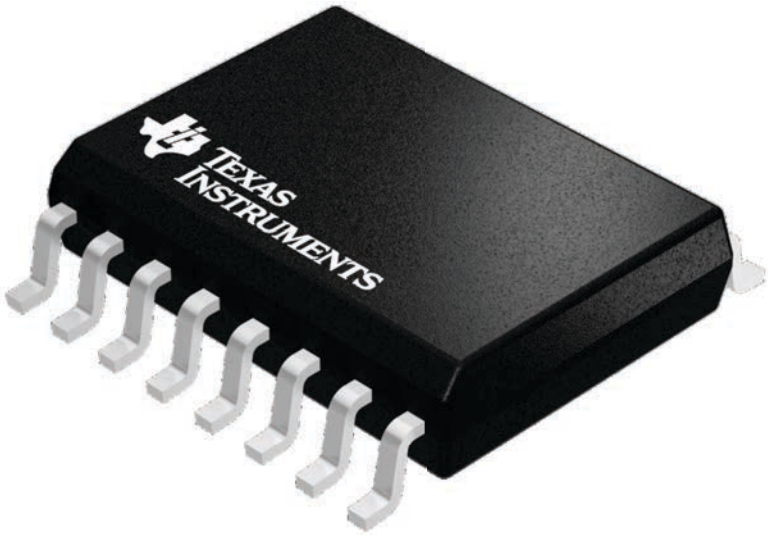
DW 16

SOIC - 2.65 mm max height

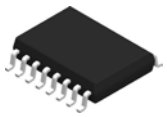
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

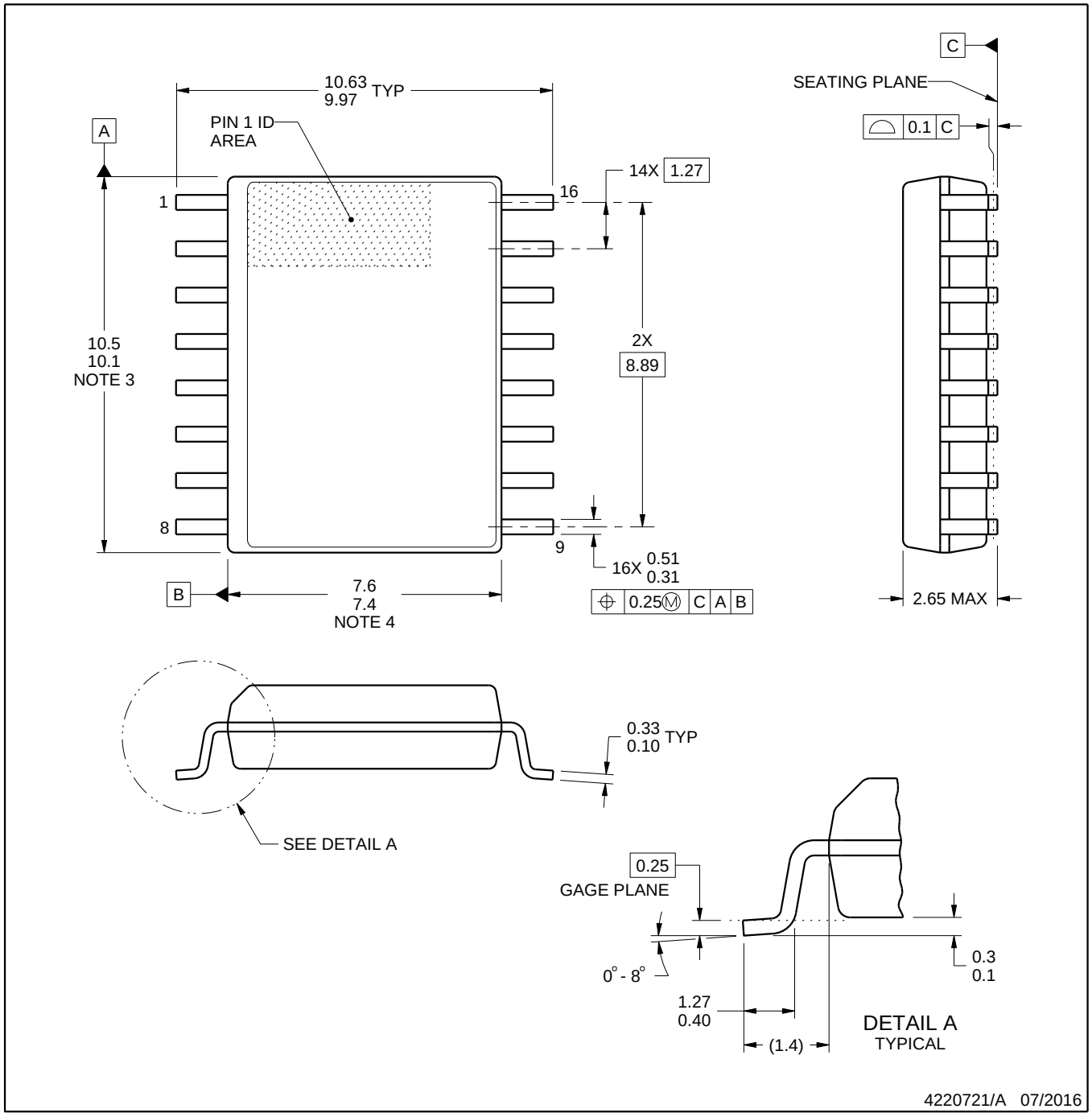


PACKAGE OUTLINE

DW0016A

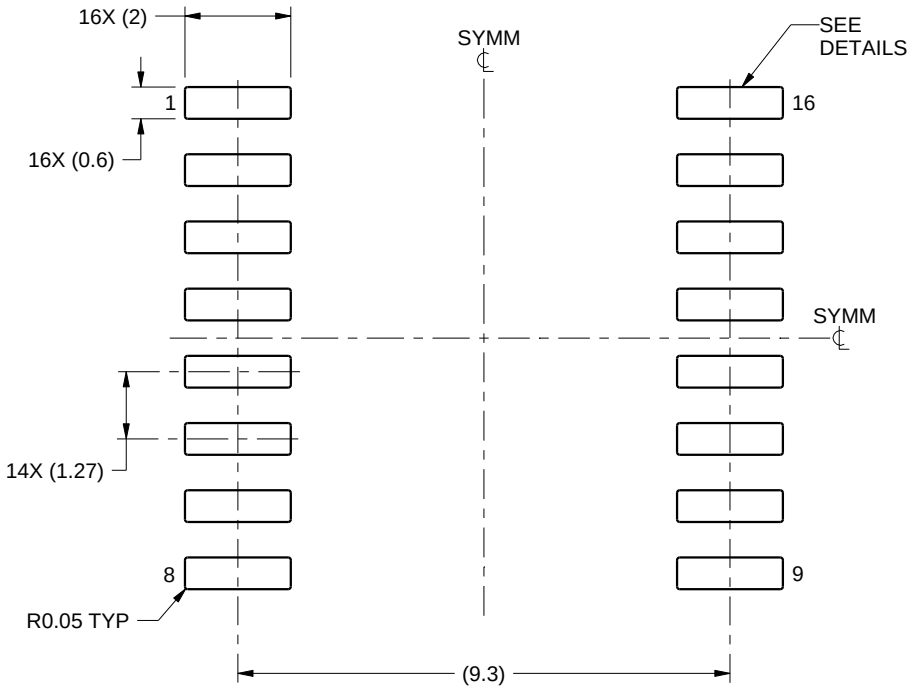
SOIC - 2.65 mm max height

SOIC

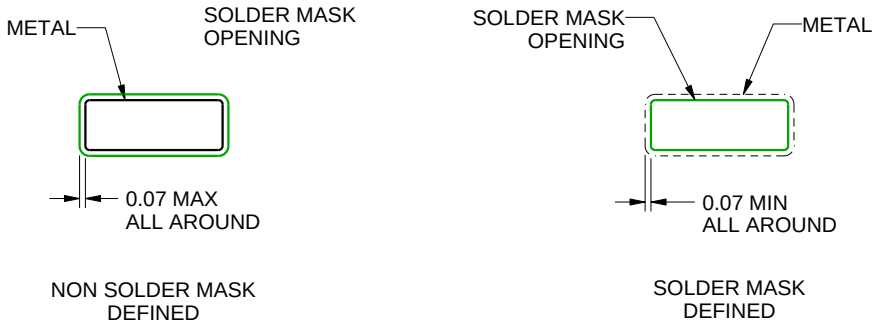


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

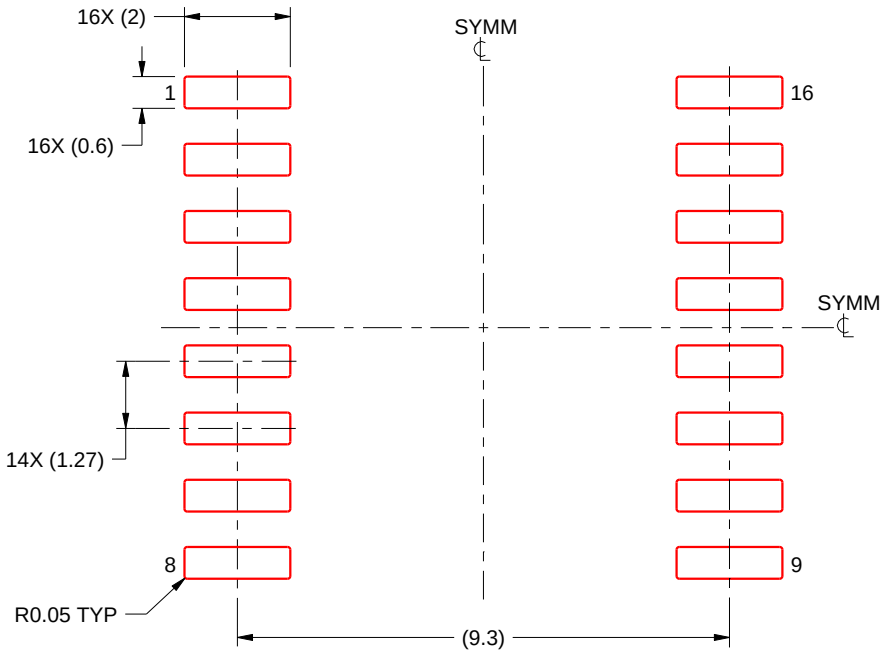


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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