

## 0.9-Ω SPDT ANALOG SWITCH 5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

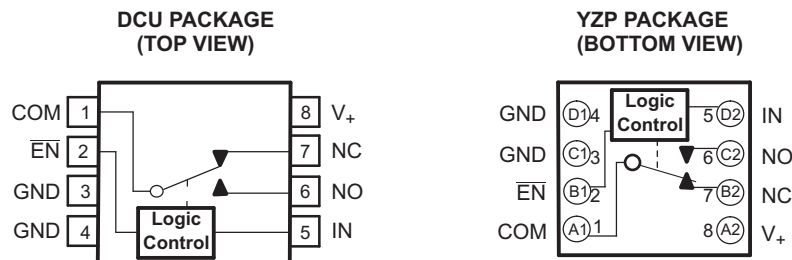
Check for Samples: [TS5A3154](#)

### FEATURES

- Specified Make-Before-Break Switching
- Low ON-State Resistance (0.9 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



### DESCRIPTION/ORDERING INFORMATION

The TS5A3154 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

**Table 1. ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1) (2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	TS5A3154YZPR	__ _JX_
	SSOP – DCU	Reel of 3000	TS5A3154DCUR	JCF_

- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (3) DCU: The actual top-side marking has one additional character that designates the assembly/test site.  
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

**Table 2. FUNCTION TABLE**

$\overline{\text{EN}}$	IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

**Table 3. Summary of Characteristics<sup>(1)</sup>**

Configuration	Single-Pole, Double-Throw 2:1 Multiplexer/Demultiplexer (SPDT)
Number of channels	1
ON-state resistance ( $r_{\text{on}}$ )	0.9 $\Omega$
ON-state resistance match ( $\Delta r_{\text{on}}$ )	0.1 $\Omega$
ON-state resistance flatness ( $r_{\text{on(flat)}}$ )	0.15 $\Omega$
Turn-on/turn-off time ( $t_{\text{ON}}/t_{\text{OFF}}$ )	8 ns/12.5 ns
Make-before-break time ( $t_{\text{MKB}}$ )	12 ns
Charge injection ( $Q_{\text{C}}$ )	10 pC
Bandwidth (BW)	100 MHz
OFF isolation ( $O_{\text{ISO}}$ )	-64 dB at 1 MHz
Crosstalk ( $X_{\text{TALK}}$ )	-64 dB at 1 MHz
Total harmonic distortion (THD)	0.004%
Leakage current ( $I_{\text{COM(OFF)}}$ / $I_{\text{NC(OFF)}}$ )	$\pm 20$ nA
Power-supply current ( $I_{+}$ )	0.1 $\mu\text{A}$
Package option	8-pin SSOP or DSBGA

(1)  $V_{+} = 5$  V,  $T_{\text{A}} = 25^{\circ}\text{C}$

**Absolute Minimum and Maximum Ratings<sup>(1) (2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range <sup>(3)</sup>	-0.5	6.5	V
$V_{NC}$ , $V_{NO}$ , $V_{COM}$	Analog voltage range <sup>(3) (4) (5)</sup>	-0.5	$V_+ + 0.5$	V
$I_K$	Analog port diode current	$V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NO}, V_{NC}, V_{COM} > V_+$		mA
$I_{NC}$ , $I_{COM}$ , $I_{NO}$	On-state switch current	-200	200	mA
	On-state peak switch current <sup>(6)</sup>	-400	400	
$V_I$	Digital input voltage range <sup>(3) (4)</sup>	-0.5	6.5	V
$I_{IK}$	Digital input clamp current	$V_I < 0$		mA
$I_+$	Continuous current through $V_+$		100	mA
$I_{GND}$	Continuous current through GND	-100	100	mA
$\theta_{JA}$	Package thermal impedance <sup>(7)</sup>	DCU package		227
		YZP package		102
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics for 5-V Supply<sup>(1)</sup>

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V	0.9	1.1	$\Omega$	
				Full					1.3
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V	0.8	0.9	$\Omega$	
				Full					1.1
ON-state resistance matching between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V	0.05	0.1	$\Omega$	
				Full					0.1
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V	0.15		$\Omega$	
				Full					
				25°C		4.5 V	0.09		0.15
Full	0.15								
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = 4.5\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	5.5 V	-20	2	20	nA
				Full		-150	150		
	$I_{NC(PWROFF)}, I_{NO(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to } 0$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	0 V	-5	0.7	5	$\mu\text{A}$
				Full		-25	25		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	5.5 V	-20	2	20	nA
				Full		-150	150		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$ , $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , or $V_{COM} = 4.5\text{ V}$ , $V_{NC} \text{ or } V_{NO} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	5.5 V	-20	2	20	nA
				Full		-150	150		
	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to } 0$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	0 V	-5	0.7	5	$\mu\text{A}$
				Full		-25	25		
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NC} \text{ or } V_{NO} = \text{Open}$ , or $V_{COM} = 4.5\text{ V}$ , $V_{NC} \text{ or } V_{NO} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	5.5 V	-20	2	20	nA
Full	-150	150							
<b>Digital Control Inputs (<math>I_N, \overline{EN}</math>)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$			Full		2.4	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.8	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0\text{ V}$		25°C	5.5 V	-100	25	100	nA
				Full		-100	100		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time, IN or $\overline{\text{OE}}$	$t_{\text{ON}}$	$V_{\text{COM}} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	1	5.2	8	ns
				Full	4.5 V to 5.5 V	1		9	
Turn-off time, IN or $\overline{\text{OE}}$	$t_{\text{OFF}}$	$V_{\text{COM}} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	5	9.5	12.5	ns
				Full	4.5 V to 5.5 V	4		13.5	
Make-before-break time	$t_{\text{MBB}}$	$V_{\text{COM}} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	4	6.3	12	ns
				Full	4.5 V to 5.5 V	4		13	
Charge injection	$Q_C$	$V_{\text{GEN}} = 0$ , $R_{\text{GEN}} = 0$ ,	$C_L = 1 \text{ nF}$ , See <a href="#">Figure 22</a>	25°C	5 V		10	pC	
NC, NO OFF capacitance	$C_{\text{NC(OFF)}}$ , $C_{\text{NO(OFF)}}$	$V_{\text{NC}}$ or $V_{\text{NO}} = V_+$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	5 V		19	pF	
NC, NO ON capacitance	$C_{\text{NC(ON)}}$ , $C_{\text{NO(ON)}}$	$V_{\text{NC}}$ or $V_{\text{NO}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	5 V		57	pF	
COM OFF capacitance	$C_{\text{COM(OFF)}}$	$V_{\text{COM}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	5 V		36	pF	
COM ON capacitance	$C_{\text{COM(ON)}}$	$V_{\text{COM}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	5 V		57	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	5 V		2	pF	
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON, See <a href="#">Figure 19</a>	25°C	5 V		100	MHz	
OFF isolation	$O_{\text{ISO}}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 20</a>	25°C	5 V		-64	dB	
Crosstalk	$X_{\text{TALK}}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch ON, See <a href="#">Figure 21</a>	25°C	5 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , See <a href="#">Figure 23</a>	25°C	5 V		0.004	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V		0.02	0.1	$\mu\text{A}$
				Full				0.5	

## Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	3 V		1.3 1.6	1.9	$\Omega$
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	3 V		1.2 1.5	1.7	$\Omega$
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2\text{ V}, 0.8\text{ V}$ $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	3 V		0.08 0.15	0.15	$\Omega$
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , $V_{NO} \text{ or } V_{NC} = 2\text{ V}, 0.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full 25°C Full	3 V		0.3 0.09 0.15	0.15	$\Omega$
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}, V_{COM} = 3\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 3\text{ V}, V_{COM} = 1\text{ V}$ , Switch OFF, See <a href="#">Figure 14</a>	25°C Full	3.6 V		-20 -50	2 50	20 nA
			25°C Full	0 V		-1 -15	0.2 15	1 $\mu\text{A}$
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}, V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 3\text{ V}, V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 15</a>	25°C Full	3.6 V		-20 -50	2 50	20 nA
			25°C Full	3.6 V		-20 -50	2 50	20 nA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}, V_{NC} \text{ or } V_{NO} = 3\text{ V}$ , or $V_{COM} = 3\text{ V}, V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , Switch OFF, See <a href="#">Figure 14</a>	25°C Full	3.6 V		-20 -50	2 50	20 nA
			25°C Full	0 V		-1 -15	0.2 15	1 $\mu\text{A}$
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}, V_{NC} \text{ or } V_{NO} = \text{Open}$ , or $V_{COM} = 3\text{ V}, V_{NC} \text{ or } V_{NO} = \text{Open}$ , Switch ON, See <a href="#">Figure 15</a>	25°C Full	3.6 V		-20 -50	2 50	20 nA
			25°C Full	3.6 V		-20 -50	2 50	20 nA
<b>Digital Control Inputs (<math>I_N, \overline{EN}</math>)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full			2	5.5	V
Input logic low	$V_{IL}$		Full			0	0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C Full	3.6 V		-100 -100	25 100	100 nA
			25°C Full	3.6 V		-100 -100	25 100	100 nA

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.  
 (2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time, IN or $\overline{\text{OE}}$	$t_{\text{ON}}$	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	3	6	10	ns
				Full	3 V to 3.6 V	2		10.5	
Turn-off time, IN or $\overline{\text{OE}}$	$t_{\text{OFF}}$	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	5	10	15	ns
				Full	3 V to 3.6 V	4		17	
Make-before-break time	$t_{\text{MBB}}$	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	4	5.7	12	ns
				Full	3 V to 3.6 V	4		13	
Charge injection	$Q_C$	$V_{\text{GEN}} = 0$ , $R_{\text{GEN}} = 0$ ,	$C_L = 1\ \text{nF}$ , See <a href="#">Figure 22</a>	25°C	3.3 V		9	pC	
NC, NO OFF capacitance	$C_{\text{NC(OFF)}}$ , $C_{\text{NO(OFF)}}$	$V_{\text{NC}}$ or $V_{\text{NO}} = V_+$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	3.3 V		19	pF	
NC, NO ON capacitance	$C_{\text{NC(ON)}}$ , $C_{\text{NO(ON)}}$	$V_{\text{NC}}$ or $V_{\text{NO}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	3.3 V		57	pF	
COM OFF capacitance	$C_{\text{COM(OFF)}}$	$V_{\text{COM}} = V_+$ or GND,	Switch ON, See	25°C	3.3 V		36	pF	
COM ON capacitance	$C_{\text{COM(ON)}}$	$V_{\text{COM}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	3.3 V		57	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	3.3 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ ,	Switch ON, See <a href="#">Figure 19</a>	25°C	3.3 V		100	MHz	
OFF isolation	$O_{\text{ISO}}$	$R_L = 50\ \Omega$ , $f = 1\ \text{MHz}$ ,	Switch OFF, See <a href="#">Figure 20</a>	25°C	3.3 V		-64	dB	
Crosstalk	$X_{\text{TALK}}$	$R_L = 50\ \Omega$ , $f = 1\ \text{MHz}$ ,	Switch ON, See <a href="#">Figure 21</a>	25°C	3.3 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\ \text{pF}$ ,	$f = 20\ \text{Hz to }20\ \text{kHz}$ , See <a href="#">Figure 23</a>	25°C	3.3 V		0.01 0	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V	0.01	0.1	$\mu\text{A}$	
				Full			0.25		

### Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>

V<sub>+</sub> = 3 V to 3.6 V, T<sub>A</sub> = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>				0		V <sub>+</sub>	V	
Peak ON resistance	r <sub>peak</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –8 mA,	Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V	1.9	2.5	Ω	
				Full					2.7
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.8 V, I <sub>COM</sub> = –8 mA,	Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V	1.6	2.1	Ω	
				Full					2.5
ON-state resistance matching between channels	Δr <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.8 V, I <sub>COM</sub> = –8 mA,	Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V	0.12	0.2	Ω	
				Full					0.2
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –8 mA,	Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V	0.65		Ω	
				Full					
				25°C		0.5			
				Full		1			
NC, NO OFF leakage current	I <sub>NC(OFF)</sub> , I <sub>NO(OFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0.5 V, V <sub>COM</sub> = 2.3 V, or V <sub>NC</sub> or V <sub>NO</sub> = 2.3 V, V <sub>COM</sub> = 0.5 V,	Switch OFF, See <a href="#">Figure 14</a>	25°C	2.7 V	–20	2	20	nA
				Full		–50		50	
	I <sub>NC(PWROFF)</sub> , I <sub>NO(PWROFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0 to 2.7 V, V <sub>COM</sub> = 2.7 V to 0,	Switch OFF, See <a href="#">Figure 14</a>	25°C	0 V	–1		1	μA
				Full		–10		10	
NC, NO ON leakage current	I <sub>NC(ON)</sub> , I <sub>NO(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0.5 V, V <sub>COM</sub> = Open, or V <sub>NC</sub> or V <sub>NO</sub> = 2.3 V, V <sub>COM</sub> = Open,	Switch ON, See <a href="#">Figure 15</a>	25°C	2.7 V	–20		20	nA
				Full		–50		50	
COM OFF leakage current	I <sub>COM(OFF)</sub>	V <sub>COM</sub> = 0.5 V, V <sub>NC</sub> or V <sub>NO</sub> = 2.3 V, or V <sub>COM</sub> = 2.3 V, V <sub>NC</sub> or V <sub>NO</sub> = 0.5V,	Switch OFF, See <a href="#">Figure 14</a>	25°C	2.7 V	–20		20	nA
				Full		–50		50	
	I <sub>COM(PWROFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0 to 2.7 V, V <sub>COM</sub> = 2.7 V to 0,	Switch OFF, See <a href="#">Figure 14</a>	25°C	0 V	–1		1	μA
				Full		–10		10	
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>COM</sub> = 0.5 V, V <sub>NC</sub> or V <sub>NO</sub> = Open, or V <sub>COM</sub> = 2.3 V, V <sub>NC</sub> or V <sub>NO</sub> = Open,	Switch ON, See <a href="#">Figure 15</a>	25°C	2.7 V	–20		20	nA
				Full		–50		50	
<b>Digital Control Inputs (IN, EN)<sup>(2)</sup></b>									
Input logic high	V <sub>IH</sub>		Full		1.8		5.5	V	
Input logic low	V <sub>IL</sub>		Full		0		0.6	V	
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = 5.5 V or 0	25°C	2.7 V	–100	25	100	nA	
			Full		–100		100		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time, IN or $\overline{OE}$	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	4	7.0	11.5	ns
				Full	2.3 V to 2.7 V	3.5		12	
Turn-off time, IN or $\overline{OE}$	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	5	11.5	18.5	ns
				Full	2.3 V to 2.7 V	4		21	
Make-before-break time	$t_{MKB}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	2.5 V	4	6.3	15	ns
				Full	2.3 V to 2.7 V	4		16	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 22</a>	25°C	2.5 V		7	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	2.5 V		19	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.5 V		57	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.5 V		36	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.5 V		57	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	2.5 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ ,	Switch ON, See <a href="#">Figure 19</a>	25°C	2.5 V		100	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 20</a>	25°C	2.5 V		-64	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch ON, See <a href="#">Figure 21</a>	25°C	2.5 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 23</a>	25°C	2.5 V		0.020	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V	0.001	0.05	$\mu\text{A}$	
				Full			0.15		

### Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>

V<sub>+</sub> = 1.65 V to 1.95 V, T<sub>A</sub> = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>				0		V <sub>+</sub>	V	
Peak ON resistance	r <sub>peak</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –2 mA,	25°C	1.65 V		5.5	25	Ω	
			Full				30		
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V, I <sub>COM</sub> = –2 mA,	25°C	1.65 V		2	2.7	Ω	
			Full				3.1		
ON-state resistance matching between channels	Δr <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V, I <sub>COM</sub> = –2 mA,	25°C	1.65 V		0.16	0.3	Ω	
			Full				0.3		
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –2 mA,	25°C	1.65 V		3		Ω	
		V <sub>NO</sub> or V <sub>NC</sub> = 0.6 V, 1.5 V, I <sub>COM</sub> = –2 mA,	25°C			3	20		
			Full				25		
NC, NO OFF leakage current	I <sub>NC(OFF)</sub> , I <sub>NO(OFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0.3 V, V <sub>COM</sub> = 1.65 V, or V <sub>NC</sub> or V <sub>NO</sub> = 1.65 V, V <sub>COM</sub> = 0.3 V,	25°C	1.95 V		–20	1.5	20	nA
			Full			–50		50	
	I <sub>NC(PWROFF)</sub> , I <sub>NO(PWROFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0 to 1.95 V, V <sub>COM</sub> = 1.95 V to 0,	25°C	0 V		–1	0.1	1	μA
			Full			–10		10	
NC, NO ON leakage current	I <sub>NC(ON)</sub> , I <sub>NO(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0.3 V, V <sub>COM</sub> = Open, or V <sub>NC</sub> or V <sub>NO</sub> = 1.65 V, V <sub>COM</sub> = Open,	25°C	1.95 V		–20	1.5	20	nA
			Full			–50		50	
COM OFF leakage current	I <sub>COM(OFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 1.65 V, V <sub>COM</sub> = 0.3 V, or V <sub>NC</sub> or V <sub>NO</sub> = 0.3 V, V <sub>COM</sub> = 1.65 V,	25°C	1.95 V		–20	1.5	20	nA
			Full			–50		50	
	I <sub>COM(PWROFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 1.95 V to 0, V <sub>COM</sub> = 0 to 1.95 V,	25°C	0 V		–1	0.06	1	μA
			Full			–10		10	
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = Open, V <sub>COM</sub> = 0.3 V, or V <sub>NC</sub> or V <sub>NO</sub> = Open, V <sub>COM</sub> = 1.65 V,	25°C	1.95 V		–20	1.5	20	nA
			Full			–50		50	
<b>Digital Control Inputs (IN, EN)<sup>(2)</sup></b>									
Input logic high	V <sub>IH</sub>		Full		1.5		5.6	V	
Input logic low	V <sub>IL</sub>		Full		0		0.6	V	
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = 5.5 V or 0	25°C	1.95 V		–100	25	100	nA
			Full			–100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time, IN or $\overline{\text{OE}}$	$t_{\text{ON}}$	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	5	20.5	ns	
				Full	1.65 V to 1.95 V	4.5	21		
Turn-off time, IN or $\overline{\text{OE}}$	$t_{\text{OFF}}$	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	7	16.5	27.5	ns
				Full	1.65 V to 1.95 V	5	30		
Make-before-break time	$t_{\text{MBB}}$	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	4	8.3	15	ns
				Full	1.65 V to 1.95 V	4	16		
Charge injection	$Q_C$	$V_{\text{GEN}} = 0$ , $R_{\text{GEN}} = 0$ ,	$C_L = 1\ \text{nF}$ , See <a href="#">Figure 22</a>	25°C	1.8 V	5		pC	
NC, NO OFF capacitance	$C_{\text{NC(OFF)}}$ , $C_{\text{NO(OFF)}}$	$V_{\text{NC}}$ or $V_{\text{NO}} = V_+$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	1.8 V	19		pF	
NC, NO ON capacitance	$C_{\text{NC(ON)}}$ , $C_{\text{NO(ON)}}$	$V_{\text{NC}}$ or $V_{\text{NO}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	1.8 V	57		pF	
COM OFF capacitance	$C_{\text{COM(OFF)}}$	$V_{\text{COM}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	1.8 V	36		pF	
COM ON capacitance	$C_{\text{COM(ON)}}$	$V_{\text{COM}} = V_+$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	1.8 V	57		pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	1.8 V	2.0		pF	
Bandwidth	BW	$R_L = 50\ \Omega$ ,	Switch ON, See <a href="#">Figure 19</a>	25°C	1.8 V	100		MHz	
OFF isolation	$O_{\text{ISO}}$	$R_L = 50\ \Omega$ , $f = 1\ \text{MHz}$ ,	Switch OFF, See <a href="#">Figure 20</a>	25°C	1.8 V	-64		dB	
Crosstalk	$X_{\text{TALK}}$	$R_L = 50\ \Omega$ , $f = 1\ \text{MHz}$ ,	Switch ON, See <a href="#">Figure 21</a>	25°C	1.8 V	-64		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\ \text{pF}$ ,	$f = 20\ \text{Hz to }20\ \text{kHz}$ , See <a href="#">Figure 23</a>	25°C	1.8 V	0.060		%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V	0.001	0.05	$\mu\text{A}$	
				Full		0.1			

TYPICAL PERFORMANCE

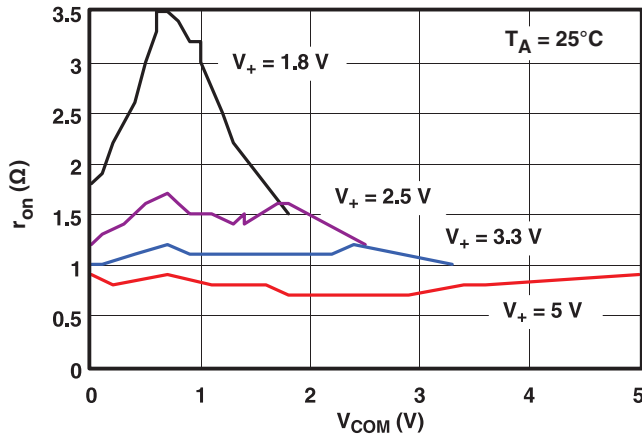


Figure 1.  $r_{on}$  vs  $V_{COM}$

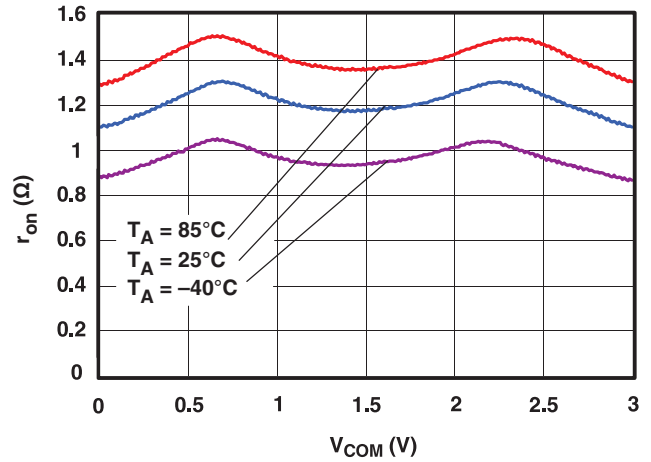


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3V$ )

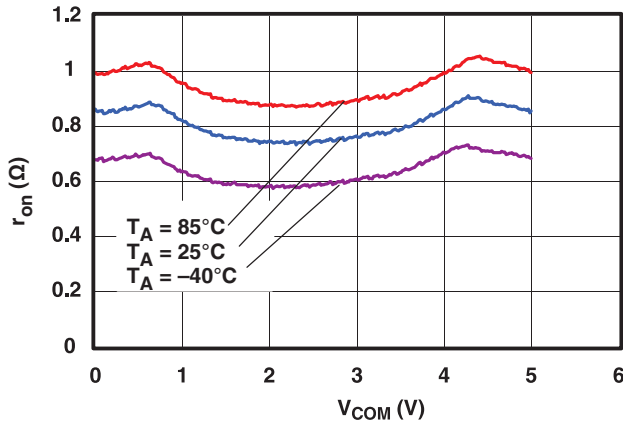


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5V$ )

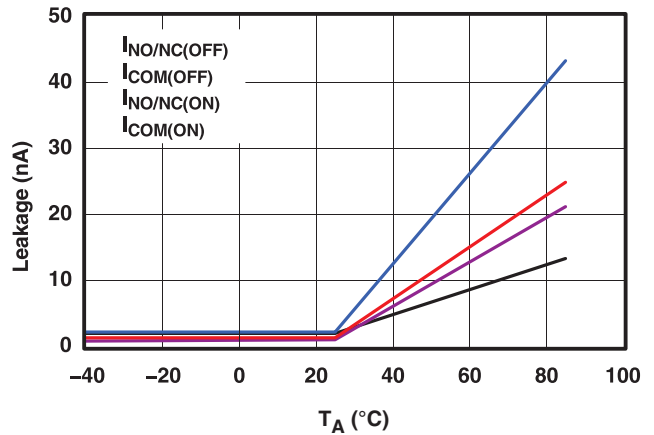


Figure 4. Leakage Current vs Temperature ( $V_+ = 5.5V$ )

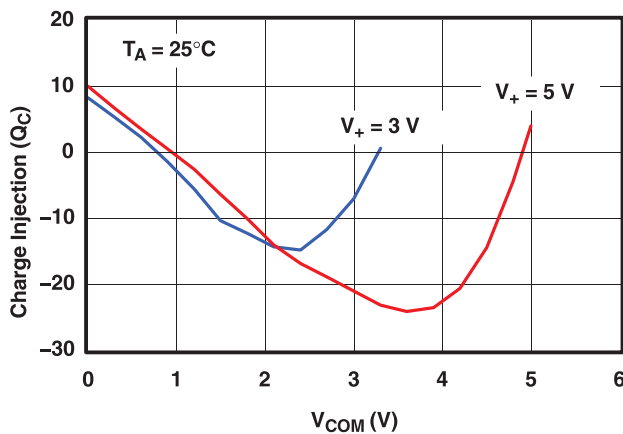


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

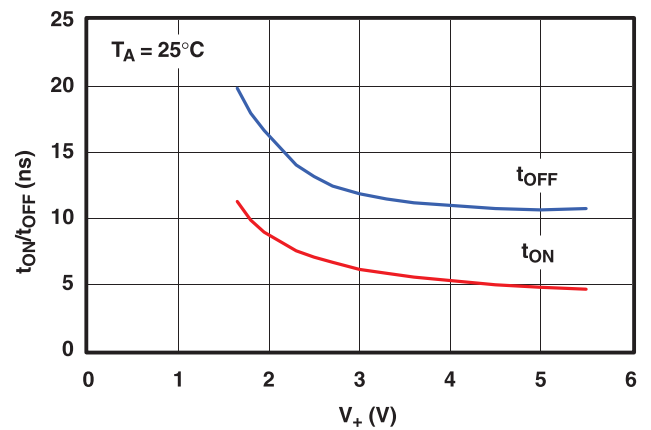


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

TYPICAL PERFORMANCE (continued)

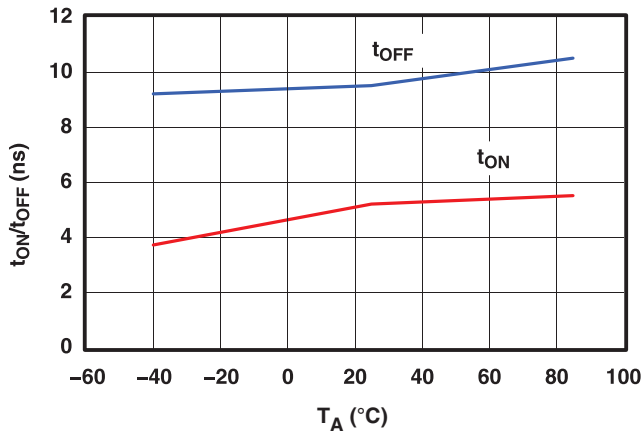


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5\text{ V}$ )

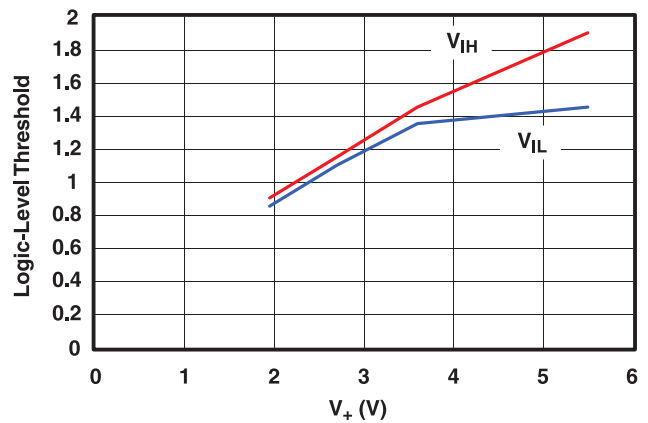


Figure 8. Logic-Level Threshold vs  $V_+$

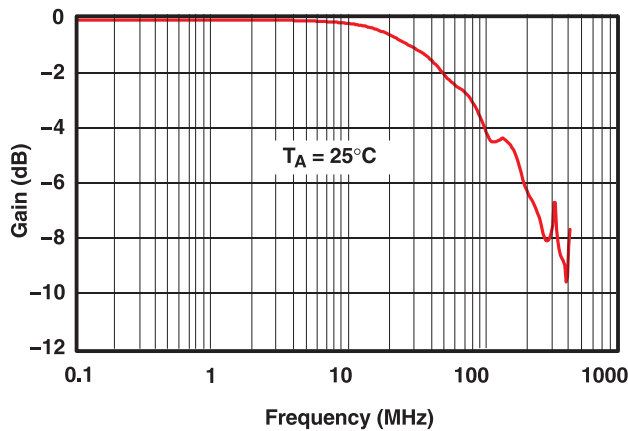


Figure 9. Bandwidth ( $V_+ = 5\text{ V}$ )

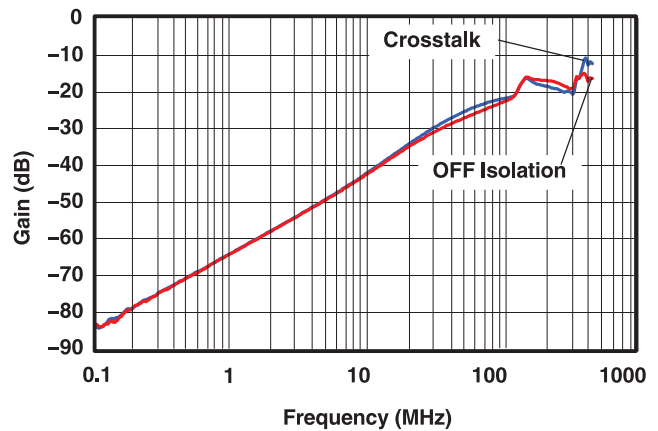


Figure 10. OFF Isolation and Crosstalk ( $V_+ = 5\text{ V}$ )

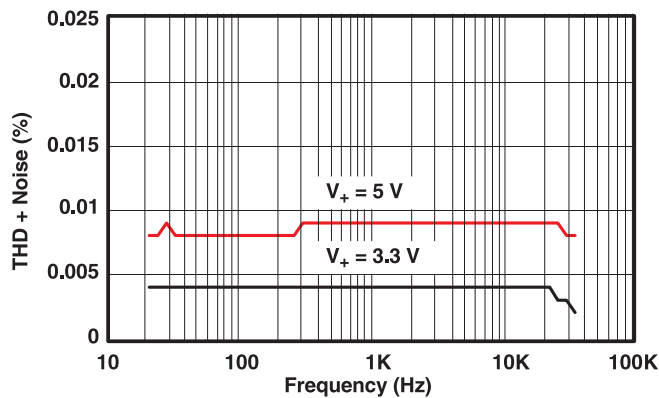


Figure 11. Total Harmonic Distortion (THD) vs Frequency

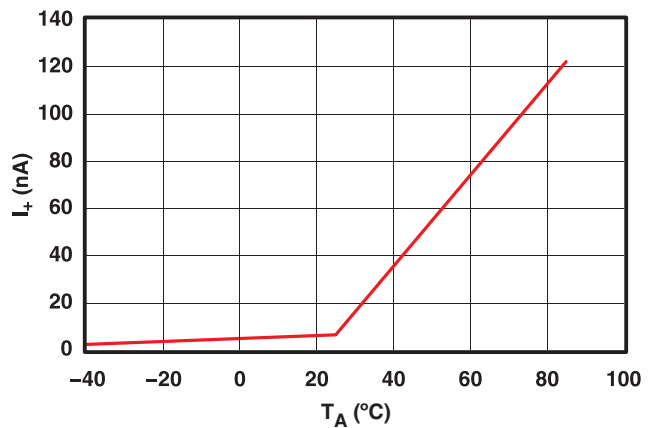


Figure 12. Power Supply Current vs Temperature ( $V_+ = 5\text{ V}$ )

**PIN DESCRIPTION**

PIN NO.	NAME	DESCRIPTION
1	COM	Common
2	$\overline{\text{EN}}$	Enable control input
3	GND	Digital ground
4	GND	Digital ground
5	IN	Digital control to connect the COM to NO or NC
6	NO	Normally open
7	NC	Normally closed
8	$V_+$	Power supply

**PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
$V_{\text{COM}}$	Voltage at COM
$V_{\text{NC}}$	Voltage at NC
$V_{\text{NO}}$	Voltage at NO
$r_{\text{on}}$	Resistance between COM and NC or COM and NO ports when the channel is ON
$\Delta r_{\text{on}}$	Difference of $r_{\text{on}}$ between channels in a specific device
$r_{\text{on(Flat)}}$	Difference between the maximum and minimum value of $r_{\text{on}}$ in a channel over the specified range of conditions
$I_{\text{NC(OFF)}}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{\text{NO(OFF)}}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{\text{NC(ON)}}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{\text{NO(ON)}}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{\text{COM(ON)}}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$V_{\text{IH}}$	Minimum input voltage for logic high for the control input (IN)
$V_{\text{IL}}$	Maximum input voltage for logic low for the control input (IN)
$V_{\text{I}}$	Voltage at the control input (IN)
$I_{\text{IH}}, I_{\text{IL}}$	Leakage current measured at the control input (IN)
$t_{\text{ON}}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
$t_{\text{OFF}}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
$t_{\text{BBM}}$	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
$Q_{\text{C}}$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_{\text{C}} = C_{\text{L}} \times \Delta V_{\text{COM}}$ , $C_{\text{L}}$ is the load capacitance and $\Delta V_{\text{COM}}$ is the change in analog output voltage.
$C_{\text{NC(OFF)}}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{\text{NO(OFF)}}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{\text{NC(ON)}}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{\text{NO(ON)}}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{\text{COM(ON)}}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
$C_{\text{I}}$	Capacitance of control input (IN)
$O_{\text{ISO}}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
$X_{\text{TALK}}$	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

PARAMETER MEASUREMENT INFORMATION

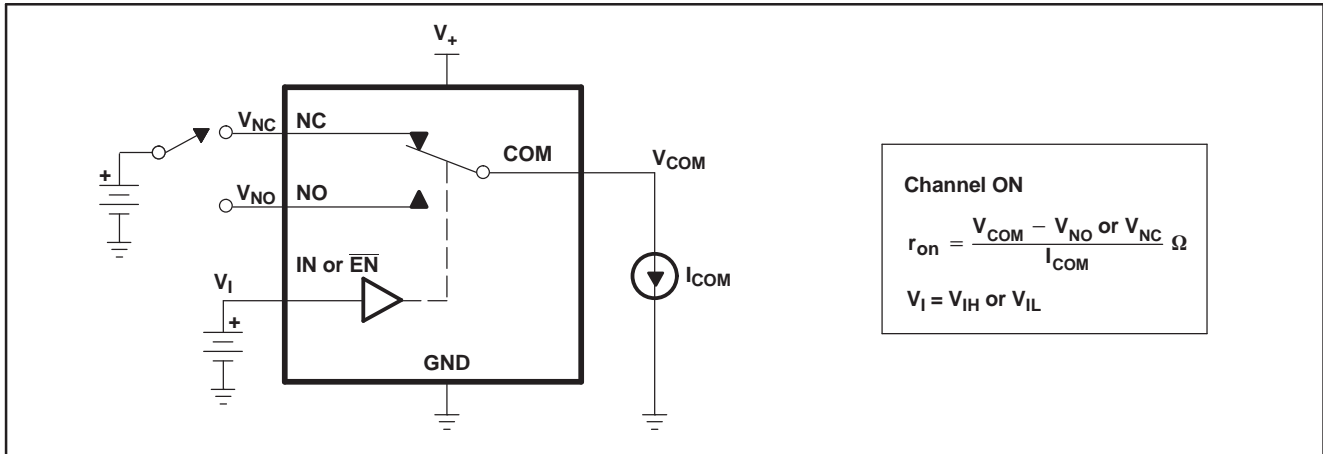


Figure 13. ON-State Resistance ( $r_{on}$ )

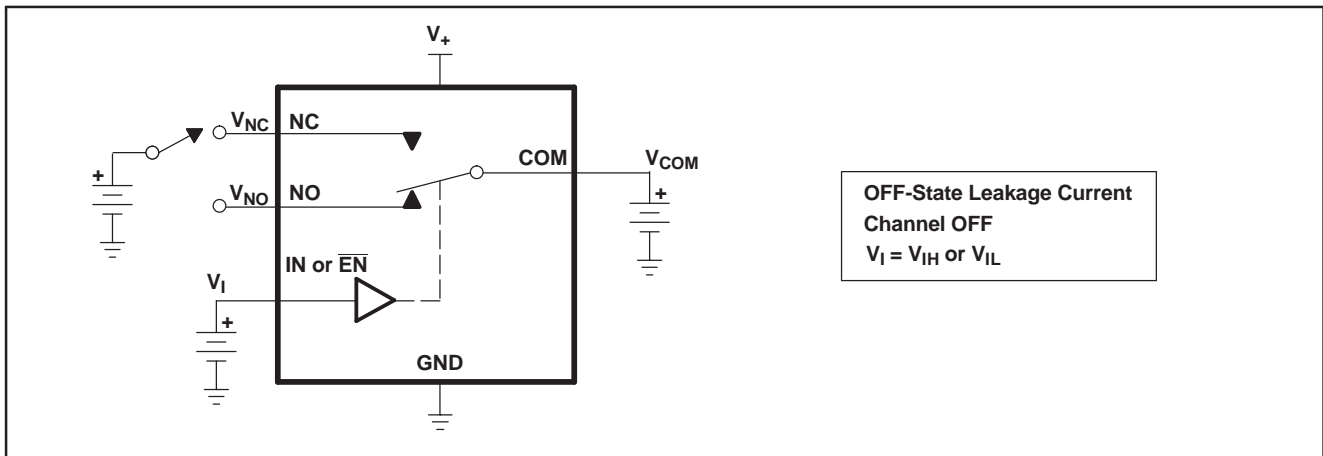
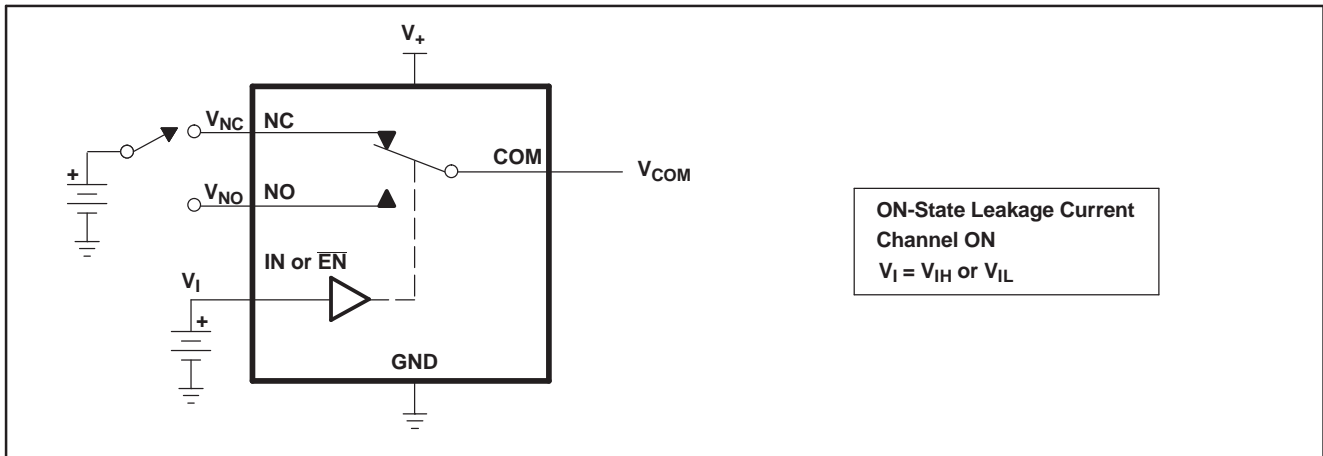
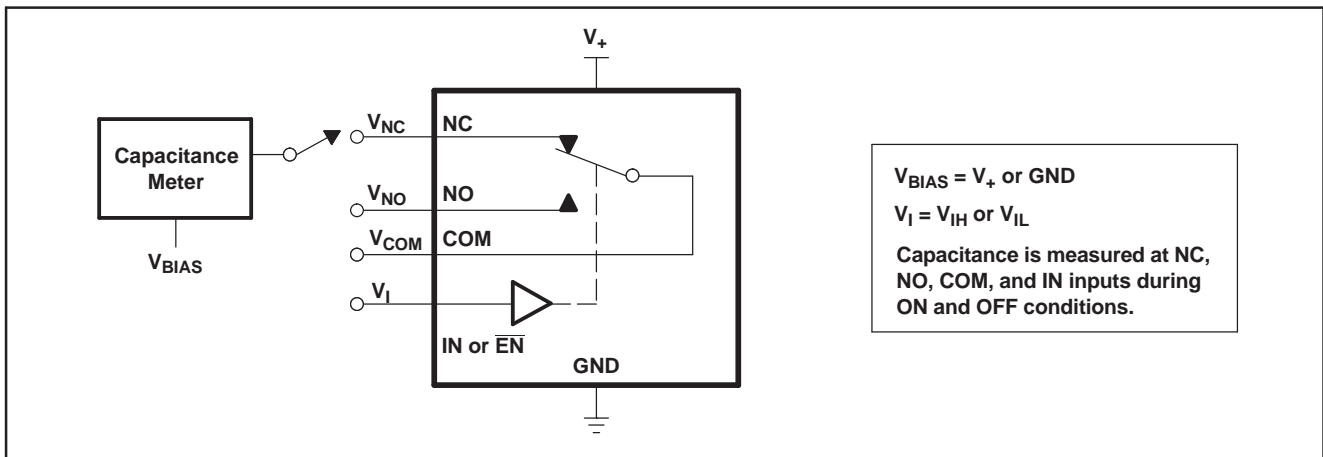


Figure 14. OFF-State Leakage Current ( $I_{NC(OFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{NO(PWROFF)}$ ,  $I_{COM(PWROFF)}$ )

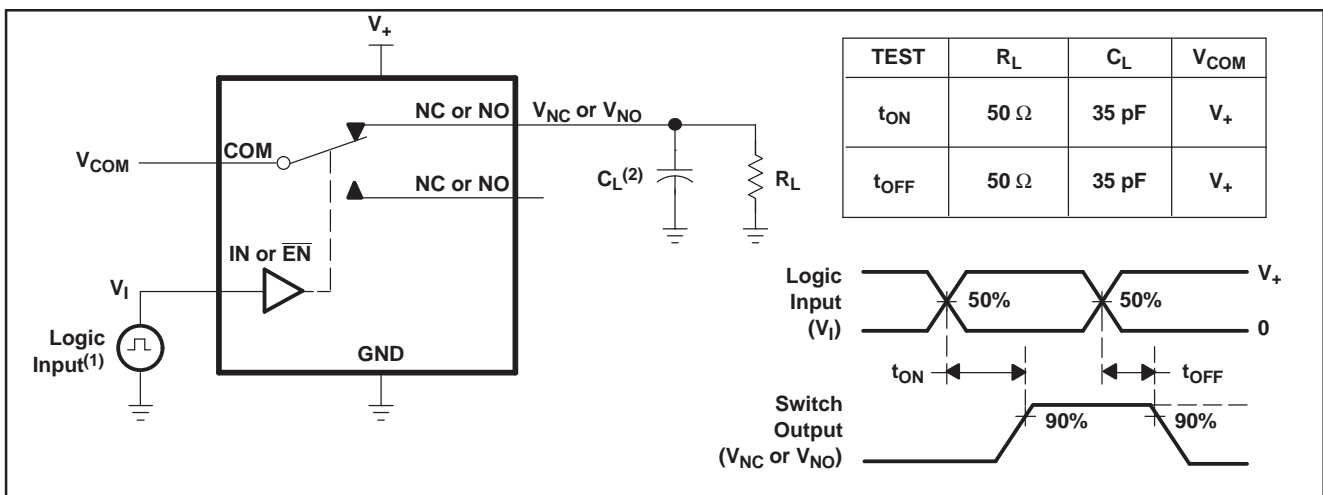
**PARAMETER MEASUREMENT INFORMATION (continued)**



**Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ ,  $I_{NO(ON)}$ )**



**Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NO(OFF)}$ ,  $C_{NC(ON)}$ ,  $C_{NO(ON)}$ )**

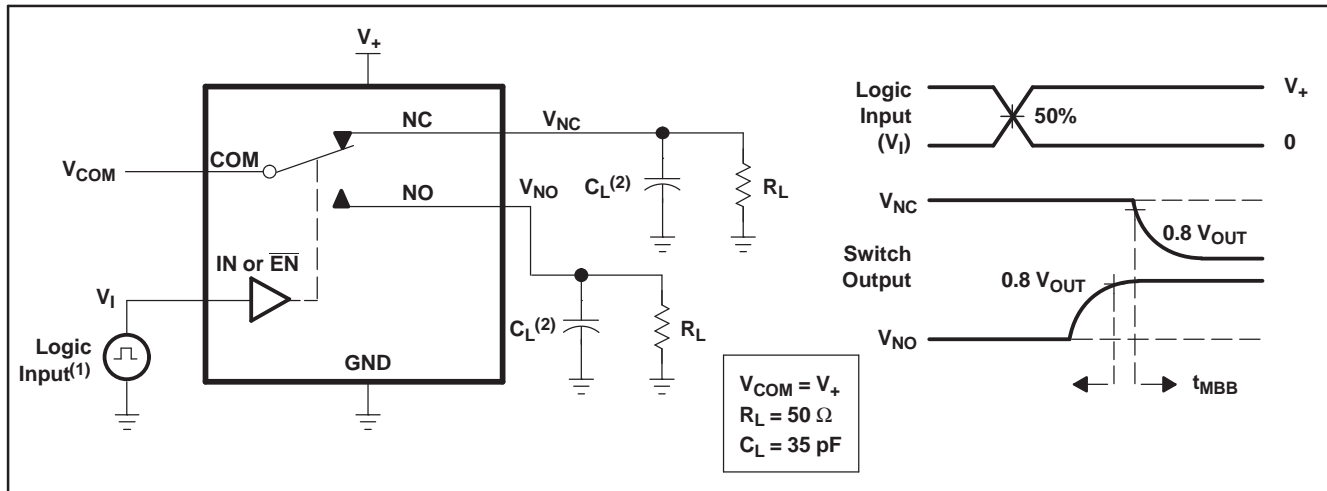


(1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.  
 (2)  $C_L$  includes probe and jig capacitance.

**Figure 17. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )**



PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- (2) C<sub>L</sub> includes probe and jig capacitance.

Figure 18. Make-Before-Break Time (t<sub>MBB</sub>)

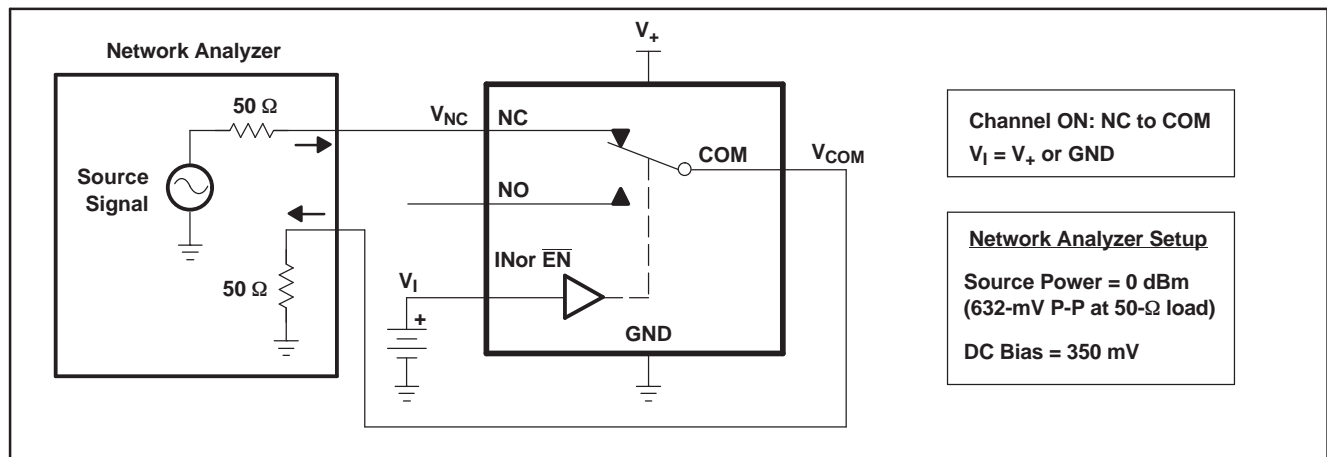


Figure 19. Bandwidth (BW)

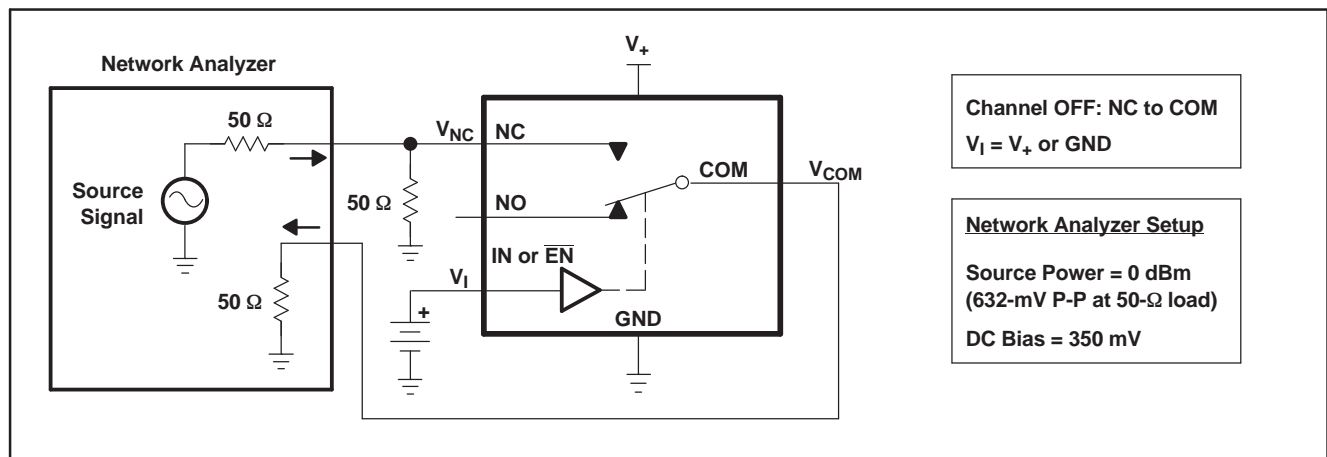
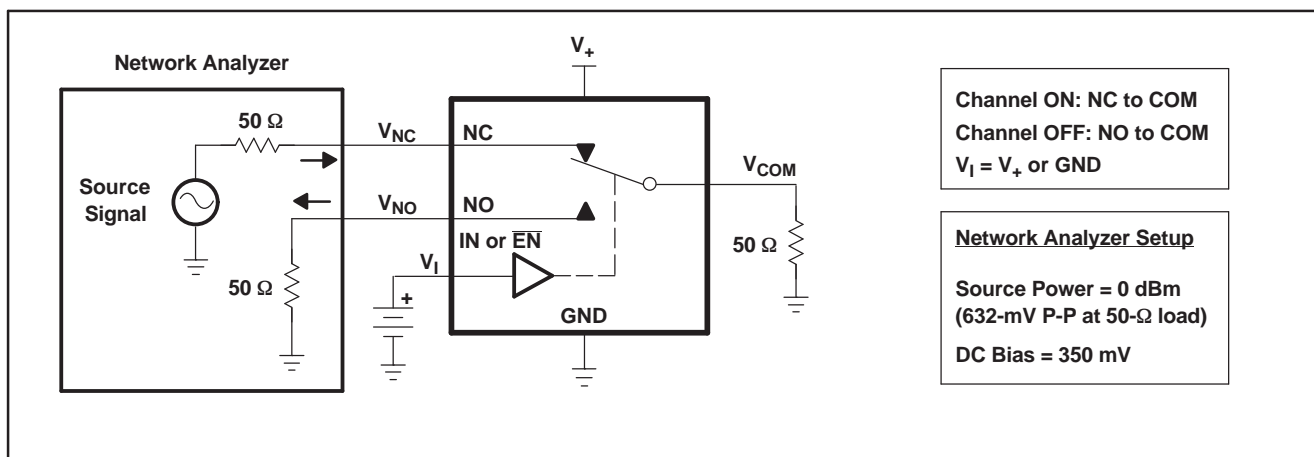
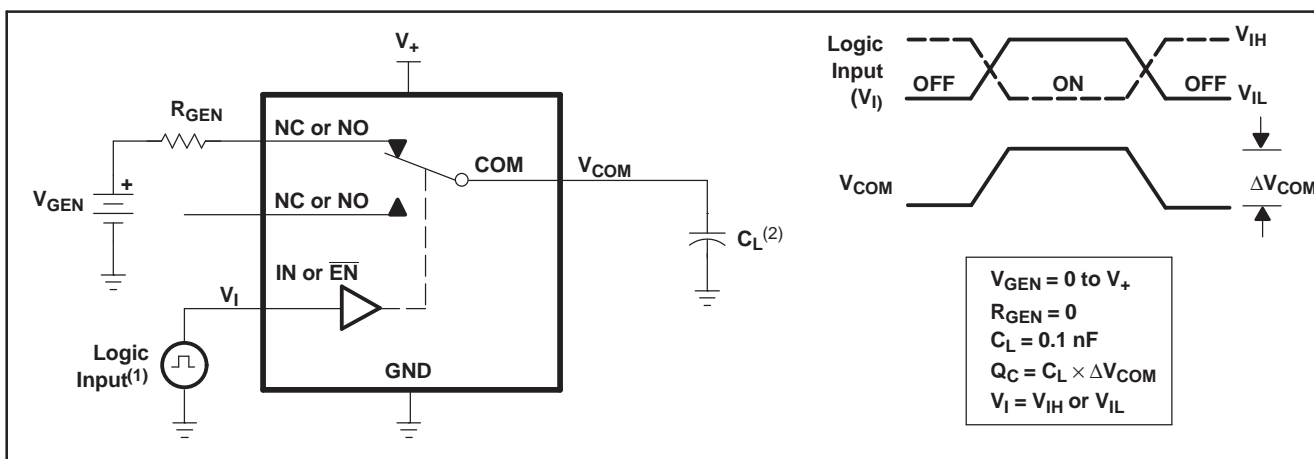


Figure 20. OFF Isolation (O<sub>ISO</sub>)

**PARAMETER MEASUREMENT INFORMATION (continued)**



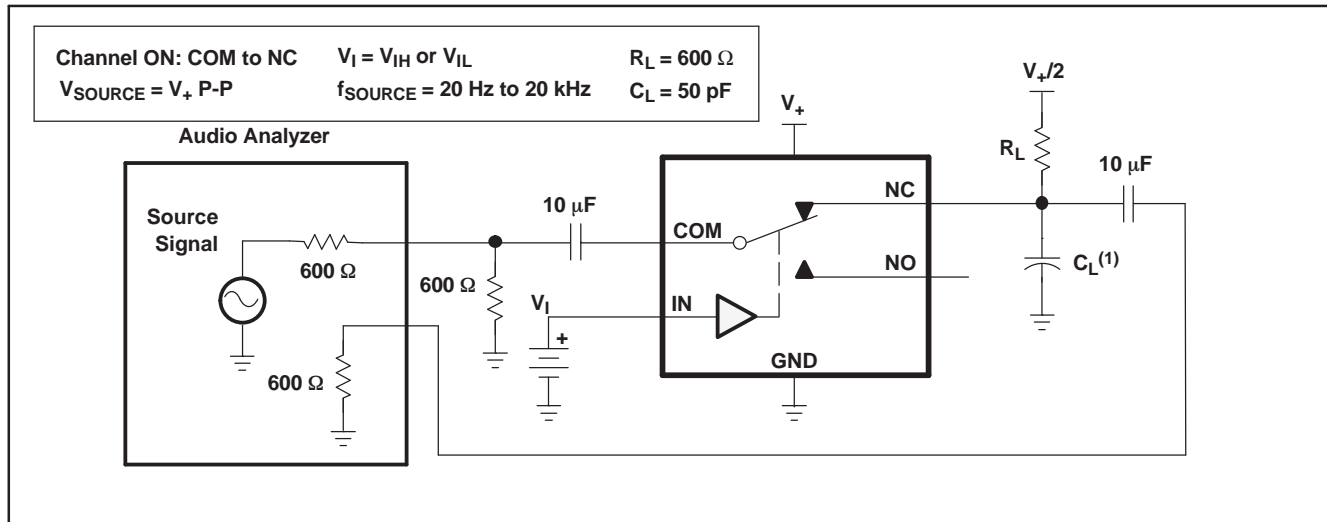
**Figure 21. Crosstalk ( $X_{TALK}$ )**



(1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.  
 (2)  $C_L$  includes probe and jig capacitance.

**Figure 22. Charge Injection ( $Q_C$ )**

PARAMETER MEASUREMENT INFORMATION (continued)



(1)  $C_L$  includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

## REVISION HISTORY

Changes from Revision B (May 2009) to Revision C	Page
• Changed ORDERING INFORMATION Table. ....	1

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3154DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(CF, JCFQ, JCFR) JZ	<a href="#">Samples</a>
TS5A3154DCURE6	PREVIEW	VSSOP	DCU	8	3000	TBD	Call TI	Call TI	-40 to 85		
TS5A3154DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JCFR	<a href="#">Samples</a>
TS5A3154YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JXN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3154DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3154DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3154DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3154YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

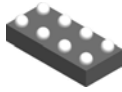
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3154DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3154DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3154DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3154YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



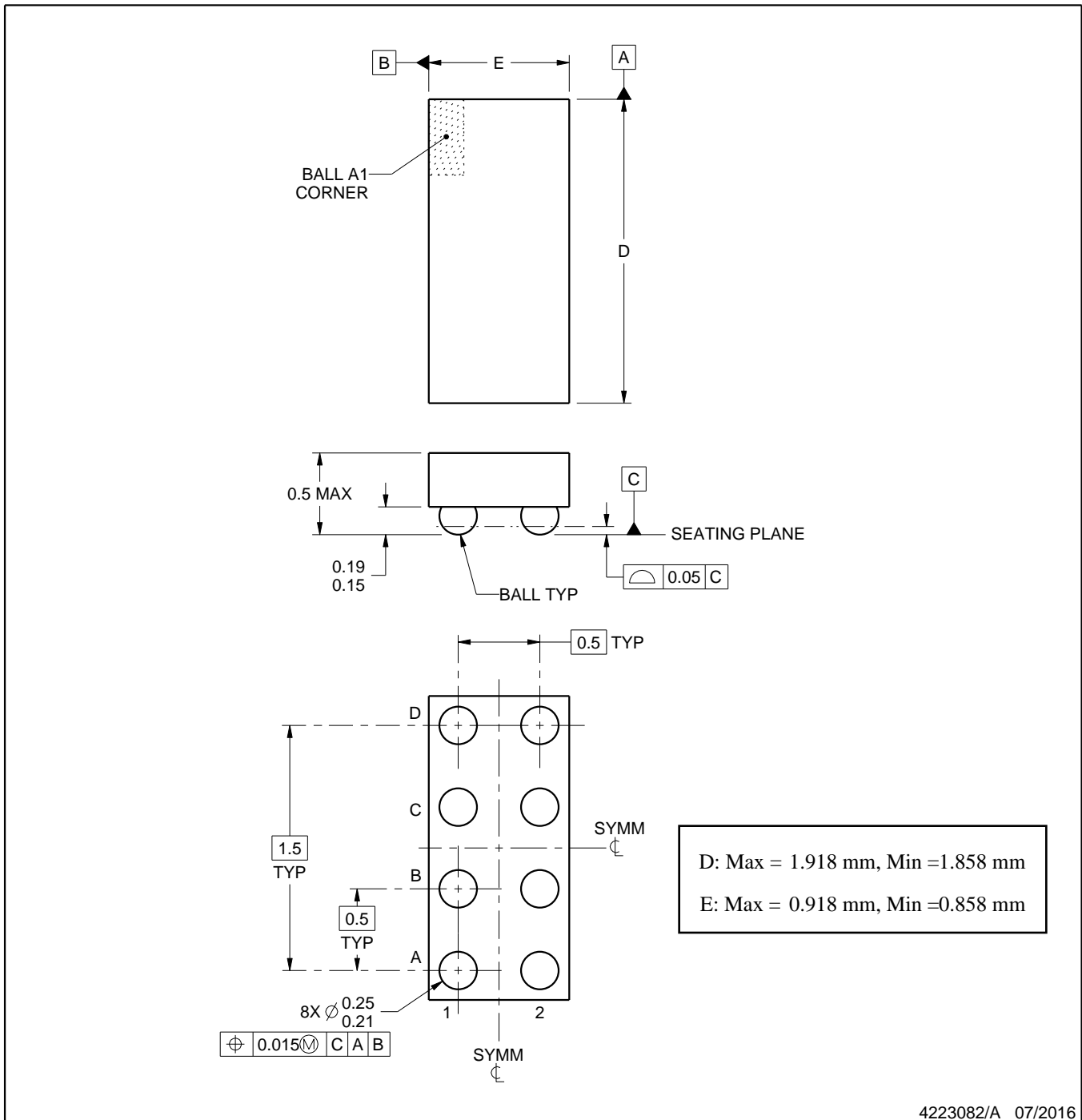
YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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